5x86 MICROPROCESSOR

Superpipelined x86 Compatible CPU

Cyrix®
Advancing the Standards

Introduction

♦ 586-CLASS PERFORMANCE
- 100 and 120 MHz core speeds with 33, 40, and 50 MHz bus options
- 16 KByte write-back cache
- Superpipelining and branch prediction
- Data forwarding
- Decoupled load/store unit
- On-chip FPU with 64-bit interface

♦ SMALL FOOTPRINT
- 208-pin QFP, 168-pin PGA

♦ BUILT-IN POWER MANAGEMENT
- System management mode
- Suspend mode
- FPU, pipeline, and cache auto idle
- Stop clock capability
- Operates at 3.45 V with 5 V tolerant I/O

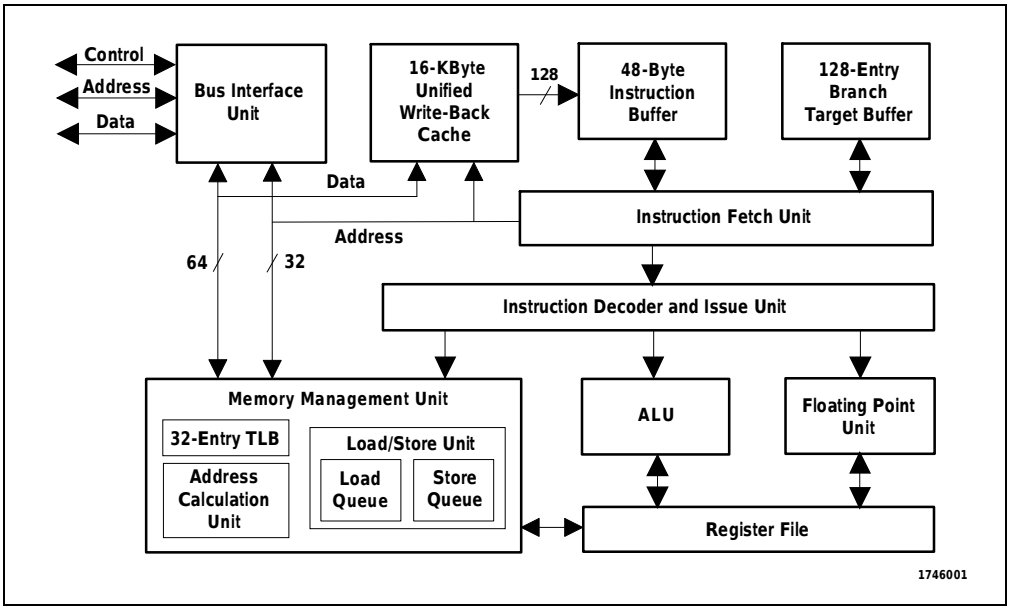
♦ x86 INSTRUCTION SET COMPATIBLE
- Runs Windows, DOS, UNIX, Novell and others

The Cyrix 5x86™ microprocessor is a high performance 586-class CPU compatible with all popular x86 operating systems, including DOS, Windows, Windows NT, Windows95, UNIX, Novell, OS/2 and Solaris.

The 586-class performance is achieved by a superpipelined architecture in the integer unit combined with data forwarding, branch prediction, a 16-KByte write-back cache, single-cycle instruction decode, and single-cycle execution.

The 5x86 processor provides many power saving features that make it ideal for power sensitive systems. The CPU automatically powers down the Floating Point Unit (FPU) and other internal circuits when they are not in use.

Fast entry into and exit from System Management Mode (SMM) allow frequent use of the SMM feature without noticeable performance degradation.



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PRELIMINARY

Cyrix® Advancing the Standards

1. ARCHITECTURE OVERVIEW

The Cyrix 5x86 family represents a new generation of x86-compatible 64-bit microprocessors with fifth-generation features. The Branch Target Buffer provides branch prediction with accuracy averaging 80%. The decoupled Load/Store unit allows multiple instructions in a single clock cycle. Other features include single-cycle execution, single-cycle instruction decode, 16-KByte Write-Back cache, and clock rates up to 120 MHz made possible by the use of advanced process technologies and superpipelining. The 100-MHz core speed option can operate with a bus speed of either 33 MHz or 50 MHz. The 120-MHz core speed option operates with a bus speed of 40 MHz.

The 5x86 CPU operates from a 3.45-volt power supply, resulting in lower power consumption at all clock frequencies. Where additional power savings are required (especially in portable applications), designers can make use of suspend mode, stop clock capability, and System Management Mode (SMM).

1.1 Major Functional Blocks

The 5x86 CPU is divided into major functional blocks as shown in the overall block diagram on the first page of this manual.

- Integer Unit
- Floating Point Unit
- Write-Back Cache
- Memory Management Unit
- Bus Interface Unit

The Integer Unit consists of the

- Instruction Buffer
- Instruction Fetch Unit
- Instruction Decoder and Issue Unit

Instructions are executed in the integer unit and in the floating point unit. The cache unit stores the most recently used data and instructions and provides fast access to this information for the integer and floating point units.

When external memory access is required, the physical address is calculated by the Memory Management Unit and then passed to the Bus Interface Unit, which provides the interface between the external system board and the processor's internal execution and cache units.

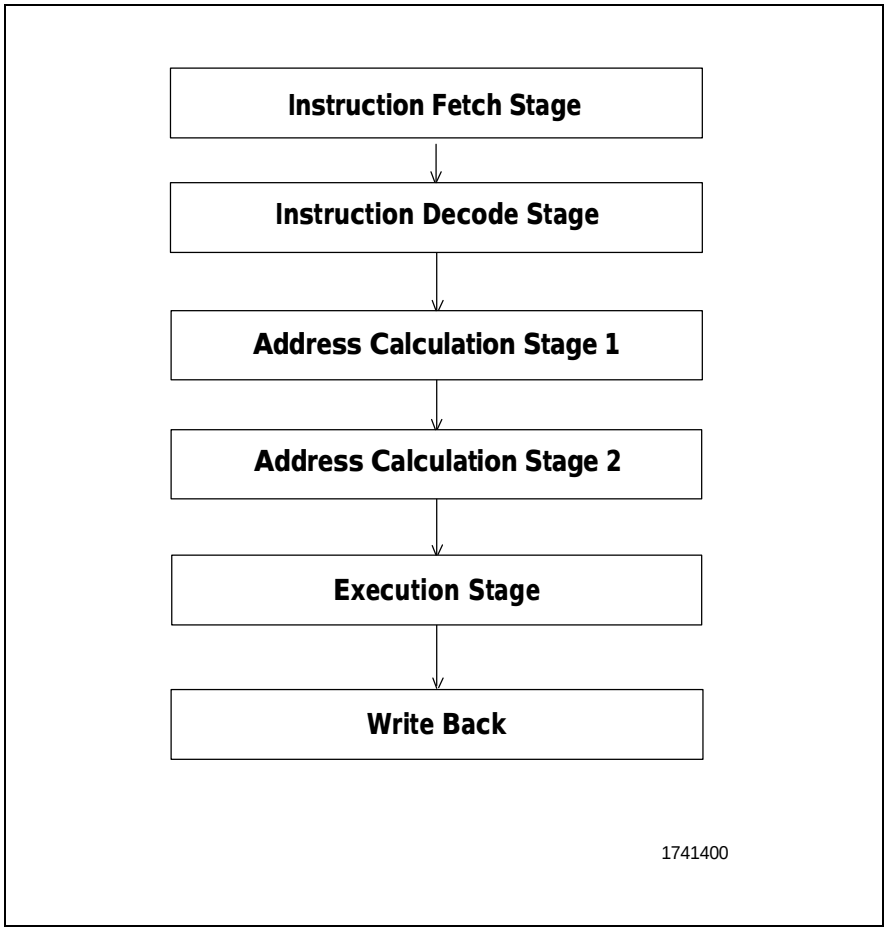

Figure 1-1. Integer-Unit Pipeline

1.2 Integer Unit

The superpipelined Integer Unit fetches, decodes, and executes x86 instructions through the use of a 6-stage integer pipeline (Figure 1-1).

1.2.1 Pipeline Stages

The **Instruction Fetch** pipe stage generates, from the on-chip cache, a continuous, high-speed instruction stream for use by the processor. Up to 128 bits of code are read during a single clock cycle.

Branch prediction logic, within the prefetch unit, generates a predicted target address for unconditional or conditional branch instructions. When a branch instruction is detected, the instruction fetch stage starts loading instructions at the predicted address within a single clock cycle. Up to 48 bytes of code are queued prior to the Instruction Decode stage.

The **Instruction Decode** stage evaluates the code stream provided by the instruction fetch stage and determines the number of bytes in each instruction and the instruction type. Instructions are processed and decoded at a maximum rate of one instruction per clock.

The **Address Calculation** function is super-pipelined and contains two stages, AC1 and AC2. If the instruction refers to a memory operand, the AC1 calculates a linear memory address for the instruction.

The AC2 stage performs any required memory management functions, cache accesses and register file accesses. If a floating point instruction is detected by AC2, the instruction is sent to the floating point unit for processing.

The **Execution** stage, under control of micro-code, executes instructions using the operands provided by the address calculation stage.

Write-Back, the last stage of the integer unit, updates the register file within the integer unit or writes to the load/store unit within the memory management unit.

1.2.2 Branch Control

Branch instructions occur, on average, every five instructions in x86-compatible programs. When the normal sequential flow of a program changes due to a branch instruction, the pipeline stages may stall because they are waiting for the CPU to calculate, retrieve and decode the new instruction stream. The 5x86 CPU minimizes the performance impact and latency of branch instructions by using branch prediction.

1.2.2.1 Branch Prediction

The 5x86 CPU uses a Branch Target Buffer (BTB) to store branch target addresses and branch prediction information. During the fetch stage, the instruction stream is checked for the presence of branch instructions. If an unconditional branch instruction is encountered, the 5x86 processor accesses the BTB to check for the branch instruction's target address. If the branch instruction hits in the BTB, the 5x86 CPU begins fetching at the target address specified by the BTB.

In the case of conditional branches, the BTB also provides history information to indicate whether the branch is more likely to be taken or not taken. If the conditional branch instruction hits in the BTB, the 5x86 CPU begins fetching instructions at the predicted target address. The decision to fetch the taken or not taken target address is based on a four-state branch prediction algorithm that achieves approximately 80% prediction accuracy. If the conditional branch misses in the BTB, the 5x86 processor predicts whether the branch will be taken or not-taken based on the opcode of the instruction.

Once fetched, a conditional branch instruction is decoded and then dispatched to the pipeline. The conditional branch instruction continues through the pipeline and is resolved in the EX stage.

Correctly predicted branch instructions execute in a single clock. If resolution of a branch indicates that a misprediction has occurred, the 5x86 CPU flushes the pipeline and starts fetching from the correct target address. Although the branch is resolved in the EX stage, the misprediction latency is five clock cycles. If a conditional branch misses in the BTB, the 5x86 CPU prefetches both the predicted path and the non-predicted path for each conditional branch, eliminating the cache access cycle on a misprediction.

Since the target address of a return (RET) instruction is dynamic rather than static, the 5x86 processor caches the target addresses for RET instructions in a return stack rather than in the BTB. The return address is pushed on the return stack during a CALL instruction and popped during the corresponding RET instruction.

1.3 Write-Back Cache

The 16-KByte write-back unified cache is a data/instruction cache and is configured as four-way set associative. The cache stores up to 16 KBytes of code and data in 1024 cache lines.

1.4 Memory Management Unit

The memory management unit translates the linear address supplied by the integer unit into a physical address to be used by the cache unit and the bus interface. Memory management procedures are x86-compatible, adhering to standard paging mechanisms.

The memory management unit also contains a load/store unit that is responsible for scheduling cache and external memory accesses. The load/store unit incorporates two performance-enhancing features:

- **Load-store reordering** that prioritizes memory reads required by the integer unit over writes to external memory
- **Memory-read bypassing** that eliminates unnecessary memory reads by using valid data still in the execution unit.

1.5 Floating Point Unit

The 5x86 processor floating point unit interfaces to the integer unit and the cache unit through a 64-bit bus. The 5x86 CPU FPU is x87-instruction-set compatible and adheres to the IEEE-754 standard. Because most applications contain FPU instructions mixed with integer instructions, the 5x86 FPU achieves high performance by completing integer and FPU operations in parallel.

FPU instructions are dispatched to the pipeline within the integer unit. The address calculation stage of the pipeline checks for memory management exceptions and accesses memory operands for use by the FPU. Once the instructions and operands have been provided to the FPU, the FPU completes instruction execution independently of the integer unit.

1.6 Bus Interface Unit

The Bus Interface Unit provides the signals and timing required by external circuitry. The signal descriptions and bus interface timing information is provided in Chapter 3 and Chapter 4 of this manual.

2.3.2.4 Configuration Registers

The 5x86 CPU provides four 8-bit Configuration Control Registers (CCR1, CCR2, CCR3 and CCR4) that include control for the on-chip write-back cache, and SMM features. The CPU also provides a Power Management Control Register (PMR), two 8-bit internal read-only device identification registers (DIR0 and DIR1), one 24-bit SMM Address Region Register (SMAR), and an eight-bit Performance Control Register PCR0. The CCR, PMR, DIR, PCR0, and SMAR registers exist in I/O memory space and are selected by a "register index" number as listed in Table 2-10 (Page 2-24).

Access to these registers is achieved by writing the index of the register to I/O port 22h. I/O port 23h is then used for data transfer. Each I/O port 23h data transfer must be preceded by an I/O port 22h register index selection, otherwise the second and later I/O port 23h operations are directed off-chip and produce external I/O cycles. If the register index number is outside the C0h-CFh, FEh-FFh range, external I/O cycles will also occur.

If the MAPEN field in CCR3 is is set to 0001, then access can be made to the CCR4, PCR0, and PMR registers. Otherwise, external I/O cycles will occur if the register index number is outside the range C0-CFh, FEh, FFh. The MAPEN field must remain 0 during normal operation to allow system registers located at port 22h to be accessed.

Table 2-10. Configuration Register Summary

REGISTER and INDEX		MAPEN	7	6	5	4	3	2	1	0
Performance Control [PCR0]	20h*	1h	LSSER					LOOP_EN	BTB_EN	RSTK_EN
Control 1 [CCR1]	C1h	xh					MMAC	SMAC	USE_SMI	
Control 2 [CCR2]	C2h	xh	USE_SUSP	BWRT		WT1	SUSP_HALT	LOCK_NW	USE_WBAK	
Control 3 [CCR3]	C3h	xh	MAPEN3	MAPEN2	MAPEN1	MAPEN0	SMM_MODE	LINBRST	NMI_EN	SMI_LOCK
Control 4 [CCR4]	E8h*	1h				DTE_EN	MEM_BYP	IORT2	IORT1	IORT0
SMM Address [SMAR0]	CDh	xh	A31	A30	A29	A28	A27	A26	A25	A24
SMM Address [SMAR1]	CEh	xh	A23	A22	A21	A20	A19	A18	A17	A16
SMM Address [SMAR2]	CFh	xh	A15	A14	A13	A12	S1ZE3	SIZE2	SIZE1	SIZE0
Power Management [PMR]	F0h*	1h						HLF_CLK	CLK1	CLK0
Device ID0 [DIR0]	FEh	xh	DEVICE_ID**							
Device ID1 [DIR1]	FFh	xh	SID3	SID2	SID1	SID0	RID3	RID2	RID1	RID0

Note: The following register index numbers are reserved for future use: C0h through CFh and FEh, FFh.
*Note: MAPEN must be set to access these registers.
** Note: Refer to Table 2-1 “Initialized Register Controls” on page 2-2 for Device_ID information

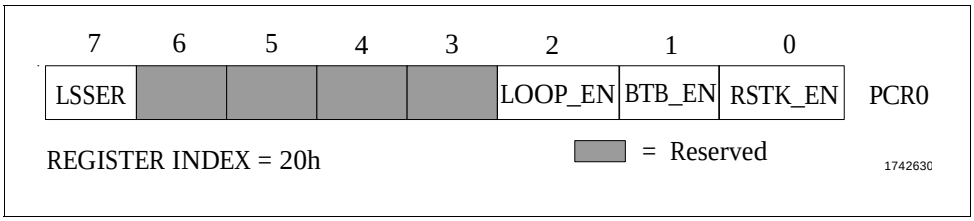

Figure 2-13. Performance Control Register 0 (PCR0)

Table 2-11. PCR0 Bit Definitions

BIT POSITION	NAME	DESCRIPTION
0	RSTK_EN	Return Stack Enable. If = 1: the Return Stack is enabled and RET instructions will speculatively execute the code following the associated CALL to improve performance. If = 0: the Return Stack is not enabled and optimum performance will not be achieved.
1	BTB_EN	Branch Target Buffer enable. If = 1: the Branch Target Buffer is enabled and branch prediction occurs. If = 0: no branch prediction will occur.
2	LOOP_EN	Loop Enable. If = 1: the CPU will not flush the prefetch buffer if the destination of a jump is already present in the prefetch buffer. This eliminates the need for a read from the cache and thus improves performance.
3-6		Reserved.
7	LSSER	Load Store Serialize Enable (Reorder Disable). If = 1: all memory reads and writes will occur in execution order (load store serializing enabled, reordering disabled). If = 0: memory reads and writes can be reordered for optimum performance (load store serializing disabled, reordering enabled). Memory accesses in the address range 640K to 1M will always be issued in execution order. LSSER should be set to ensure that memory-mapped I/O devices operating outside of the address range 640K to 1M will operate correctly.

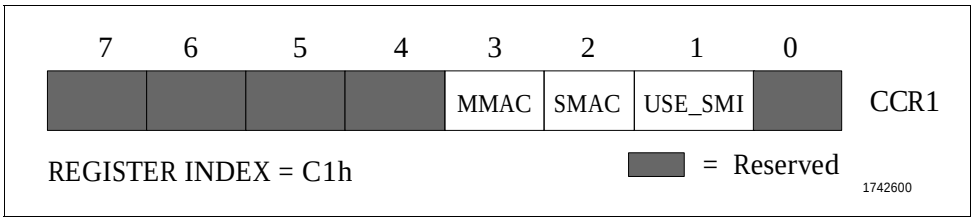

Figure 2-14. Configuration Control Register 1 (CCR1)

Table 2-12. CCR1 Bit Definitions

BIT POSITION	NAME	DESCRIPTION
1*	USE_SMI	Enable SMM Pins If = 1: SMI# input/output pin and SMADS# output pin are enabled. If = 0: SMI# input pin ignored and SMADS# output pin floats.
2*	SMAC	System Management Memory Access If = 1: Any access to addresses within the SMM memory space cause external bus cycles to be issued with SMADS# output active. SMI# input is ignored. If = 0: No effect on access.
3*	MMAC	Main Memory Access If = 1: All data accesses which occur within an SMI service routine (or when SMAC = 1) access main memory instead of SMM memory space. If = 0: No effect on access.

Note: Bits 0, 4-7 are reserved. Bits 1-3 are cleared to 0 at reset.
*Note: Access enabled by CCR3, bit 0, SMI-Lock bit.

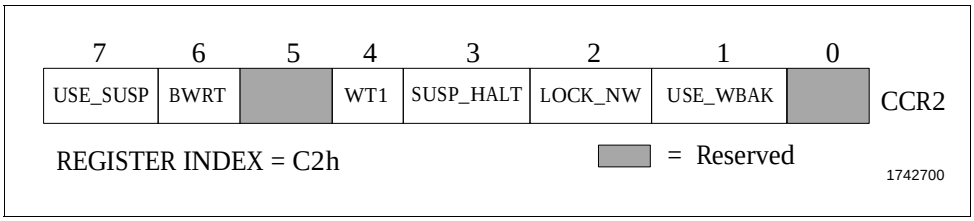

Figure 2-15. Configuration Control Register 2 (CCR2)

Table 2-13. CCR2 Bit Definitions

1	USE_WBAK	Enable Write-Back Cache Interface Pins If = 1: Enable INVAL and WM_RST input pins, CACHE#, and HITM# output pins. When enabling write-back cache mode, the USE_WBAK bit must be set prior to setting the NW bit in CR0. If = 0: INVAL and WM_RST input pins are ignored, and CACHE# and HITM# output pins float.
2	LOCK_NW	LOCK NW Bit If = 1: Prohibits changing the state of the NW bit in CR0.
3	SUSP_HALT	Suspend on HALT If = 1: CPU enters suspend mode following execution of a HALT instruction.
4	WT1	Write-Through Region 1 If = 1: Forces all writes to the address region between 640 KBytes to 1 MByte that hit in the on-chip cache to be issued on the external bus.
6	BWRT	Enable Burst Write Cycles If = 1: Enables use of 16-byte burst write-back cycles.
7	USE_SUSP	Enable Suspend Pins If = 1: SUSP# input and SUSPA# output are enabled. If = 0: SUSP# input is ignored and SUSPA# output floats.

Note: Bits 0 and 5 are reserved. Bits 1-4, 6 and 7 are cleared to 0 at reset.

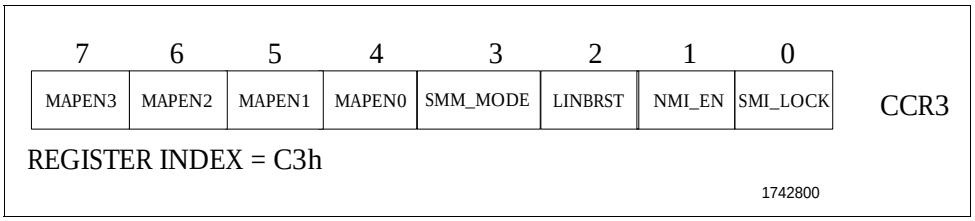

Figure 2-16. Configuration Control Register 3 (CCR3)

Table 2-14. CCR3 Bit Definitions

BIT POSITION	NAME	DESCRIPTION
0	SMI_LOCK	SMM Register Lock If = 1: the following SMM control bits can not be modified: CCR1 bits: 1, 2, and 3 CCR3 bit: 1 all SMAR bits. However, while operating within a SMI handler these SMM control bits can be modified. Once set, the SMI_LOCK bit can only be cleared by asserting the RESET pin.
1*	NMI_EN	NMI Enable If = 1: NMI is enabled during SMM. If = 0: NMI is not recognized during SMM.
2	LINBRST	Linear Address Burst Cycles If = 1: linear address sequence is used while performing burst cycles. If = 0: "1+4" address sequencing is used while performing burst cycles.
3*	SMM_MODE	SMM Mode If = 1: SMM pins function as defined for SL-compatible mode. If = 0: SMM pins function as defined for standard Cyrix SMM mode.
4-7	MAPEN[3-0]	MAP Enable If = 1h: all configuration registers are accessible. All accesses to port 22h are trapped. If = 0h: only configuration registers C0h through CFh, FEh and FFh are accessible.

Note: Bits 0-7 are cleared to zero at reset.
*Note: Access defined by CCR3, bit 0, SMI-Lock bit.

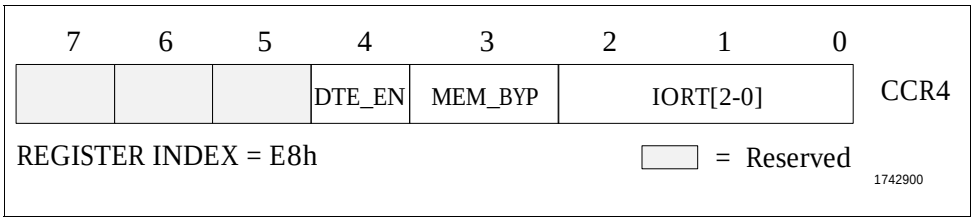

Figure 2-17. Configuration Control Register 4 (CCR4)

Table 2-15. CCR4 Bit Definitions

BIT POSITION	NAME	DESCRIPTION
2 - 0	IORT[2-0]	I/O Recovery Time Specifies the minimum number of bus clocks between I/O accesses: 0h = no clock delay 1h = 2-clock delay 2h = 4-clock delay 3h = 8-clock delay 4h = 16-clock delay 5h = 32-clock delay (default value after RESET) 6h = 64-clock delay 7h = 128-clock delay
3	MEM_BYP	If = 1: Memory read bypassing is enabled. If = 0: Memory read bypassing is disabled.
4	DTE_EN	Enable Directory Table Entry Cache If = 1: the Directory Table Entry cache is enabled. If = 0: the Directory Table Entry cache is disabled.

Note: Bits 0-4 are cleared to zero at reset, bits 5-7 are reserved.

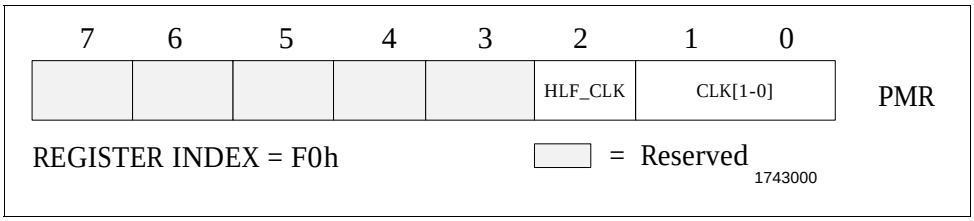

Figure 2-18. Power Management Register (PMR)

Table 2-16. PMR Bit Definitions

BIT POSITION	NAME	DESCRIPTION
1 - 0	CLK[1-0]	Core Clock/Bus Clock Ratio If = 0h: ratio = 1/1 If = 1h: ratio = 2/1 (default power-up for CLKMUL pin = 0) If = 2h: ratio = reserved If = 3h: ratio = 3/1 (default power-up for CLKMUL pin = 1) At reset, the CLK[1-0] bits are initialized to 1h if CLKMUL = 0, or to 3h if CLKMUL = 1. After reset is completed, CLK[1-0] bits may be set to 0h in order to obtain lower power consumption. The default power-up value must be restored when peak CPU performance is required.
2	HLF_CLK	Half Speed Clock If = 1: the CPU core operates at half the speed of the external bus clock regardless of the CLK[1-0] bits except during external bus transfers. When an external bus transfer occurs, the core clock frequency automatically increases in frequency for the duration of the transfer. When the transfer is complete, the core returns to half the frequency of the bus.

Note: Bit 2 is cleared to zero at reset, bits 3-7 are reserved.

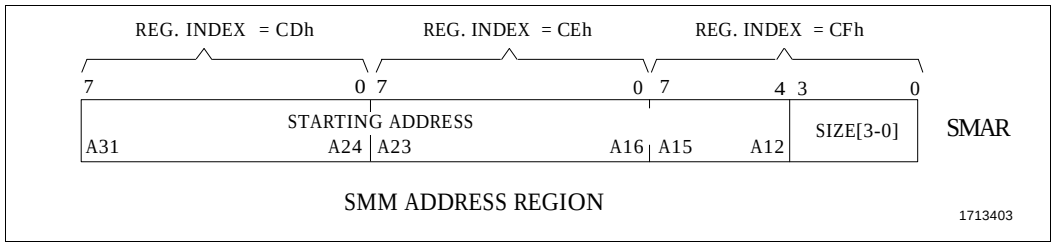

Figure 2-19. SMM Address Region Registers (SMAR)

Note: The SMAR register is accessed as three unique registers using separate register indices CDh, CEh and CFh.
Note: Access to the SMAR register is enabled by CCR3 bit 0, SMI_LOCK bit.

Table 2-17. SMAR-SIZE Field Bit Definitions

SIZE (3-0)	BLOCK SIZE	SIZE (3-0)	BLOCK SIZE
0h	Disabled	8h	512 KBytes
1h	4 KBytes	9h	1 MBytes
2h	8 KBytes	Ah	2 MBytes
3h	16 KBytes	Bh	4 MBytes
4h	32 KBytes	Ch	8 MBytes
5h	64 KBytes	Dh	16 MBytes
6h	128 KBytes	Eh	32 MBytes
7h	256 KBytes	Fh	4 KBytes (same as 1h)

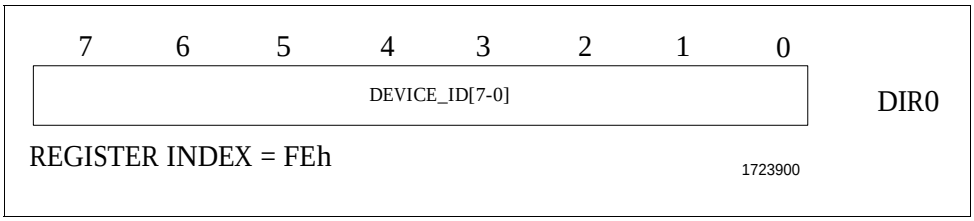

Figure 2-20. Device Identification Register 0 (DIR0)

Table 2-18. DIR0 Bit Definitions

BIT POSITION	NAME	DESCRIPTION
7 - 0	DEVICE_ID[7-0]	CPU Device Identification Number (read only). See Table 2-1 on page 2-2 for actual values.

4.0 ELECTRICAL SPECIFICATIONS

This section provides information on electrical connections, absolute maximum ratings, recommended operationg conditions, and DC characteristics, and AC characteristics. All voltage values in Electrical Specifications are with respect to V_{SS} unless otherwise noted.

4.1 Electrical Connections

4.1.1 Power and Ground Connections and Decoupling

Testing and operating the 5x86 CPU requires the use of standard high frequency techniques to reduce parasitic effects. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the V_{CC} and GND pins.

4.1.2 Pull-Up/Pull-Down Resistors

Table 4-1 lists the input pins that are internally connected to pull-up and pull-down resistors. When unused, these inputs do not require connection to external pull-up or pull-down resistors. The SUSP# pin is unique in that it is connected to a pull-up resistor only when SUSP# is not asserted. CLKMUL should not be connected to a switching signal.

Table 4-1. Pins Connected to Internal Pull-Up and Pull-Down Resistors

SIGNAL	RESISTOR
A20M#	20-kΩ pull-up
AHOLD	20-kΩ pull-down
BOFF#	20-kΩ pull-up
BS16#	20-kΩ pull-up
BS8#	20-kΩ pull-up
BRDY#	20-kΩ pull-up
CLKMUL	20-kΩ pull-up
EADS#	20-kΩ pull-up
FLUSH#	20-kΩ pull-up
IGNNE#	20-kΩ pull-up
INVAL	20-kΩ pull-up
KEN#	20-kΩ pull-up
RDY#	20-kΩ pull-up
SUSP#	20-kΩ pull-up
UP#	20-kΩ pull-up
WM_RST	20-kΩ pull-down

It is recommended that the ADS#, LOCK# and SMI# output pins be connected to pull-up resistors, as indicated in Table 4-2. The external pull-ups guarantee that the signals remain high (inactive) during hold acknowledge states.

Table 4-2. Pins Requiring External Pull-Up Resistors

SIGNAL	EXTERNAL RESISTOR
ADS#	20-kΩ pull-up
LOCK#	20-kΩ pull-up
SMI#	20-kΩ pull-up

4.1.3 Unused Input Pins

All inputs not used by the system designer and not listed in Table 4-1 (Page 4-1) should be kept at either ground or V_{CC}. To prevent possible spurious operation, connect active-high inputs to ground through a 20-kΩ (± 10%) pull-down resistor and active-low inputs to V_{CC} through a 20-kΩ (± 10%) pull-up resistor.

4.1.4 NC Designated Pins

Pins designated NC should be left disconnected. Connecting an NC pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

4.2 Absolute Maximum Ratings

Table 4-3 lists absolute maximum ratings for the 5x86 microprocessors. Stresses beyond the listed ratings may cause permanent damage to the device. Exposure to conditions beyond these limits may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced useful life and reliability These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" Table 4-4 (Page 4-3) is possible.

Table 4-3. Absolute Maximum Ratings

PARAMETER	ALL 5x86 CPUs		UNITS	NOTES
	MIN	MAX		
Operating Case Temperature	-65	110	°C	Power Applied
Storage Temperature	-65	150	°C	No Bias
Supply Voltage, V_{CC}	-0.5	4.0	V	
Voltage On Any Pin	-0.5	6.0	V	
Input Clamp Current, I_{IK}		10	mA	Power Applied
Output Clamp Current, I_{OK}		25	mA	Power Applied

4.3 Recommended Operating Conditions

Table 4-4 lists the recommended operating conditions for the 5x86 CPU.

Table 4-4. Recommended Operating Conditions

PARAMETER	ALL 5x86 CPUs		UNITS	NOTES
	MIN	MAX		
T_C Operating Case Temperature	0	85	°C	
V_{CC} Supply Voltage	3.3	3.6	V	
V_{IH} High Level Input	2.0	5.5	V	
V_{IL} Low Level Input Except CLK CLK	-0.3 -0.3	0.6 0.5	V	
I_{OH} Output Current (High)		-2.0	mA	$V_O=V_{OH(MIN)}$
I_{OL} Output Current (Low)		5.0	mA	$V_O=V_{OL(MAX\}}$

4.4 DC Characteristics

Table 4-5. DC Characteristics (at Recommended Operating Conditions)

PARAMETER	ALL 5x86 CPUs		UNITS	NOTES
	MIN	MAX		
V_{OL} Output Low Voltage		0.45	V	I_{OL} = 5 mA
V_{OH} Output High Voltage	2.4		V	I_{OH} = -2 mA
I_I Input Leakage Current for all pins except those with internal pull-ups or pull-downs		±15	µA	$0 < V_{IN} < V_{CC}$, See Table 4-1
I_{IH} Input Leakage Current for all pins with internal pull-downs.		200	µA	V_{IH} = 2.4 V, See Table 4-1
I_{IL} Input Leakage Current for all pins with internal pull-ups.		-400	µA	V_{IL} = 0.45 V, See Table 4-1
I_{CC} Active I_{CC} 5x86-100 at f_{CLK} = 100 MHz 5x86-120 at f_{CLK} = 120 MHz	 0.9 TYP 1.0 TYP	 1.2 1.4	A	Note 1
I_{CCSM} Suspend Mode I_{CC} 5x86-100 at f_{CLK} = 100 MHz 5x86-120 at f_{CLK} = 120 MHz	 20 TYP 50 TYP	 75 75	mA	Notes 1, 3
I_{CCSS} Standby I_{CC} (Suspended and CLK Stopped)	15 TYP	60	mA	f_{CLK} = 0 MHz, Note 4
C_{IN} Input Capacitance		20	pF	f = 1 MHz, Note 2
C_{OUT} Output or I/O Capacitance		20	pF	f = 1 MHz, Note 2
C_{CLK} CLK Capacitance		20	pF	f = 1 MHz, Note 2

Notes:
1. f_{CLK} ratings refer to internal clock frequency.
2. Not 100% tested.
3. All inputs are at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held are static except clock and all outputs are unloaded (static I_{OUT} = 0 mA). This specification is also valid for UP# = 0.
4. All inputs are at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs are held static and all outputs are unloaded (static I_{OUT} = 0 mA).

4.5 AC Characteristics

Tables 4-6 through 4-12 (Pages 4-7 through 4-12) list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1 (Page 4-6) and Figure 4-2 (Page 4-7). The rising-clock-edge reference level V_{REF}, and other reference levels are shown in Table 4-6 below. Input or output signals must cross these levels during testing.

Figure 4-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

Table 4-6. Drive Level and Measurement Points for Switching Characteristics

SYMBOL	VOLTAGE (Volts)
V_{REF}	1.5
V_{IHD}	2.3
V_{ILD}	0

Note: Refer to Figure 4-1.

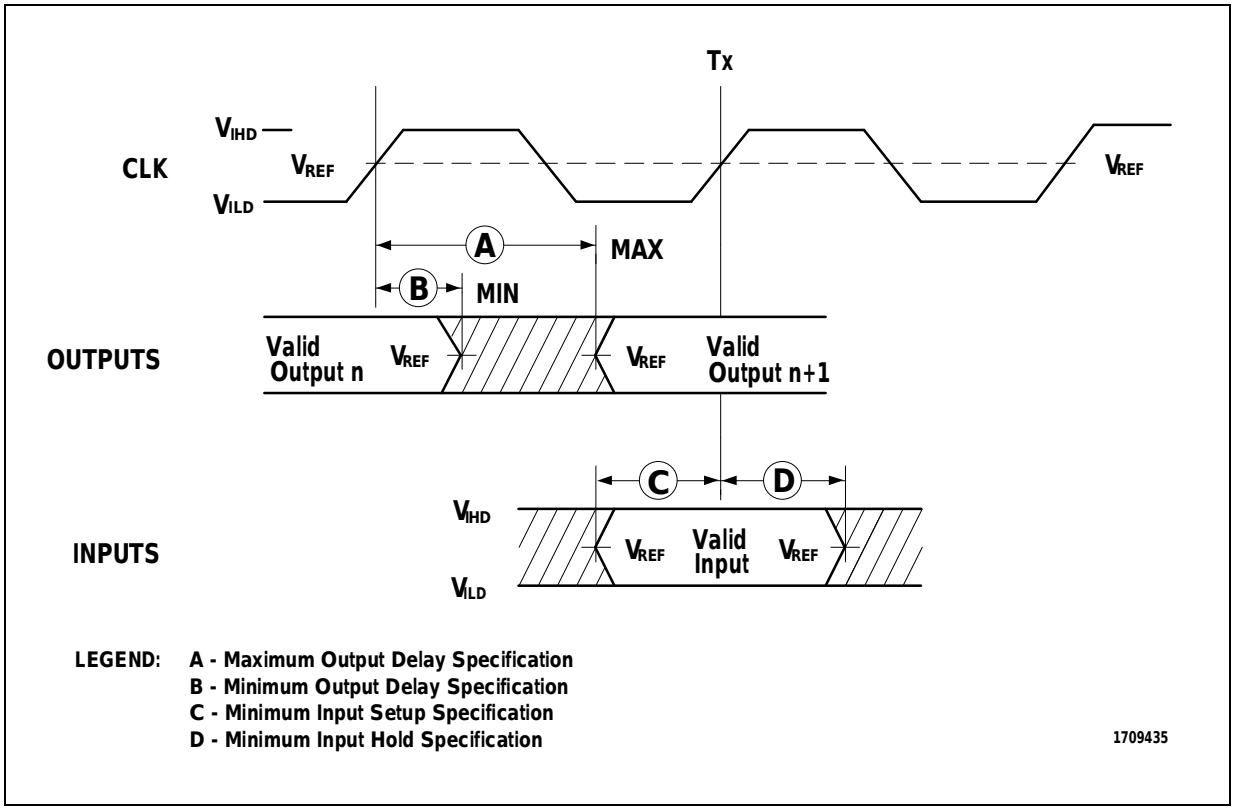

Figure 4-1. Drive Level and Measurement Points for Switching Characteristics

Table 4-7. Clock Specifications

T_{case} = 0 to 85 °C (See Figure 4-2)

	PARAMETER	5x86-100 33-MHz BUS		5x86-120 40-MHz BUS		5x86-100 50-MHz BUS		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
	CLK Frequency		33		40		50	MHz	
T1	CLK Period	30		25		20		ns	
T2	CLK Period Stability		± 250		± 250		± 250	ps	
T3	CLK High Time	11		9		7		ns	At 2 V
T4	CLK Low Time	11		9		7		ns	0.5 V
T5	CLK Fall Time		3		3		2	ns	2 to 0.5 V
T6	CLK Rise Time		3		3		2	ns	0.5 to 2 V

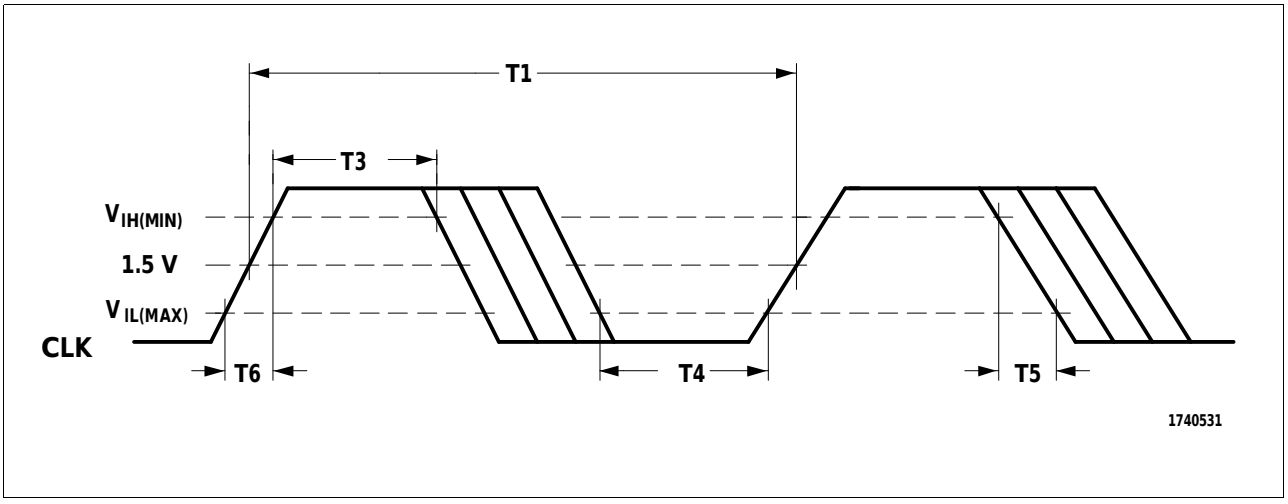

Figure 4-2. CLK Timing and Measurement Points

Table 4-8. Output Valid Delays
C_L = 50 pF, T_{case} = 0 to 85 °C (See Figure 4-3)

	PARAMETER	5x86-100 33-MHz BUS		5x86-120 40-MHz BUS		5x86-100 50-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
T7	All output signals not listed below	3	14	3	14	2	12	ns
T7a	D31 - D0, DP3 - DP0	3	14	3	14	3	12	ns
T7b	A19 - A2	3	14	3	14	2	10.5	ns

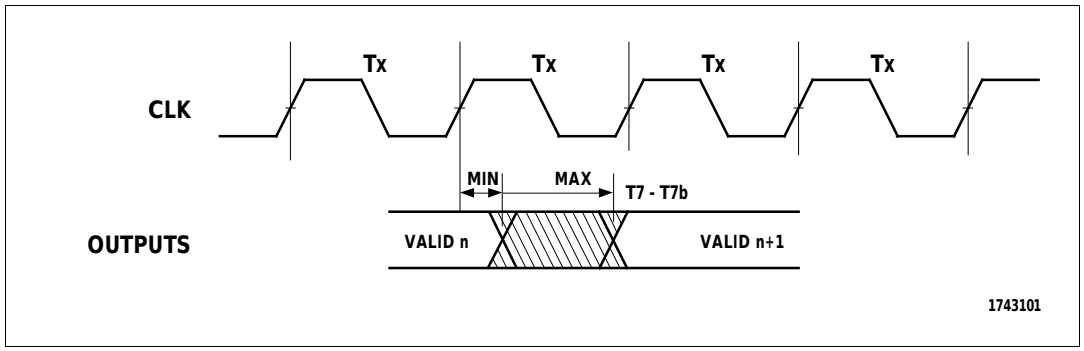

Figure 4-3. Output Valid Delay Timing

Table 4-9. Output Float Delays
C_L = 50 pF, T_{case} = 0 to 85 °C (See Figure 4-4)

	PARAMETER	5x86-100 33-MHz BUS		5x86-120 40-MHz BUS		5x86-100 50-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
T8	All output signals.		20		19		18	ns

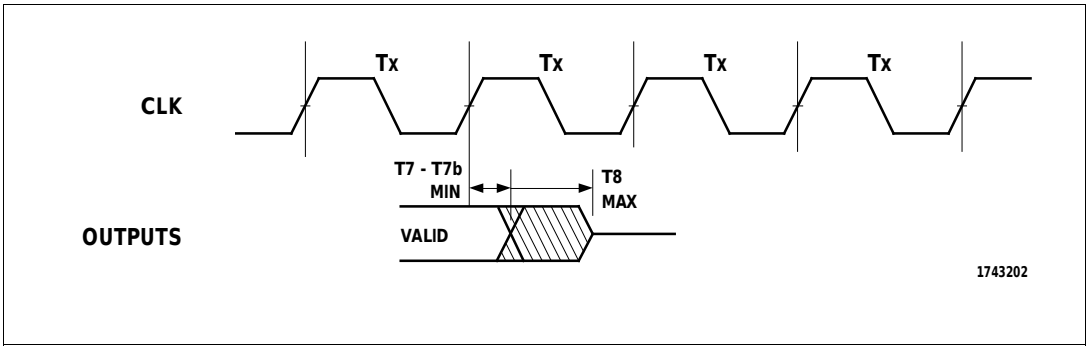

Figure 4-4. Output Float Delay Timing

Table 4-10. Input Setup Times

T_{case} = 0 to 85 °C (See Figure 4-5)

	PARAMETER	5x86-100 33-MHz BUS	5x86-120 40-MHz BUS	5x86-100 50-MHz BUS	UNITS
		MIN	MIN	MIN	
T9	All inputs not listed below	5	5	5	ns
T9a	HOLD, AHOLD	6	5	5	ns
T9b	BOFF#	7	6	5	ns
T9c	A31 - A4, D31 - D0, DP3 - DP0	5	5	4	ns

Table 4-11. Input Hold Times

T_{case} = 0 to 85 °C (See Figure 4-5)

	PARAMETER	5x86-100 33-MHz BUS	5x86-120 40 MHz-BUS	5x86-100 50-MHz BUS	UNITS
		MIN	MIN	MAX	
T10	All inputs	3	3	2	ns

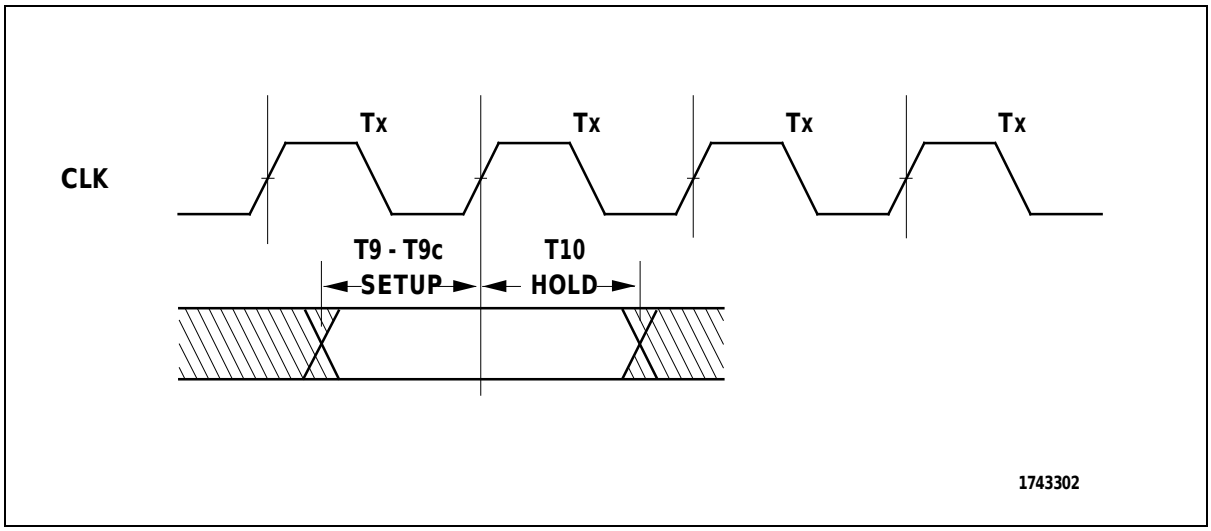

Figure 4-5. Input Setup and Hold Timing

Table 4-12. JTAG AC Specifications

SYMBOL	PARAMETER	ALL BUS FREQUENCIES		UNITS	FIGURE
		MIN	MAX		
	TCK Frequency (MHz)		25	ns	
T37	TCK Period	40		ns	4-6
T38	TCK High Time	10		ns	4-6
T39	TCK Low Time	10		ns	4-6
T40	TCK Rise Time		4	ns	4-6
T41	TCK Fall Time		4	ns	4-6
T42	TDO Valid Delay	3	25	ns	4-7
T43	Non-test Outputs Valid Delay	3	25	ns	4-7
T44	TDO Float Delay		30	ns	4-7
T45	Non-test Outputs Float Delay		36	ns	4-7
T47	TDI, TMS Setup Time	8		ns	4-7
T48	Non-test Inputs Setup Time	8		ns	4-7
T49	TDI, TMS Hold Time	7		ns	4-7
T50	Non-test Inputs Hold Time	7		ns	4-7

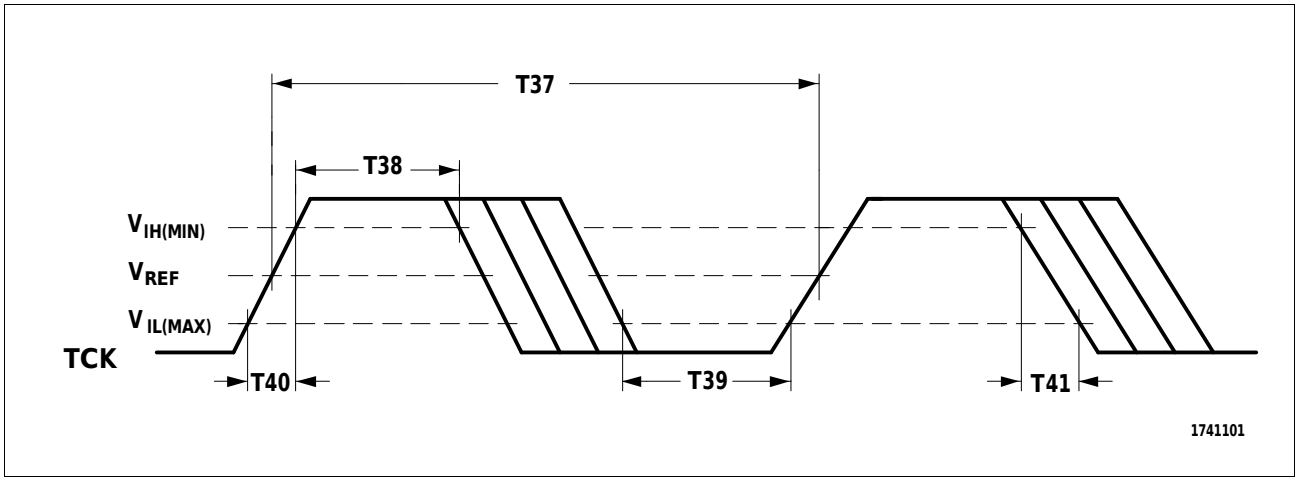

Figure 4-6. TCK Timing and Measurement Points

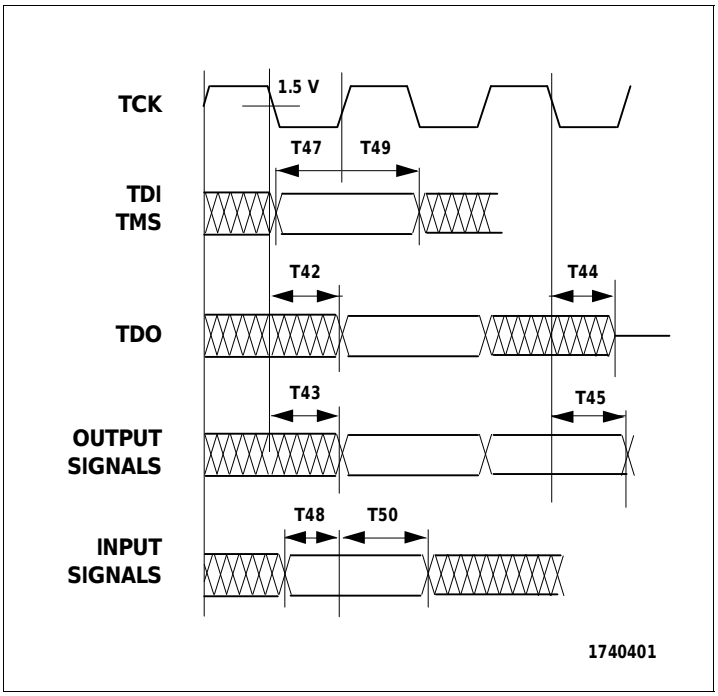

Figure 4-7. JTAG Test Timings

5.0 MECHANICAL SPECIFICATIONS

5.1 168-Pin PGA Package

The pin assignments for the 5x86-100GP and 5x86-120GP are shown in Figure 5-1. The pins are listed by signal name and pin number in Tables 5-1 and 5-2 respectively. Dimensions for the 168-pin PGA package are shown in Figure 5-2 and Table 5-3.

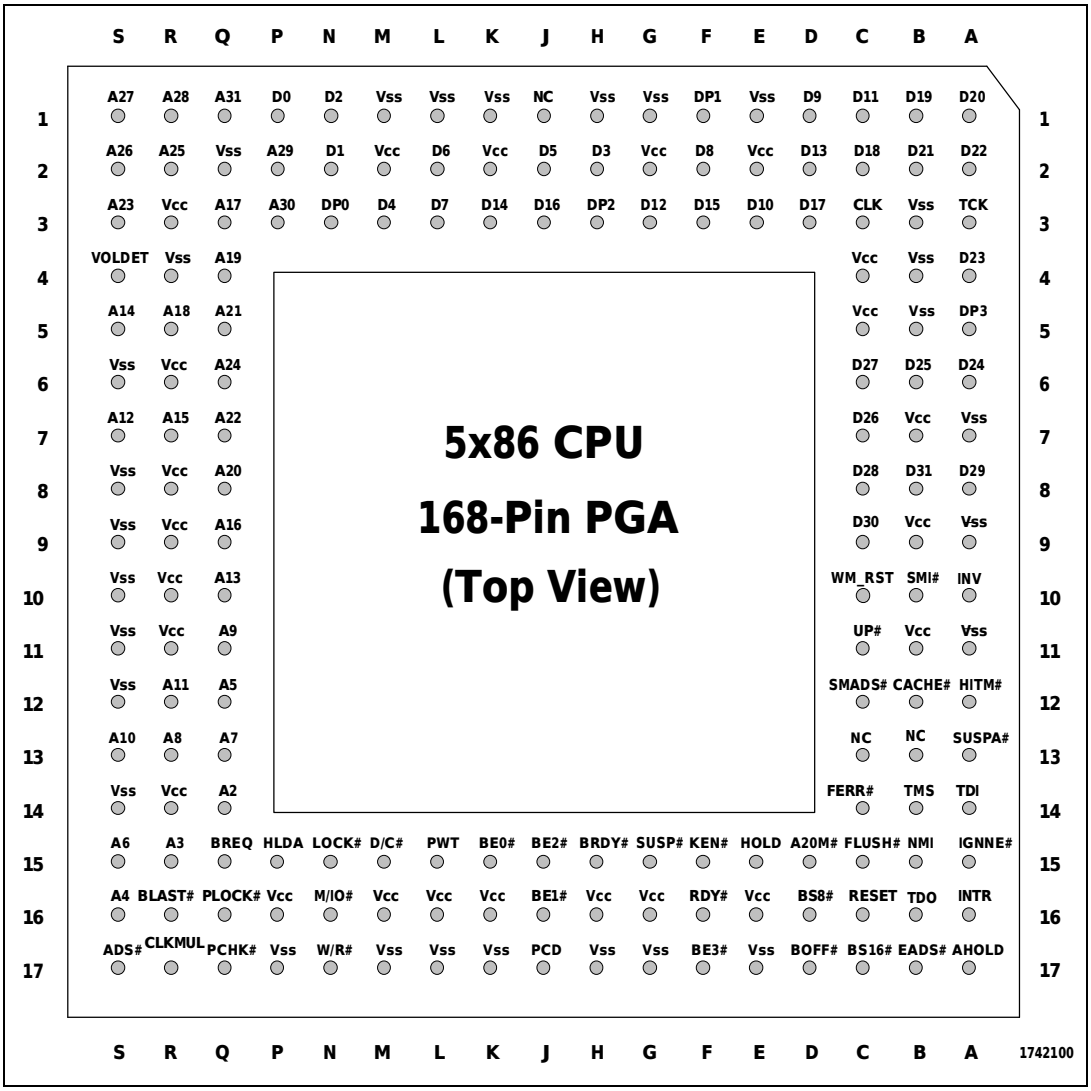

Figure 5-1. 168-Pin PGA Package Pin Assignments

Table 5-1. 168-Pin PGA Package Pin Numbers Sorted by Signal Name

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A2	Q14	A29	P2	D9	D1	FERR#	C14	TMS	B14	VSS	A11
A3	R15	A30	P3	D10	E3	FLUSH#	C15	UP#	C11	VSS	B3
A4	S16	A31	Q1	D11	C1	HITM#	A12	VCC	B7	VSS	B4
A5	Q12	ADS#	S17	D12	G3	HLDA	P15	VCC	B9	VSS	B5
A6	S15	AHOLD	A17	D13	D2	HOLD	E15	VCC	B11	VSS	E1
A7	Q13	BE0#	K15	D14	K3	IGNNE#	A15	VCC	C4	VSS	E17
A8	R13	BE1#	J16	D15	F3	INTR	A16	VCC	C5	VSS	G1
A9	Q11	BE2#	J15	D16	J3	INVAL	A10	VCC	E2	VSS	G17
A10	S13	BE3#	F17	D17	D3	KEN#	F15	VCC	E16	VSS	H1
A11	R12	BLAST#	R16	D18	C2	LOCK#	N15	VCC	G2	VSS	H17
A12	S7	BOFF#	D17	D19	B1	M/IO#	N16	VCC	G16	VSS	K1
A13	Q10	BRDY#	H15	D20	A1	NC	B13	VCC	H16	VSS	K17
A14	S5	BREQ	Q15	D21	B2	NC	C13	VCC	K2	VSS	L1
A15	R7	BS8#	D16	D22	A2	NC	J1*	VCC	K16	VSS	L17
A16	Q9	BS16#	C17	D23	A4	NMI	B15	VCC	L16	VSS	M1
A17	Q3	CACHE#	B12	D24	A6	PCD	J17	VCC	M2	VSS	M17
A18	R5	CLK	C3	D25	B6	PCHK#	Q17	VCC	M16	VSS	P17
A19	Q4	CLKMUL	R17	D26	C7	PLOCK#	Q16	VCC	P16	VSS	Q2
A20	Q8	D/C#	M15	D27	C6	PWT	L15	VCC	R3	VSS	R4
A20M#	D15	D0	P1	D28	C8	RDY#	F16	VCC	R6	VSS	S6
A21	Q5	D1	N2	D29	A8	RESET	C16	VCC	R8	VSS	S8
A22	Q7	D2	N1	D30	C9	SMADS#	C12	VCC	R9	VSS	S9
A23	S3	D3	H2	D31	B8	SMI#	B10	VCC	R10	VSS	S10
A24	Q6	D4	M3	DP0	N3	SUSP#	G15	VCC	R11	VSS	S11
A25	R2	D5	J2	DP1	F1	SUSPA#	A13	VCC	R14	VSS	S12
A26	S2	D6	L2	DP2	H3	TCK	A3	VOLDET	S4	VSS	S14
A27	S1	D7	L3	DP3	A5	TDI	A14	VSS	A7	W/R#	N17
A28	R1	D8	F2	EADS#	B17	TDO	B16	VSS	A9	WM_RST	C10

*Note: J1 is an internal no connect and may be connected to an external supply voltage.

Table 5-2. 168-Pin PGA Package Signal Names Sorted by Pin Number

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	D20	B12	CACHE#	D17	BOFF#	J15	BE2#	P2	A29	R7	A15
A2	D22	B13	NC	E1	VSS	J16	BE1#	P3	A30	R8	VCC
A3	TCK	B14	TMS	E2	VCC	J17	PCD	P15	HLDA	R9	VCC
A4	D23	B15	NMI	E3	D10	K1	VSS	P16	VCC	R10	VCC
A5	DP3	B16	TDO	E15	HOLD	K2	VCC	P17	VSS	R11	VCC
A6	D24	B17	EADS#	E16	VCC	K3	D14	Q1	A31	R12	A11
A7	VSS	C1	D11	E17	VSS	K15	BE0#	Q2	VSS	R13	A8
A8	D29	C2	D18	F1	DP1	K16	VCC	Q3	A17	R14	VCC
A9	VSS	C3	CLK	F2	D8	K17	VSS	Q4	A19	R15	A3
A10	INVAL	C4	VCC	F3	D15	L1	VSS	Q5	A21	R16	BLAST#
A11	VSS	C5	VCC	F15	KEN#	L2	D6	Q6	A24	R17	CLKMUL
A12	HITM#	C6	D27	F16	RDY#	L3	D7	Q7	A22	S1	A27
A13	SUSPA#	C7	D26	F17	BE3#	L15	PWT	Q8	A20	S2	A26
A14	TDI	C8	D28	G1	VSS	L16	VCC	Q9	A16	S3	A23
A15	IGNNE#	C9	D30	G2	VCC	L17	VSS	Q10	A13	S4	VOLDET
A16	INTR	C10	WM_RST	G3	D12	M1	VSS	Q11	A9	S5	A14
A17	AHOLD	C11	UP#	G15	SUSP#	M2	VCC	Q12	A5	S6	VSS
B1	D19	C12	SMADS#	G16	VCC	M3	D4	Q13	A7	S7	A12
B2	D21	C13	NC	G17	VSS	M15	D/C#	Q14	A2	S8	VSS
B3	VSS	C14	FERR#	H1	VSS	M16	VCC	Q15	BREQ	S9	VSS
B4	VSS	C15	FLUSH#	H2	D3	M17	VSS	Q16	PLOCK#	S10	VSS
B5	VSS	C16	RESET	H3	DP2	N1	D2	Q17	PCHK#	S11	VSS
B6	D25	C17	BS16#	H15	BRDY#	N2	D1	R1	A28	S12	VSS
B7	VCC	D1	D9	H16	VCC	N3	DP0	R2	A25	S13	A10
B8	D31	D2	D13	H17	VSS	N15	LOCK#	R3	VCC	S14	VSS
B9	VCC	D3	D17	J1*	NC	N16	M/IO#	R4	VSS	S15	A6
B10	SMI#	D15	A20M#	J2	D5	N17	W/R#	R5	A18	S16	A4
B11	VCC	D16	BS8#	J3	D16	P1	D0	R6	VCC	S17	ADS#

*Note: J1 is an internal no connect and may be connected to an external supply voltage.

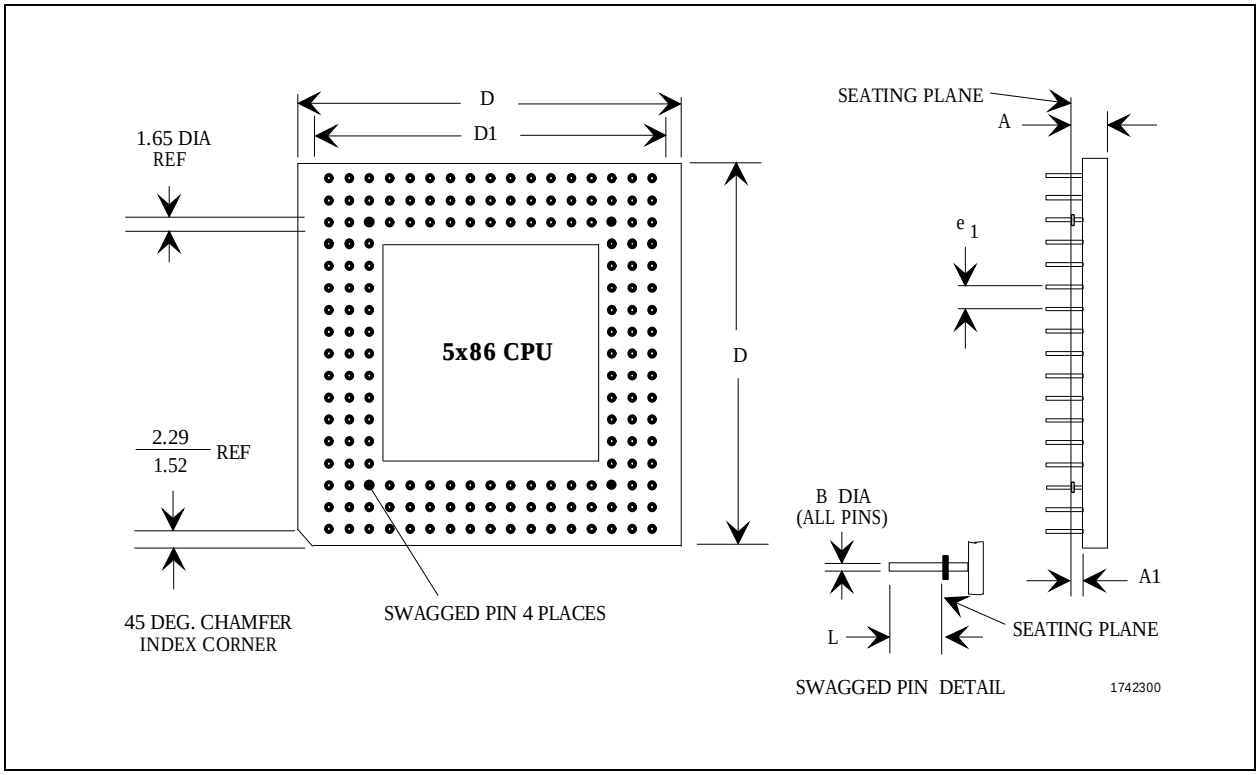

Figure 5-2. 168-Pin PGA Package

Table 5-3. 168-Pin PGA Package Dimensions

SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.56	4.57	0.140	0.180
A1	1.14	1.40	0.045	0.055
B	0.43	0.51	0.017	0.020
D	44.07	44.83	1.735	1.765
D1	40.51	40.77	1.595	1.605
e_1	2.29	2.79	0.090	0.110
L	2.54	3.30	0.100	0.130

5.2 208-Lead QFP Package

Pin Assignments

The pin assignments for the 5x86-100QP and 5x86-120QP are shown in Figure 5-3. Pins are listed by signal name in Table 5-4 and by pin number in Table 5-5 Package dimensions for the 208-lead QFP (Quad Flat Pack) are shown in Figure 5-4 and Table 5-6.

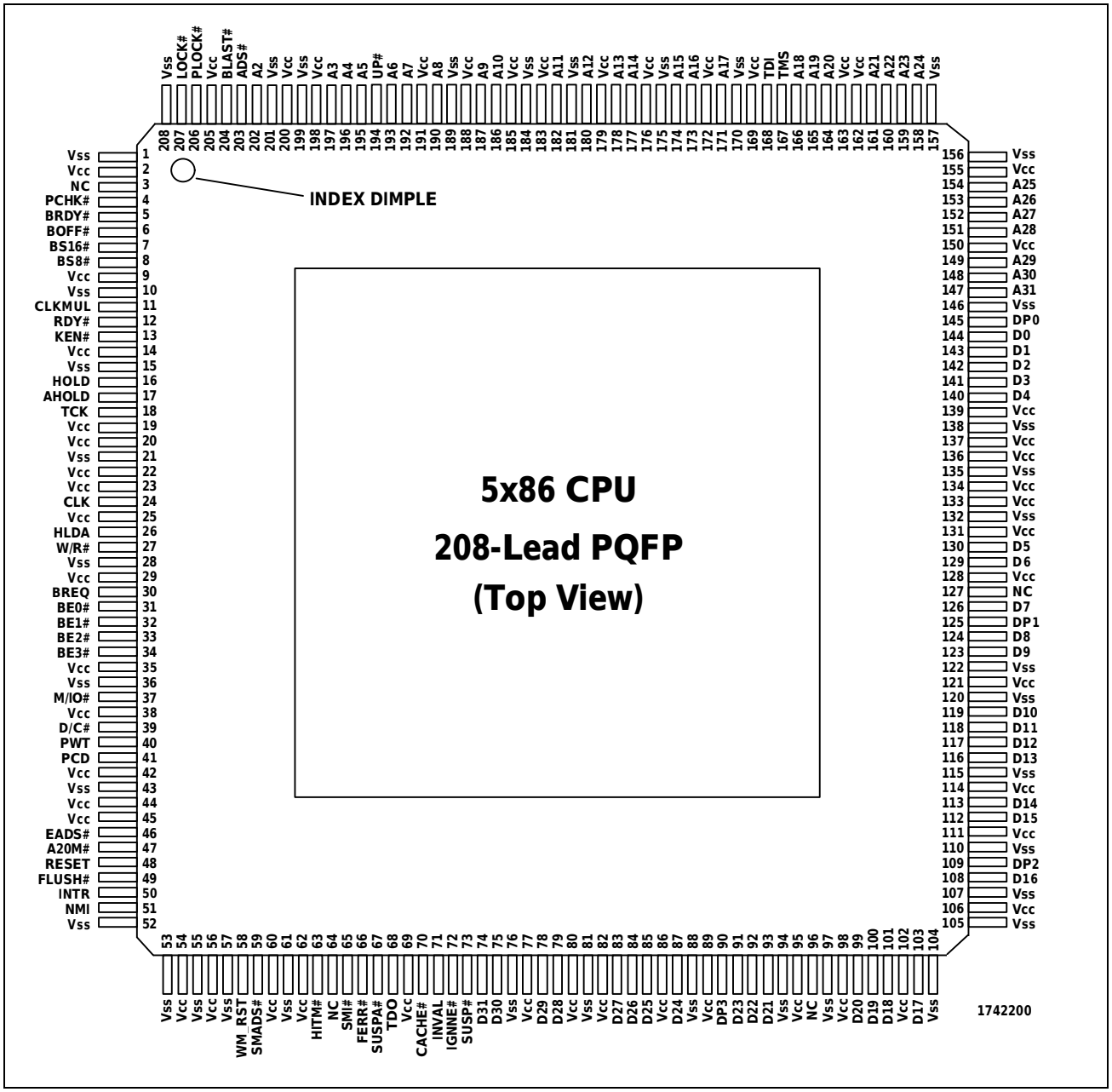

Figure 5-3. 208-Lead QFP Package Pin Assignments

Table 5-4. 208-Lead QFP Package Pins Sorted by Signal Name

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A2	202	BE2#	33	D24	87	RESET	48	Vcc	98	Vss	52
A3	197	BE3#	34	D25	85	SMADS#	59	Vcc	102	Vss	53
A4	196	BLAST#	204	D26	84	SMI#	65	Vcc	106	Vss	55
A5	195	BOFF#	6	D27	83	SUSP#	73	Vcc	111	Vss	57
A6	193	BRDY#	5	D28	79	SUSPA#	67	Vcc	114	Vss	61
A7	192	BREQ	30	D29	78	TCK	18	Vcc	121	Vss	76
A8	190	BS16#	7	D30	75	TDI	168	Vcc	128	Vss	81
A9	187	BS8#	8	D31	74	TDO	68	Vcc	131	Vss	88
A10	186	CACHE#	70	D/C#	39	TMS	167	Vcc	133	Vss	94
A11	182	CLK	24	DP0	145	UP#	194	Vcc	134	Vss	97
A12	180	CLKMUL	11	DP1	125	Vcc	2	Vcc	136	Vss	104
A13	178	D0	144	DP2	109	Vcc	9	Vcc	137	Vss	105
A14	177	D1	143	DP3	90	Vcc	14	Vcc	139	Vss	107
A15	174	D2	142	EADS#	46	Vcc	19	Vcc	150	Vss	110
A16	173	D3	141	FERR#	66	Vcc	20	Vcc	155	Vss	115
A17	171	D4	140	FLUSH#	49	Vcc	22	Vcc	162	Vss	120
A18	166	D5	130	HITM#	63	Vcc	23	Vcc	163	Vss	122
A19	165	D6	129	HLDA	26	Vcc	25	Vcc	169	Vss	132
A20	164	D7	126	HOLD	16	Vcc	29	Vcc	172	Vss	135
A20M#	47	D8	124	IGNNE#	72	Vcc	35	Vcc	176	Vss	138
A21	161	D9	123	INTR	50	Vcc	38	Vcc	179	Vss	146
A22	160	D10	119	INVAL	71	Vcc	42	Vcc	183	Vss	156
A23	159	D11	118	KEN#	13	Vcc	44	Vcc	185	Vss	157
A24	158	D12	117	LOCK#	207	Vcc	45	Vcc	188	Vss	170
A25	154	D13	116	M/IO#	37	Vcc	54	Vcc	191	Vss	175
A26	153	D14	113	NC	3*	Vcc	56	Vcc	198	Vss	181
A27	152	D15	112	NC	64	Vcc	60	Vcc	200	Vss	184
A28	151	D16	108	NC	96	Vcc	62	Vcc	205	Vss	189
A29	149	D17	103	NC	127	Vcc	69	Vss	1	Vss	199
A30	148	D18	101	NMI	51	Vcc	77	Vss	10	Vss	201
A31	147	D19	100	PCD	41	Vcc	80	Vss	15	Vss	208
ADS#	203	D20	99	PCHK	4	Vcc	82	Vss	21	WM_RST	58
AHOLD	17	D21	93	PLOCK#	206	Vcc	86	Vss	28	W/R#	27
BE0#	31	D22	92	PWT	40	Vcc	89	Vss	36		
BE1#	32	D23	91	RDY#	12	Vcc	95	Vss	43		

*Note: Pin 3 is an internal no connect and may be connected to an external supply voltage.

Table 5-5. 208-Lead QFP Package Signals Sorted by Pin Number

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Vss	36	Vss	71	INVAL	106	Vcc	141	D3	176	Vcc
2	Vcc	37	M/IO#	72	IGNNE#	107	Vss	142	D2	177	A14
3*	NC	38	Vcc	73	SUSP#	108	D16	143	D1	178	A13
4	PCHK#	39	D/C#	74	D31	109	DP2	144	D0	179	Vcc
5	BRDY#	40	PWT	75	D30	110	Vss	145	DP0	180	A12
6	BOFF#	41	PCD	76	Vss	111	Vcc	146	Vss	181	Vss
7	BS16#	42	Vcc	77	Vcc	112	D15	147	A31	182	A11
8	BS8#	43	Vss	78	D29	113	D14	148	A30	183	Vcc
9	Vcc	44	Vcc	79	D28	114	Vcc	149	A29	184	Vss
10	Vss	45	Vcc	80	Vcc	115	Vss	150	Vcc	185	Vcc
11	CLKMUL	46	EADS#	81	Vss	116	D13	151	A28	186	A10
12	RDY#	47	A20M#	82	Vcc	117	D12	152	A27	187	A9
13	KEN#	48	RESET	83	D27	118	D11	153	A26	188	Vcc
14	Vcc	49	FLUSH#	84	D26	119	D10	154	A25	189	Vss
15	Vss	50	INTR	85	D25	120	Vss	155	Vcc	190	A8
16	HOLD	51	NMI	86	Vcc	121	Vcc	156	Vss	191	Vcc
17	AHOLD	52	Vss	87	D24	122	Vss	157	Vss	192	A7
18	TCK	53	Vss	88	Vss	123	D9	158	A24	193	A6
19	Vcc	54	Vcc	89	Vcc	124	D8	159	A23	194	UP#
20	Vcc	55	Vss	90	DP3	125	DP1	160	A22	195	A5
21	Vss	56	Vcc	91	D23	126	D7	161	A21	196	A4
22	Vcc	57	Vss	92	D22	127	NC	162	Vcc	197	A3
23	Vcc	58	WM_RST	93	D21	128	Vcc	163	Vcc	198	Vcc
24	CLK	59	SMADS#	94	Vss	129	D6	164	A20	199	Vss
25	Vcc	60	Vcc	95	Vcc	130	D5	165	A19	200	Vcc
26	HLDA	61	Vss	96	NC	131	Vcc	166	A18	201	Vss
27	W/R#	62	Vcc	97	Vss	132	Vss	167	TMS	202	A2
28	Vss	63	HITM#	98	Vcc	133	Vcc	168	TDI	203	ADS#
29	Vcc	64	NC	99	D20	134	Vcc	169	Vcc	204	BLAST#
30	BREQ	65	SMI#	100	D19	135	Vss	170	Vss	205	Vcc
31	BE0#	66	FERR#	101	D18	136	Vcc	171	A17	206	PLOCK#
32	BE1#	67	SUSPA#	102	Vcc	137	Vcc	172	Vcc	207	LOCK#
33	BE2#	68	TDO	103	D17	138	Vss	173	A16	208	Vss
34	BE3#	69	Vcc	104	Vss	139	Vcc	174	A15		
35	Vcc	70	CACHE#	105	Vss	140	D4	175	Vss		

*Note: Pin 3 is an internal no connect and may be connected to an external supply voltage.

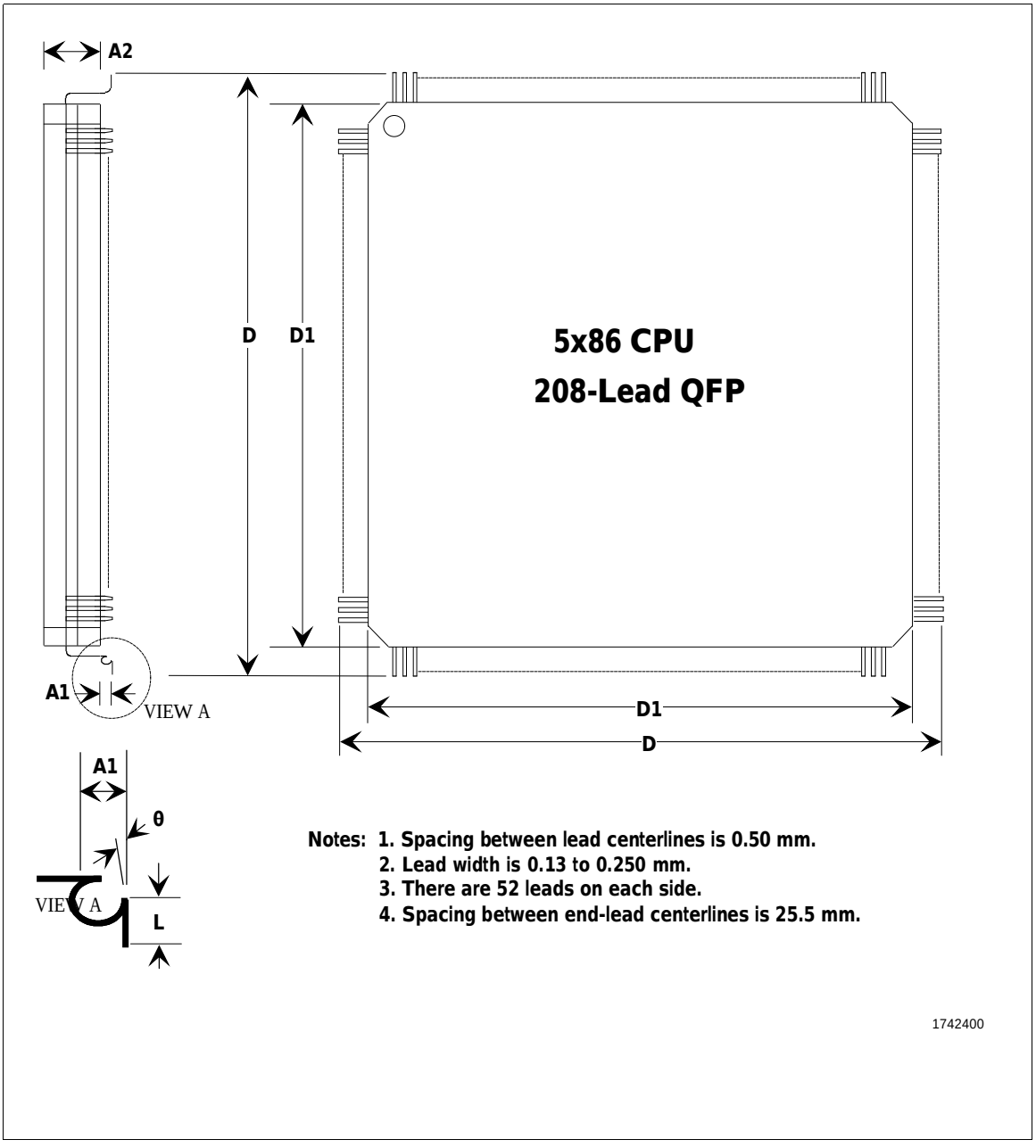

Figure 5-4. 208-Lead QFP Package

Table 5-6. 208-Lead QFP Package Dimensions

SYMBOL	MILLIMETERS		INCHES		DEGREES	
	MIN	MAX	MIN	MAX	MIN	MAX
A1	0.28	0.41	0.011	0.017		
A2	3.29	3.45	0.130	0.136		
D	30.35	30.85	1.195	1.215		
D1	27.90	28.10	1.095	1.107		
L	0.50	0.70	0.019	0.028		
θ					0	7

5.3 Thermal Characteristics

The 5x86 processor is designed to operate when the case temperature at the top center of the package is between 0°C and 85°C. The maximum die (junction) temperature, $T_{J\ MAX}$, and the maximum ambient temperature, $T_{A\ MAX}$, can be calculated by substituting thermal resistance and maximum values for case or junction temperature and power dissipation in the following equations:

$$T_J = T_C + (P * \theta_{JC})$$

$$T_A = T_J - (P * \theta_{JA})$$

where:

T_A = Ambient temperature (°C)
T_J = Average junction temperature (°C)
T_C = Case temperature at top center of package (°C)
P = Power dissipation (W)
θ_{JC} = Junction-to-case thermal resistance (°C/W)
θ_{JA} = Junction-to-ambient thermal resistance (°C/W).

PGA Package

Table 5-7 lists the junction-to-ambient and junction-to-case thermal resistances for the 5x86 processors in the 168-pin PGA (pin grid array) package. These devices have a "G" package suffix as shown in the appendix. Table 5-8 lists the maximum ambient temperatures permitted for various clock frequencies at maximum I_{CC} and V_{CC} = 3.6 volts. The heatsink used to measure the data below is characterized by θ_{JA} = 10 °C/W.

Table 5-7. PGA Package Thermal Resistance with No Airflow

PGA THERMAL RESISTANCE (°C/W)			
WITH HEATSINK		WITHOUT HEATSINK	
θ_{JA}	θ_{JC}	θ_{JA}	θ_{JC}
12.5	2.5	17	2.0

Table 5-8. PGA Package Maximum Ambient Temperature
(with Heatsink, Airflow = 0)

CPU INTERNAL CLOCK FREQUENCY	AMBIENT TEMPERATURE
100 MHz	42 ºC
120 MHz (5x86-120GP devices only)	35 ºC

QFP Package

Table 5-9 lists the junction-to-ambient and junction-to-case thermal resistances for the 5x86 processors in the QFP (quad flat pack) package without a heat sink. These devices have a "Q" package suffix as shown in the appendix.

Table 5-9. QFP Package Thermal Resistance
(without Heatsink)

AIRFLOW (LFM)	QFP THERMAL RESISTANCE (°C/W)	
	θ_{JA}	θ_{JC}
0	16	2
100	14	2

Table 5-10. QFP Package Maximum Ambient Temperature
(without Heatsink)

CPU INTERNAL CLOCK FREQUENCY	AIRFLOW (LFM)	AMBIENT TEMPERATURE (°C)
100 MHz	0	25
	100	33
120 MHz (5x86-120GP devices only)	0	14
	100	25

Heatsinking is required for most applications. The appropriate heat sink will have a total case-to-heatsink and heatsink-to-ambient thermal resistance ($\theta_{CH} + \theta_{HA}$) no larger than the value resulting from the equation below.

$$\theta_{CH} + \theta_{HA} = (T_{C\ MAX} - T_{A\ MAX}) / (V_{CC\ MAX} * I_{CC\ MAX})$$

where:

$T_{C\ MAX}$ = 85°C

$V_{CC\ MAX}$ = 3.6 V

$I_{CC\ MAX}$ = the appropriate value from Table 4-5 on page 4-4

$T_{A\ MAX}$ = maximum ambient temperature required by the application

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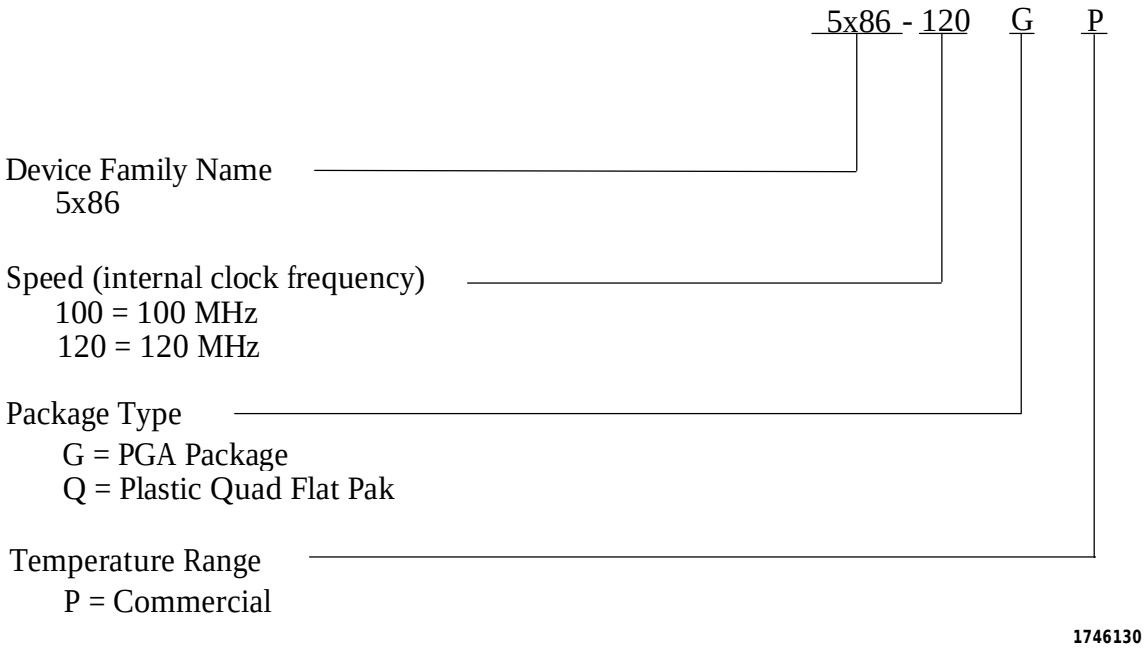
Appendix

A

Ordering Information



Cyrix 5x86 part numbers are listed below:

5x86 CPU Part Numbers

PART NUMBER	FREQUENCY (MHz)		PACKAGE	
	BUS	INTERNAL	QFP	PGA
5x86-100GP	33	100		x
	50	100		x
5x86-120GP	40	120		x
5x86-100QP	33	100	x	
	50	100	x	
5x86-120QP	40	120	x	