6x86-P200+ PROCESSOR

Sixth-Generation Superscalar
Superpipelined x86-Compatible CPU

6x86-P200+ PROCESSOR DATA BOOK ADDENDUM

θ♦ Sixth-Generation Superscalar Superpipelined Architecture

- Operating frequency of 150 MHz core, 75 MHz bus
- Optimized to run both 16-bit and 32-bit software applications
- Dual 7-stage integer pipelines
- High performance 80-bit FPU with 64-bit interface
- 16-KByte unified write-back L1 cache

♦ Best In-Class Performance Through Superior Architecture

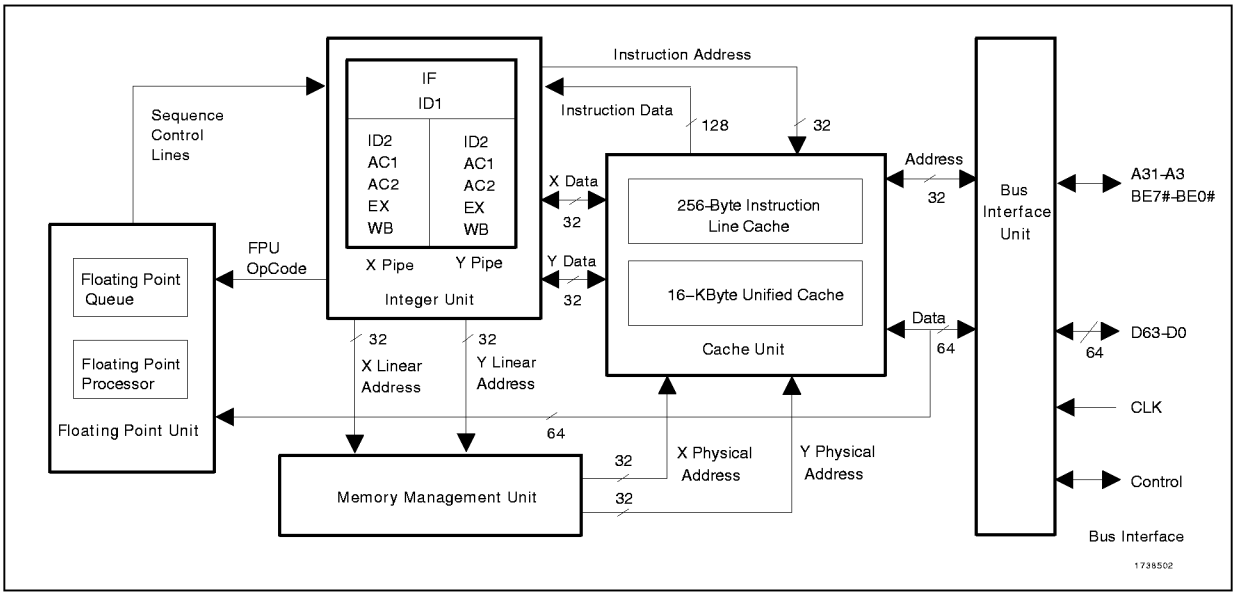
- Register renaming
- Out-of-order completion
- Data dependency removal
- Multi-branch prediction
- Speculative execution

♦ X86 Instruction Set Compatible

- Runs Windows 95, Windows 3.x, Windows NT, DOS, UNIX, OS/2, Solaris, and others

The Cyrix 6x86™-P200+ has an identical architecture compared to previous 6x86 processors, but operates at a core frequency of 150 MHz. The 6x86 series of CPUs are superscalar, superpipelined sixth generation CPUs that offer the highest level of performance available for desktop personal computers. Optimized to run both 16-bit and 32-bit software applications, the 6x86 processor is fully compatible with the x86 instruction set and delivers industry-leading performance running Windows® 95, Windows, Windows NT, OS/2®, DOS Solaris, UNIX® and other operating systems.

The 6x86 processor achieves top performance through the use of two optimized superpipelined integer units and an on-chip floating point unit. Additionally, the integer and floating point units are optimized for maximum instruction throughput by using advanced architectural techniques including register renaming, out-of-order completion, data dependency removal, branch prediction and speculative execution. These design innovations eliminate many data dependencies and resource conflicts to achieve high performance when executing existing 16-bit and future 32-bit software applications.



1.0 OVERVIEW

The Cyrix 6x86–P200+ Processor operates at a frequency of 150 MHz, and interfaces to a system with a 75 MHz bus. This document includes the electrical specifications for the 6x86–P200+ devices. The 6x86–P200+ timing information is included for refrence. Refer to the *6x86 Processor Data Book* for complete information on the achitecture, programming interface and bus interface.

2.0 ELECTRICAL SPECIFICATIONS

2.1 Electrical Connections

This section provides information on electrical connections, absolute maximum ratings, recommended operating conditions, DC characteristics, and AC characteristics. All voltage values in Electrical Specifications are measured with respect to V_{SS} unless otherwise noted.

2.2 Power and Ground Connections and Decoupling

Testing and operating the 6x86 CPU requires the use of standard high frequency techniques to reduce parasitic effects. The high clock frequencies used in the 6x86 CPU and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the V_{CC} and GND pins. The 6x86 CPU contains 296 pins with 53 pins connected to V_{CC} and 53 connected to V_{SS} (ground).

2.3 Pull-Up/Pull-Down Resistors

Table 4–1 lists the input pins that are internally connected to pull-up and pull-down resistors. The pull-up resistors are connected to V_{CC} and the pull-down resistors are connected to V_{SS}. When unused, these inputs do not require connection to external pull-up or pull-down resistors. The SUSP# pin is unique in that it is connected to a pull-up resistor only when SUSP# is not asserted.

Table 4–1. Pins Connected to Internal Pull-Up and Pull-Down Resistors

SIGNAL	PIN NO.	RESISTOR
BRDYC#	Y3	20-kΩ pull-up
CLKMUL	Y33	20-kΩ pull-down
QDUMP#	AL7	20-kΩ pull-up
SMI#	AB34	
SUSP#	Y34	20-kΩ pull-up (see text)
TCK	M34	20-kΩ pull-up
TDI	N35	
TMS	P34	
TRST#	Q33	
Reserved	J33	
Reserved	W35	
Reserved	Y35	
Reserved	AN35	20-kΩ pull-down

2.3.1 Unused Input Pins

All inputs not used by the system designer and not listed in Table 4–1 should be connected either to ground or to V_{CC}. Connect active–high inputs to ground through a 20 kΩ (± 10%) pull–down resistor and active–low inputs to V_{CC} through a 20 kΩ (± 10%) pull–up resistor to prevent possible spurious operation.

2.3.2 NC and Reserved Pins

Pins designated NC have no internal connections. Pins designated RESV or RESERVED should be left disconnected. Connecting a reserved pin to a pull–up resistor, pull–down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

2.4 Absolute Maximum Ratings

Table 2–1 lists the absolute maximum ratings for the 6x86 Processors. For further information on these ratings refer to the *6x86 Processor Data Book*.

Table 2–1. Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS	NOTES
Operating Case Temperature	-65	110	°C	Power Applied
Storage Temperature	-65	150	°C	
Supply Voltage, V_{CC}	-0.5	4.0	V	
Voltage On Any Pin	-0.5	V_{CC} + 0.5	V	
Input Clamp Current, I_{IK}		10	mA	Power Applied
Output Clamp Current, I_{OK}		25	mA	Power Applied

2.5 Recommended Operating Conditions

Table 2–2 presents the recommended operating conditions for the 6x86 CPU device.

Table 2–2. Recommended Operating Conditions

PARAMETER	MIN	MAX	UNITS	NOTES
T_C Operating Case Temperature	0	70	°C	Power Applied
V_{CC} Supply Voltage	3.15	3.70	V	
V_{IH} High-Level Input Voltage	2.0	5.5	V	
V_{IL} Low-Level Input Voltage	-0.3	0.8	V	
I_{OH} High-Level Output Current		-1.0	mA	$V_O=V_{OH(MIN)}$
I_{OL} Low-Level Output Current		5.0	mA	$V_O=V_{OL(MAX)}$

2.6 DC Characteristics

Table 2–3. DC Characteristics (at Recommended Operating Conditions)

PARAMETER		MIN	TYP	MAX	UNITS	NOTES
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 5 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –1 mA
I_I	Input Leakage Current For all pins except those listed in Table 4–1.			±15	µA	$0 < V_{IN} < V_{CC}$
I_{IH}	Input Leakage Current For all pins with internal pull-downs.			200	µA	V_{IH} = 2.4 V See Table 4–1.
I_{IL}	Input Leakage Current For all pins with internal pull-ups.			–400	µA	V_{IL} = 0.45 V See Table 4–1.
I_{CC}	Active I_{CC} 150 MHz		5.9	7.0	A	Note 1, 5
I_{CCSM}	Suspend Mode I_{CC} 150 MHz		64	105	mA	Note 1, 3, 5
I_{CCSS}	Standby I_{CC} 0 MHz (Suspended/CLK Stopped)		35	55	mA	Note 4,5
C_{IN}	Input Capacitance			15	pF	f = 1 MHz, Note 2
C_{OUT}	Output Capacitance			20	pF	f = 1 MHz, Note 2
C_{OUT}	I/O Capacitance			25	pF	f = 1 MHz, Note 2
C_{CLK}	CLK Capacitance			15	pF	f = 1 MHz, Note 2

Notes:
1. Frequency (MHz) ratings refer to the internal clock frequency.
2. Not 100% tested.
3. All inputs at 0.4 or V_{CC} –0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I_{OUT} = 0 mA).
4. All inputs at 0.4 or V_{CC} –0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I_{OUT} = 0 mA).
5. Typical, measured at V_{CC} = 3.52 V.

2.7 AC Characteristics

Tables 2–6 through 2–11 (Pages 2–7 through 2–13) list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 2–1 (Page 2–5) and Figure 2–2 (Page 2–6). The rising clock edge reference level V_{REF} and other reference levels are shown in Table 2–4. Input or output signals must cross these levels during testing.

Figure 2–1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

The AC tables lists the 6x86–P166$^+$ (66 MHz) device for comparison with the 6x86–P200$^+$ (75 MHz).

The correspondence between core frequency, bus frequency and Performance (P) rating is shown Table 2–4. The plus sign ($^+$) indicates that testing has shown that the performance of the device was actually higher than its stated P rating.

Table 2–4. 6x86 Devices

DEVICE NUMBER	FREQUENCY (MHz)	
	CORE	BUS
6x86–P90$^+$GP	80	40
6x86–P120$^+$GP	100	50
6x86–P133$^+$GP	110	55
6x86–P150$^+$GP	120	60
6x86–P166$^+$GP	133	66
6x86–P200$^+$GP	150	75

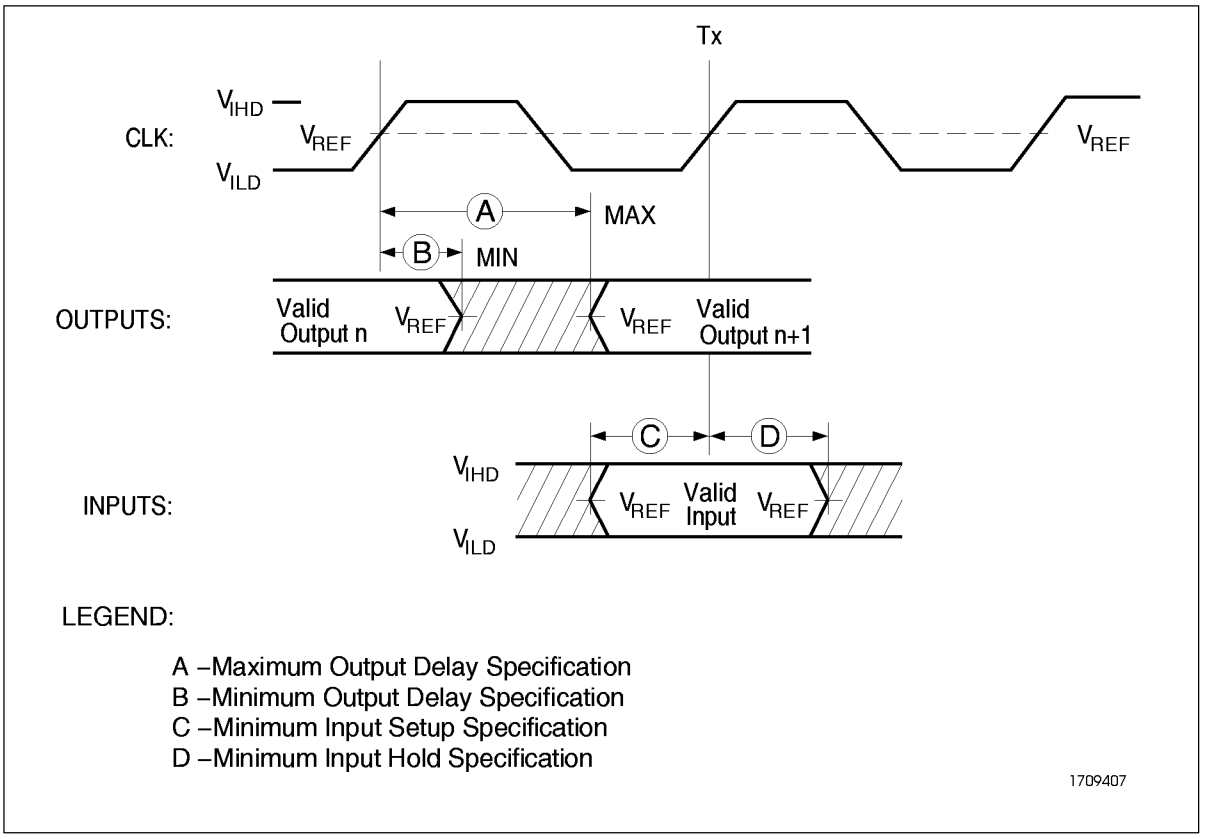


Figure 2–1. Drive Level and Measurement Points for Switching Characteristics

Table 2–5. Drive Level and Measurement Points for Switching Characteristics

SYMBOL	VOLTAGE (Volts)
V_{REF}	1.5
V_{IHD}	2.3
V_{ILD}	0

Note: Refer to Figure 2–1.

Table 2-6. Clock Specifications

T_{CASE} = 0°C to 70°C, See Figure 2-2

	PARAMETER	66-MHz BUS		75-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	
	CLK Frequency		66.6		75	MHz
T1	CLK Period	15.0	30.0	13.3	26.7	ns
T2	CLK Period Stability		±250		± 250	ps
T3	CLK High Time	4.0		4.0		ns
T4	CLK Low Time	4.0		4.0		ns
T5	CLK Fall Time	0.15	1.5	0.15	1.5	ns
T6	CLK Rise Time	0.15	1.5	0.15	1.5	ns

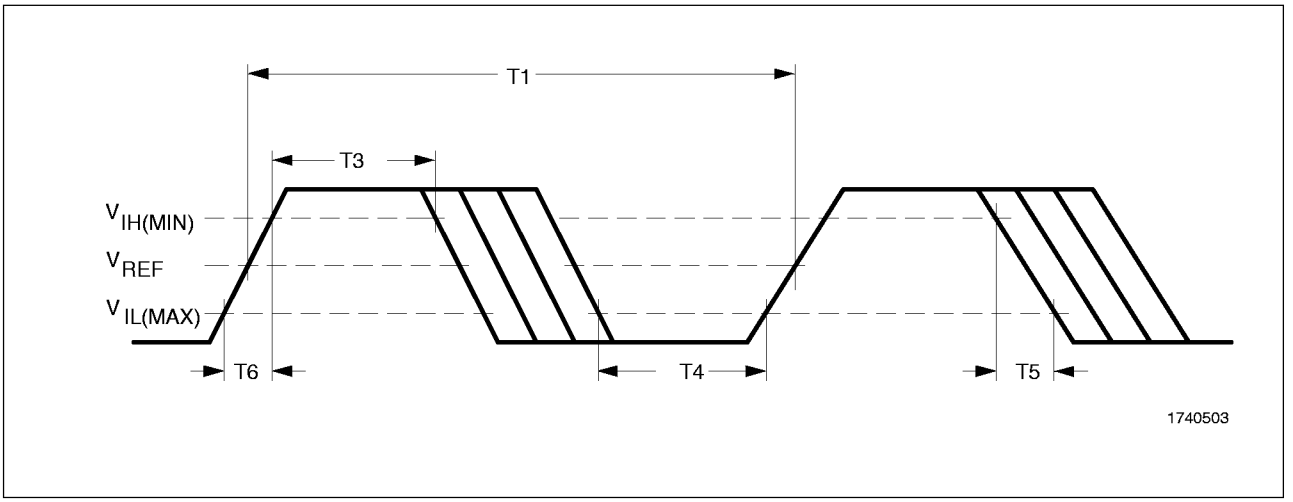


Figure 2-2. CLK Timing and Measurement Points

Table 2–7. Output Valid Delays

C_L = 50 pF, T_{case} = 0°C to 70°C, See Figure 2–3

	PARAMETER	66–MHz BUS		75–MHz BUS		UNITS
		MIN	MAX	MIN	MAX	
T7a	A31–A3, BE7#–BE0#, CACHE#, D/C#, LBA#, LOCK#, PCD, PWT, SCYC, SMIACT#, W/R#	1.0	7.0	1.0	7.0	ns
T7b	ADS#, M/IO#	1.0	6.0	1.0	6.0	ns
T8	ADSC#	1.0	7.0	1.0	7.0	ns
T9	AP	1.0	8.5	1.0	8.5	ns
T10	APCHK#, PCHK#, FERR#	1.0	7.0	1.0	7.0	ns
T11	D63–D0, DP7–DP0 (Write)	1.3	7.5	1.3	7.5	ns
T12a	HIT#	1.0	8.0	1.0	8.0	ns
T12b	HITM#	1.1	6.0	1.1	6.0	ns
T13	BREQ, HLDA	1.0	8.0	1.0	8.0	ns
T14	SUSPA#	1.0	8.0	1.0	8.0	ns

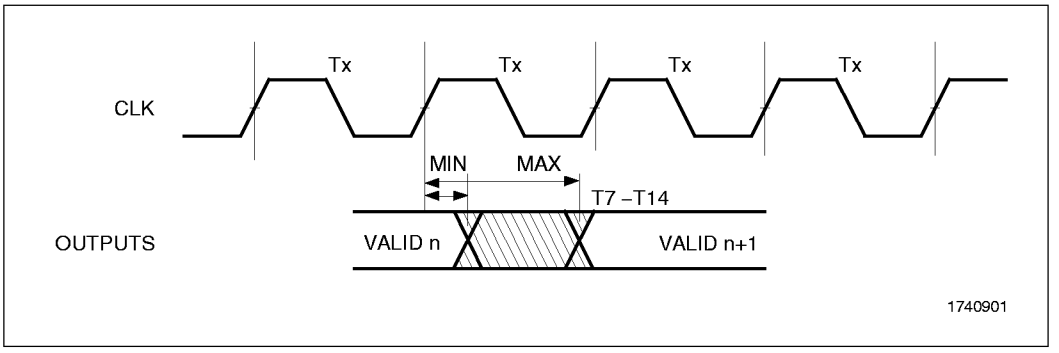


Figure 2–3. Output Valid Delay Timing

Table 2-8. Output Float Delays

C_L = 50 pF, T_{case} = 0°C to 70°C, See Figure 2-5

	PARAMETER	66-MHz BUS		75-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	
T15	A31-A3, ADS#, BE7#-BE0#, BREQ, CACHE#, D/C#, LBA#, LOCK#, M/IO#, PCD, PWT, SCYC, SMIACT#, W/R#		10		10	ns
T16	AP		10		10	ns
T17	D63-D0, DP7-DP0 (Write)		10		10	ns

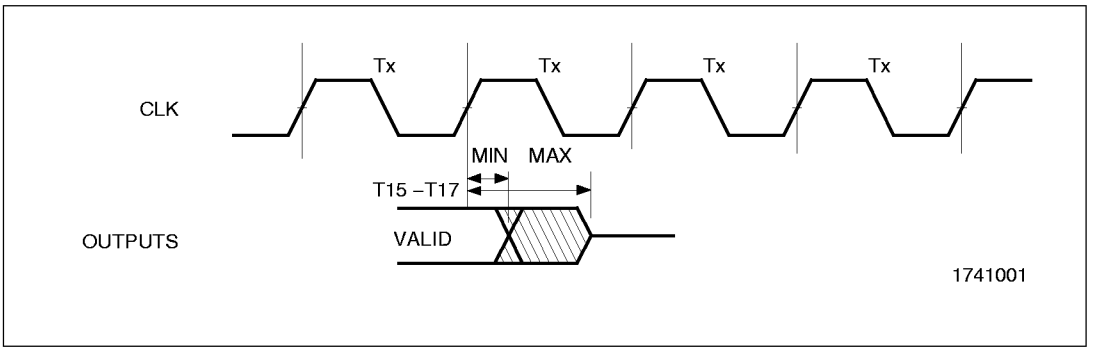


Figure 2-4. Output Float Delay Timing

Table 2–9. Input Setup Times

T_{case} = 0°C to 70°C, See Figure 2–5

	PARAMETER	66–MHz BUS	75–MHz BUS	UNITS
		MIN	MIN	
T18	A20M#, FLUSH#, IGNNE#, SUSP#	5.0	3.3	ns
T19	AHOLD, BHOLD, BOFF#, DHOLD, HOLD	5.0	3.3	ns
T20	BRDY#	5.0	3.3	ns
T21	BRDYC#	5.0	3.3	ns
T22a	A31–A3, BE7#–BE0#	5.0	3.3	ns
T22b	AP	5.0	4.0	ns
T22c	D63–D0 (Read), DP7–DP0 (Read)	3.0	3.0	ns
T23	EADS#, INV	5.0	3.3	ns
T24	INTR, NMI, RESET, SMI#, WM_RST	5.0	3.3	ns
T25	EWBE#, KEN#, NA#, WB/WT#	4.5	3.0	ns
T26	QDUMP#	5.0	3.3	ns

Table 2–10. Input Hold Times

T_{case} = 0°C to 70°C, See Figure 2–5

SYMBOL	PARAMETER	66–MHz BUS	75–MHz BUS	UNITS
		MIN	MIN	
T27	A20M#, FLUSH#, IGNNE#, SUSP#	1.0	1.0	ns
T28	AHOLD, BHOLD, BOFF#, DHOLD, HOLD	1.0	1.0	ns
T29	BRDY#	1.0	1.0	ns
T30	BRDYC#	1.0	1.0	ns
T31a	A31–A3, AP, BE7#–BE0#	1.0	1.0	ns
T31b	D63–D0, DP7–DP0 (Read)	2.0	2.0	ns
T32	EADS#, INV	1.0	1.0	ns
T33	INTR, NMI, RESET, SMI#, WM_RST	1.0	1.0	ns
T34	EWBE#, KEN#, NA#, WB/WT#	1.0	1.0	ns
T35	QDUMP#	1.0	1.0	ns

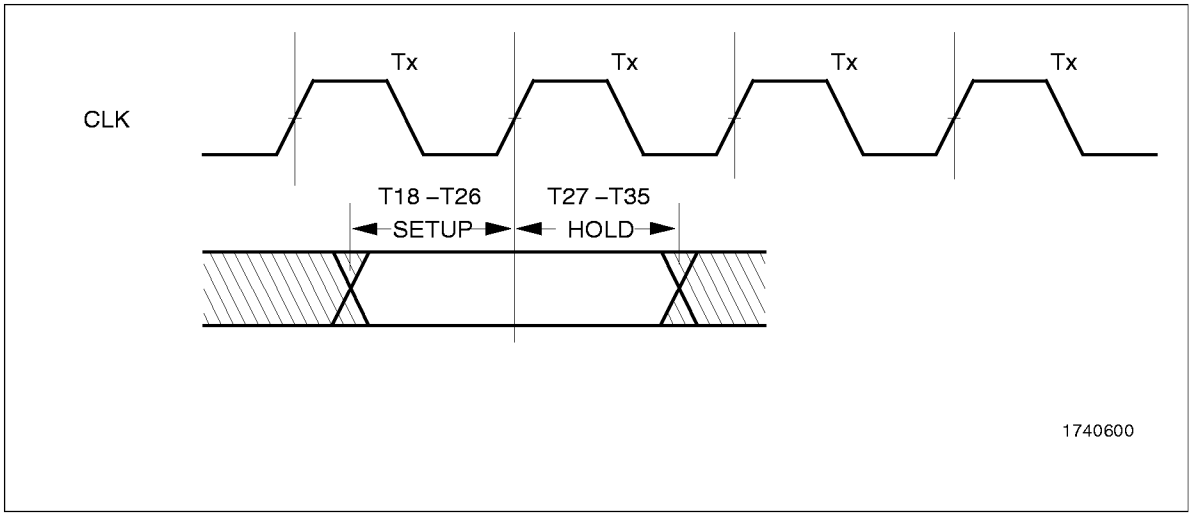


Figure 2–5. Input Setup and Hold Timing

Table 2–11. JTAG AC Specifications

SYMBOL	PARAMETER	ALL BUS FREQUENCIES		UNITS	FIGURE
		MIN	MAX		
	TCK Frequency (MHz)		20	ns	
T36	TCK Period	50		ns	4-6
T37	TCK High Time	25		ns	4-6
T38	TCK Low Time	25		ns	4-6
T39	TCK Rise Time		5	ns	4-6
T40	TCK Fall Time		5	ns	4-6
T41	TDO Valid Delay	3	20	ns	4-7
T42	Non-test Outputs Valid Delay	3	20	ns	4-7
T43	TDO Float Delay		25	ns	4-7
T44	Non-test Outputs Float Delay		25	ns	4-7
T45	TRST# Pulse Width	40		ns	4-8
T46	TDI, TMS Setup Time	20		ns	4-7
T47	Non-test Inputs Setup Time	20		ns	4-7
T48	TDI, TMS Hold Time	13		ns	4-7
T49	Non-test Inputs Hold Time	13		ns	4-7

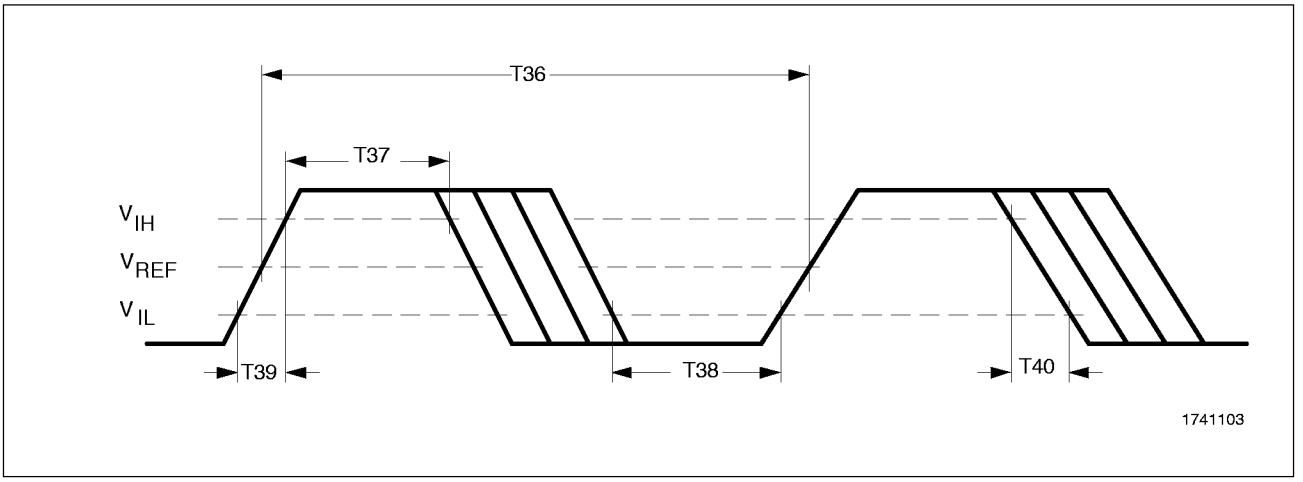


Figure 2–6. TCK Timing and Measurement Points

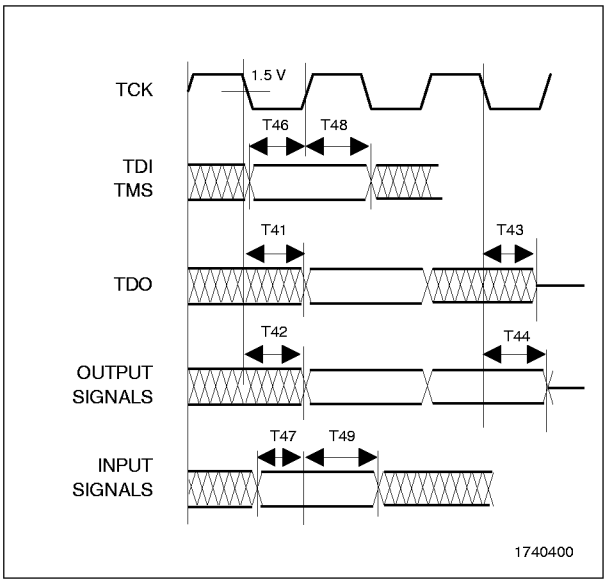


Figure 2–7. JTAG Test Timings

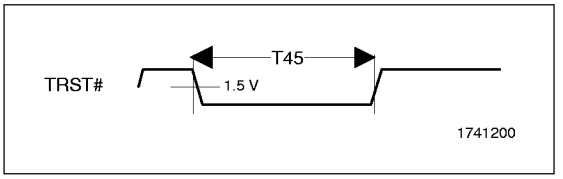


Figure 2–8. Test Reset Timing