CIRRUS LOGIC®

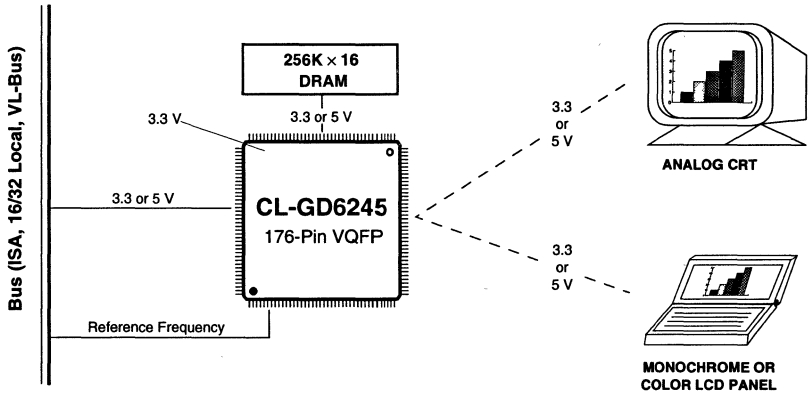
CL-GD6245

Advance Data Book

FEATURES

Single-DRAM LCD/VGA Controller for Monochrome/ Color Notebook Computers

- **Integrated single-chip solution**
  - — Compatible with IBM® VGA hardware
  - — Programmable frequency synthesizer
  - — RAMDAC
  - — Frame accelerator for less power consumption
- **Direct connection to host bus**
  - — 32-bit '486 local bus
  - — VESA® VL-Bus™
  - — 16-bit '386 local bus
  - — ISA bus (PC AT)
- **Supports a variety of 640 × 480 LCDs**
  - — Dual- and single-scan color STN
  - — Dual- and single-scan monochrome STN
  - — 9-, 12-, and 18-bit color TFT
  - — Multi-shade monochrome TFT
- **Simultaneous CRT and LCD operation (SimulSCAN™) in 640 × 480 256-color modes for all supported LCDs, including dual-scan color STN LCDs**
- **Up to 64 shades (at 640 × 480) with monochrome STN and TFT LCDs**
- **CRT resolution up to 1024 × 768 with 16 colors or 800 × 600 with 256 colors**
  - — Maximum 65-MHz video clock at 5.0 V
  - — Maximum 40-MHz video clock at 3.3 V
  - — 132-column text modes
- **Windows® performance-improvement features**
  - — True packed-pixel addressing
  - — Color expansion for 8-bit-per-pixel graphics
  - — 32 × 32 hardware graphics cursor (2 bits per pixel)
  - — Improved data latches for block moves
- **Supports single 256K × 16 DRAM configuration**
  - — Symmetric or asymmetric DRAMs
  - — Dual-WE* or dual-CAS* DRAMs
  - — Self-refresh DRAMs
  - — Maximum 50-MHz memory clock at 5.0 V
  - — Maximum 45-MHz memory clock at 3.3 V
- **Supports 3.3- and 5.0-V mixed-voltage operation**
- **Standby and Suspend modes for reduced power consumption**
- **176-pin (EIAJ standard) VQFP package**
  - — Small form factor
  - — Thin 1.4-mm package



OVERVIEW

The CL-GD6245 is an advanced, single-chip, VGA LCD controller that is optimized for low-cost notebook and subnotebook personal computers with stringent form-factor, display-quality, and power-consumption requirements.

The CL-GD6245 integrates the RAMDAC, frequency synthesizer, color/monochrome STN/TFT LCD interface, LCD power-sequencing logic, host bus interface, and all other functional logic necessary to operate a VGA-compatible video subsystem. This video subsystem is completed with the addition of a single 256K × 16 DRAM. To further minimize board space, the CL GD6245 is packaged in a 176-pin VQFP package, which also features a minimized height for use on boards with two-sided component assembly.

LCD, VGA, or SimulSCAN™

The CL-GD6245 supports 640 × 480 dual-/single-scan color/monochrome STN LCDs and color/monochrome TFT LCDs.

The CL-GD6245 provides up to 64 gray shades or 262,144 (256K) colors on STN LCDs. A state-of-the-art grayscaling algorithm significantly reduces flicker and pattern motion in gray shades with the latest fast-response STN LCDs. The CL-GD6245 provides a 9-, 12-, or 18-bit interface to TFT LCDs. CRTs with resolutions up to 1024 × 768 with 16 colors or 800 × 600 with 256 colors are supported.

The CL-GD6245 provides simultaneous CRT and LCD operation (SimulSCAN™) for single- and dual-scan color and monochrome LCDs, as well as fixed- and multi-frequency analog CRTs. Using a single DRAM for display memory, the CL-GD6245 optimizes the memory and LCD interfaces to provide 640 × 480 256-color SimulSCAN operation on dual-scan color STN LCDs.

Direct Host Bus Connection

The host interface of the CL-GD6245 is designed for use with various CPUs, including direct connection to 32-bit '486 local bus, VESA® VL-Bus™, and ISA bus. Moreover, most popular core-logic chip sets can be directly connected to the CL-GD6245 without additional components. The '486 burst mode for multiple-cycle accesses is also supported to further enhance graphics performance.

High Performance and Low Power

The CL GD6245's integrated frame-accelerator technology enables low-power LCD operation with high LCD vertical-refresh rates. The CL-GD6245 efficiently uses the unused portions of display memory for the frame accelerator so additional DRAMs are not required.

The CL-GD6245 combines high performance with design flexibility in CPU, display-memory interface, and power management. The CL-GD6245 offers true packed-pixel addressing, color expansion for 8-bit-per-pixel graphics, and a hardware graphics cursor, thus improving Windows® performance. Other incorporated features that boost performance include memory-write buffers and internal asynchronous display-data FIFOs.

Each interface on the CL-GD6245 can operate from either a 3.3- or 5.0-V power supply. Mixed-voltage operation is optimized for quick implementation of a notebook computer with reduced power consumption. The display memory, host bus interface, LCD interface, and CRT interface can be independently implemented for either 3.3 or 5.0 V, in any combination.

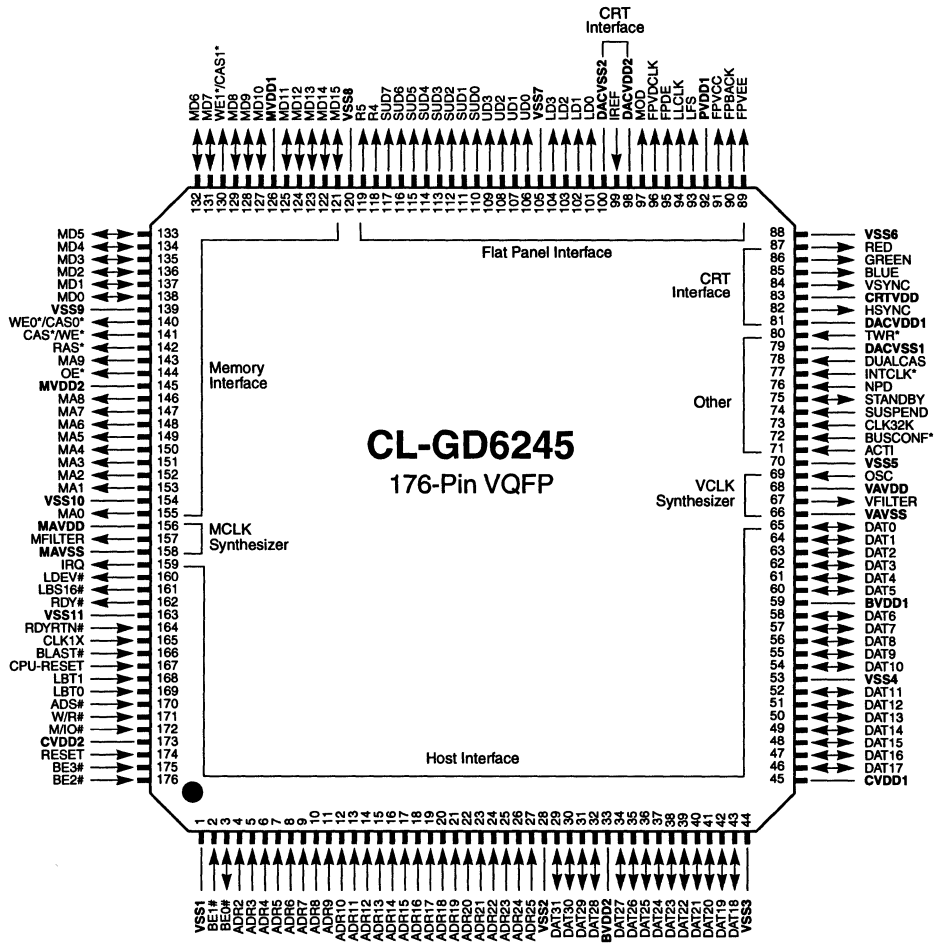
Standby and Suspend power-management modes reduce power consumption when the system is not active. The internal Standby Counter can initiate Standby mode without software intervention. During this reduced-power mode, the LCD is turned off, while the display memory can be accessed and modified. In Suspend mode, all I/O pins, except a dedicated Suspend-mode pin, are deactivated to further reduce power consumption. In this mode, the display-memory data is preserved but cannot be accessed — this feature is useful when a system remains inactive for a relatively long time.

Table of Contents

1. PIN INFORMATION

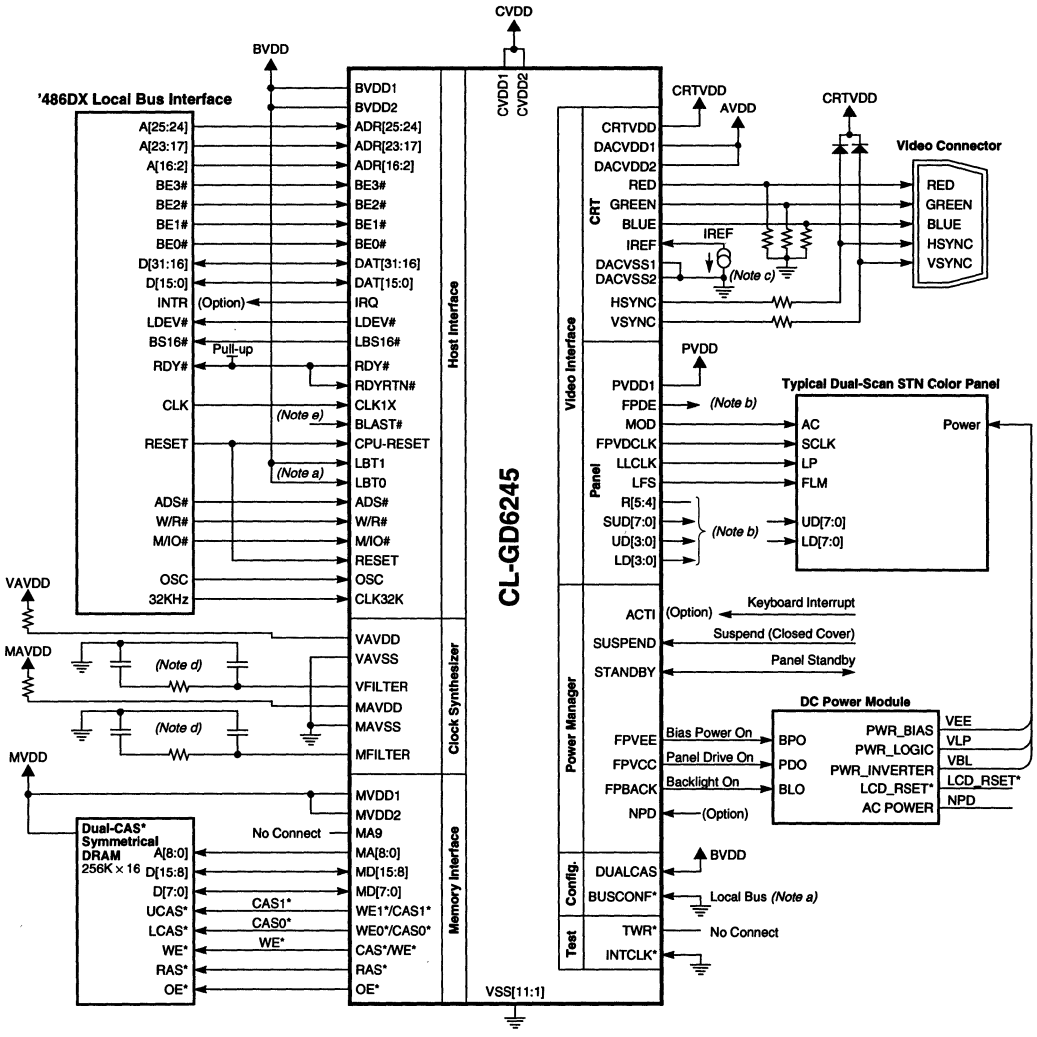
The CL-GD6245 VGA controller is available in a 176-pin very-tight-pitch quad flat pack (VQFP) device configuration, shown below.

1.1 Pin Diagram



NOTE: Power and ground pin names are in bold type.

1.2 Dual-Scan STN Color Panel Connections — '486DX Local Bus Using 256K × 16 DRAM with Dual CAS*



NOTES:

a. Refer to Table 2-1 for bus configuration.

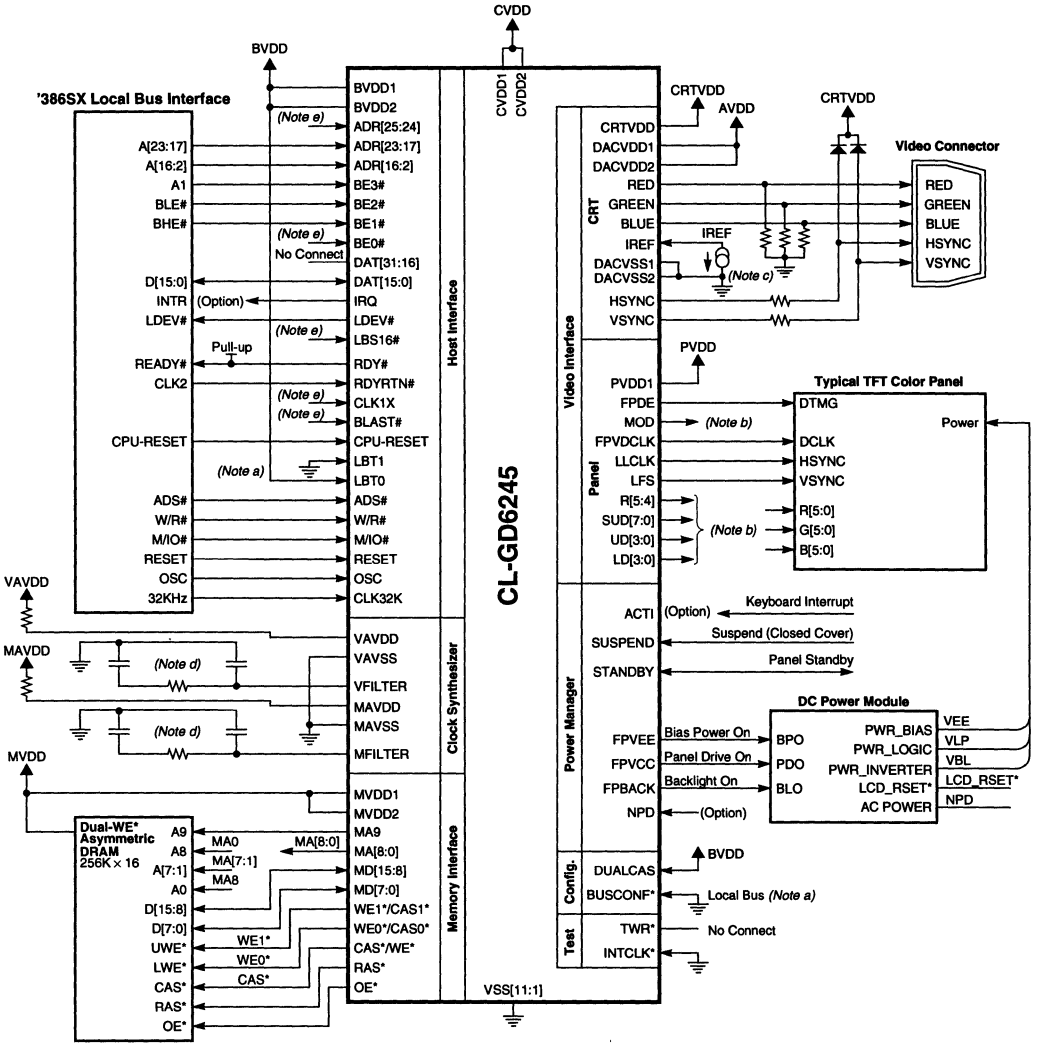
b. See the "Panel Interface Connection Table" in the *CL-GD6245 Application Book* for specific pin connections.

c. See the application note "IREF Current Source for the CL-GD6245" in the *CL-GD6245 Application Book* for details on this circuit.

d. See the application note "CL-GD6245 Analog Voltage Filtering and MFILTER/VFILTER Recommendations" in the *CL-GD6245 Application Book* for details on this circuit.

e. Ground these input signals when not used.

1.3 TFT Color Panel Connections — '386SX Local Bus Using 256K × 16 DRAM with Dual WE*



NOTES:

a. Refer to Table 2-1 for bus configuration.

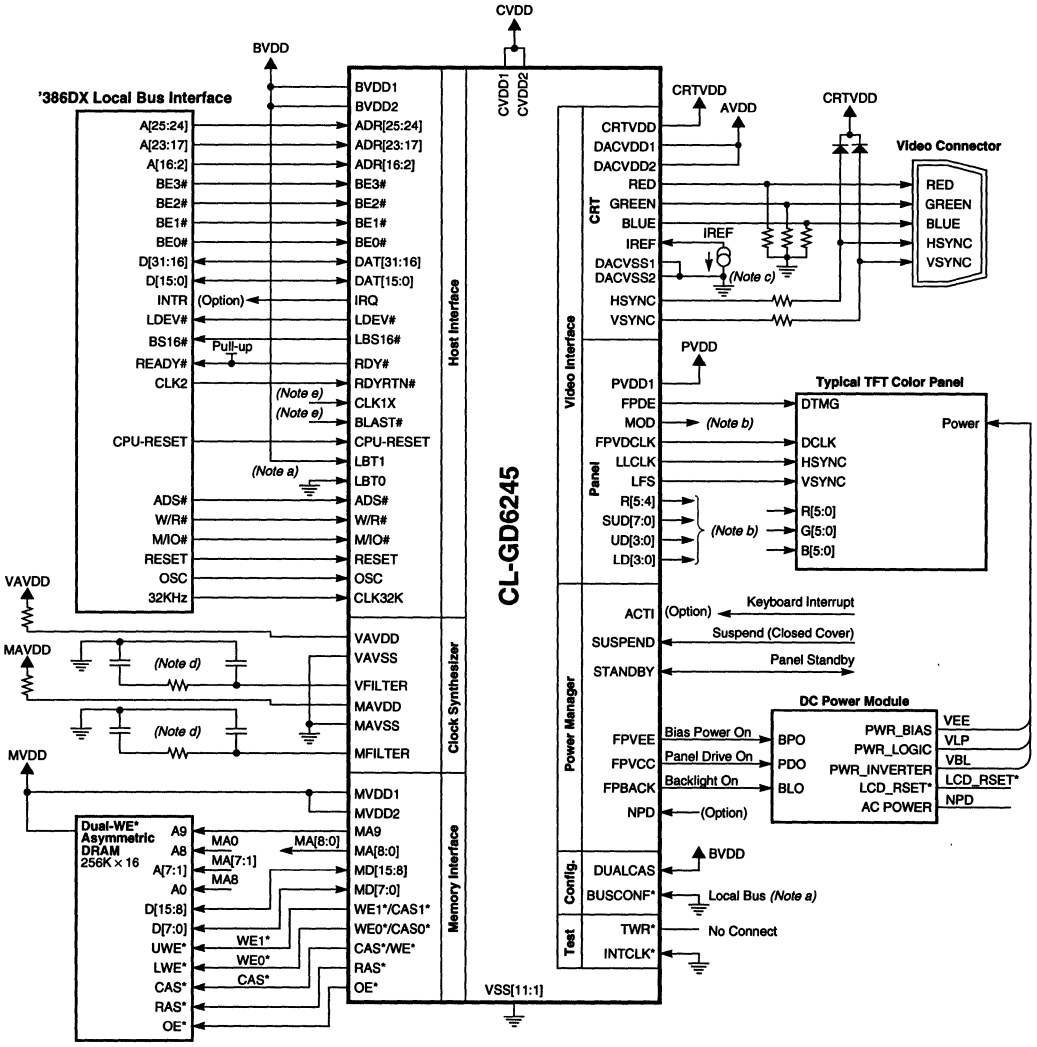
b. See the "Panel Interface Connection Table" in the *CL-GD6245 Application Book* for specific pin connections.

c. See the application note "IREF Current Source for the CL-GD6245" in the *CL-GD6245 Application Book* for details on this circuit.

d. See the application note "CL-GD6245 Analog Voltage Filtering and MFILTER/VFILTER Recommendations" in the *CL-GD6245 Application Book* for details on this circuit.

e. Ground these input signals when not used.

1.4 TFT Color Panel Connections — '386DX Local Bus Using 256K × 16 DRAM with Dual WE*



NOTES:

a. Refer to Table 2-1 for bus configuration.

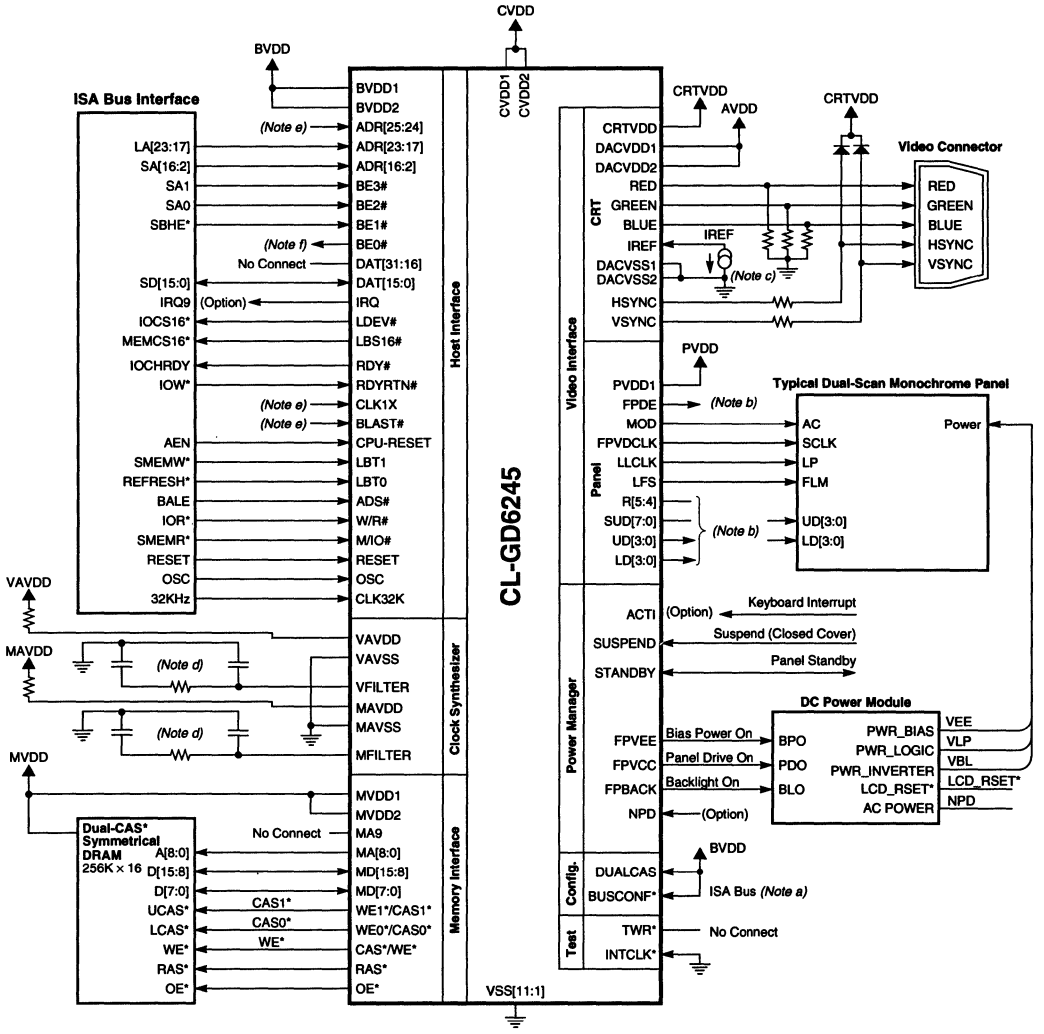
b. See the "Panel Interface Connection Table" in the *CL-GD6245 Application Book* for specific pin connections.

c. See the application note "IREF Current Source for the CL-GD6245" in the *CL-GD6245 Application Book* for details on this circuit.

d. See the application note "CL-GD6245 Analog Voltage Filtering and MFILTER/VFILTER Recommendations" in the *CL-GD6245 Application Book* for details on this circuit.

e. Ground these input signals when not used.

1.5 Typical Dual-Scan Monochrome Panel Connections — ISA Bus Using 256K × 16 DRAM with Dual CAS*



NOTES:

a. Refer to Table 2-1 for bus configuration.

b. See the "Panel Interface Connection Table" in the *CL-GD6245 Application Book* for specific pin connections.

c. See the application note "IREF Current Source for the CL-GD6245" in the *CL-GD6245 Application Book* for details on this circuit.

d. See the application note "CL-GD6245 Analog Voltage Filtering and MFILTER/VFILTER Recommendations" in the *CL-GD6245 Application Book* for details on this circuit.

e. Ground these input signals when not used.

f. BE0# controls the Chip Enable of the optional BIOS EPROMs.

1.6 Pin Summary

These abbreviations are used for pin types in the following sections:

- (I) indicates input pin.
- (O) indicates output pin.
- (I/O) indicates either an input or output pin, depending on the mode.
- (OC) indicates open-collector output pin.
- (3-S) indicates three-state output pin.
- (#) indicates an active-'low' pin for the host local bus, and (*) indicates an active-'low' pin for other interfaces.
- (n/c) indicates no connect.

Table 1-1. Host Interface Pins

CL-GD6245 Pin			ISA Bus	'386SX Local Bus	'386DX Local Bus	'486 Local Bus	VESA® VL-Bus™
Number	Name	Type					
27:26	ADR[25:24]	I	Tie to ground	Tie to ground	A[25:24]	A[25:24]	ADR[25:24]
25:19	ADR[23:17]	I	LA[23:17]	A[23:17]	A[23:17]	A[23:17]	ADR[23:17]
18:4	ADR[16:2]	I	SA[16:2]	A[16:2]	A[16:2]	A[16:2]	ADR[16:2]
175	BE3#	I	SA1	A1	BE3#	BE3#	BE3#
176	BE2#	I	SA0	BLE#	BE2#	BE2#	BE2#
2	BE1#	I	SBHE*	BHE#	BE1#	BE1#	BE1#
3	BE0#	I (O[a])	(Note [a])	Tie to ground	BE0#	BE0#	BE0#
29–32	DAT[31:28]	I/O	n/c	n/c	D[31:28]	D[31:28]	DAT[31:28]
34–43	DAT[27:18]	I/O	n/c	n/c	D[27:18]	D[27:18]	DAT[27:18]
46–47	DAT[17:16]	I/O	n/c	n/c	D[17:16]	D[17:16]	DAT[17:16]
48–52	DAT[15:11]	I/O	SD[15:11]	D[15:11]	D[15:11]	D[15:11]	DAT[15:11]
54–58	DAT[10:6]	I/O	SD[10:6]	D[10:6]	D[10:6]	D[10:6]	DAT[10:6]
60–65	DAT[5:0]	I/O	SD[5:0]	D[5:0]	D[5:0]	D[5:0]	DAT[5:0]
159	IRQ	O	IRQ9 or n/c	INTR or n/c	INTR or n/c	INTR or n/c	IRQ9 or n/c
160	LDEV#	OC	IOCS16*	LDEV#	LDEV#	LDEV#	LDEV#
161	LBS16#	OC	MEMCS16*	Tie to ground	BS16#	BS16#	LBS16#
162	RDY#	3-S	IOCHRDY	READY#	READY#	RDY#	LRDY#
164	RDYRTN#	I	IOW#	CLK2	CLK2	RDY#	RDYRTN#
165	CLK1X	I	Tie to ground	Tie to ground	Tie to ground	CLK	LCLK
166	BLAST#	I	Tie to ground	Tie to ground	Tie to ground	Tie to ground	BLAST#
167	CPU-RESET	I	AEN	CPU-RESET	CPU-RESET	RESET	RESET
168	LBT1	I	SMEMW*	Tie to ground	Tie to BVDD1	Tie to BVDD1	Tie to BVDD1
169	LBT0	I	REFRESH*	Tie to BVDD1	Tie to ground	Tie to BVDD1	Tie to BVDD1
170	ADS#	I	BALE	ADS#	ADS#	ADS#	ADS#
171	W/R#	I	IOR*	W/R#	W/R#	W/R#	W/R#
172	M/IO#	I	SMEMR*	M/IO#	M/IO#	M/IO#	M/IO#
174	RESET	I	RESET	RESET	RESET	RESET	RESET

[a] If an EPROM is used to load the BIOS, the BE0# pin is an active-low output used to control the EPROM Chip Enable.

Table 1-2. CRT Interface Pins

CL-GD6245 Pin			Description
Number	Name	Type	
82	HSYNC	3-S	Horizontal synchronization pulse for monitor
84	VSYNC	3-S	Vertical synchronization pulse for monitor
85	BLUE	Analog Out	Analog current representing Blue value of pixel
86	GREEN	Analog Out	Analog current representing Green value of pixel
87	RED	Analog Out	Analog current representing Red value of pixel
99	IREF	Analog In	DAC current reference — sets full-scale DAC output

Table 1-3. LCD Flat-Panel Interface Pins

CL-GD6245 Pin			Monochrome Panel Pin[a]	STN Color Panel Pin[a]	TFT Color Panel Pin[a]
Number	Name	Type			
119	R5	O	n/c	n/c	R5
118	R4	O	n/c	n/c	R4
117	SUD7	O	n/c	SUD7	R3
116	SUD6	O	n/c	SUD6	R2
115	SUD5	O	n/c	SUD5	G5
114	SUD4	O	n/c	SUD4	G4
113	SUD3	O	n/c	SUD3	G3
112	SUD2	O	n/c	SUD2	B5
111	SUD1	O	n/c	SUD1	B4
110	SUD0	O	n/c	SUD0	B3
109	UD3	O	UD3	SLD7	R1
108	UD2	O	UD2	SLD6	R0
107	UD1	O	UD1	SLD5	G2
106	UD0	O	UD0	SLD4	G1
104	LD3	O	LD3	SLD3	G0
103	LD2	O	LD2	SLD2	B2
102	LD1	O	LD1	SLD1	B1
101	LD0	O	LD0	SLD0	B0
97	MOD	O	MOD	MOD	MOD
96	FPVDCLK	O	FPVDCLK	FPVDCLK	FPVDCLK
95	FPDE	O	FPDE	n/c	FPDE
94	LLCLK	3-S	LLCLK	LLCLK	HSYNC
93	LFS	3-S	LFS	LFS	VSYNC

[a] For exact pin connections, refer to the panel interface connection tables located in the "Panel Interface Guide" section of the *CL-GD6245 Application Book*.

Table 1-4. Display Memory Interface Pins

CL-GD6245 Pin			Dual-WE* DRAM (DUALCAS is 'low')	Dual-CAS* DRAM (DUALCAS is 'high')
Number	Name	Type		
143	MA9	O	MA9[a]	MA9[a]
146	MA8	O	MA8	MA8
147	MA7	O	MA7	MA7
148	MA6	O	MA6	MA6
149	MA5	O	MA5	MA5
150	MA4	O	MA4	MA4
151	MA3	O	MA3	MA3
152	MA2	O	MA2	MA2
153	MA1	O	MA1	MA1
155	MA0	O	MA0[a]	MA0[a]
121	MD15	I/O	MD15	MD15
122	MD14	I/O	MD14	MD14
123	MD13	I/O	MD13	MD13
124	MD12	I/O	MD12	MD12
125	MD11	I/O	MD11	MD11
127	MD10	I/O	MD10	MD10
128	MD9	I/O	MD9	MD9
129	MD8	I/O	MD8	MD8
131	MD7	I/O	MD7	MD7
132	MD6	I/O	MD6	MD6
133	MD5	I/O	MD5	MD5
134	MD4	I/O	MD4	MD4
135	MD3	I/O	MD3	MD3
136	MD2	I/O	MD2	MD2
137	MD1	I/O	MD1	MD1
138	MD0	I/O	MD0	MD0
130	WE1*/CAS1*	O	WE1*	CAS1*
140	WE0*/CAS0*	O	WE0*	CAS0*
141	CAS*/WE*	O	CAS*	WE*
142	RAS*	O	RAS*	RAS*
144	OE*	O	OE*	OE*

[a] MA9 and MA0 are not used to drive column addresses on asymmetrical DRAMs. For a detailed explanation, see the application note "A Single-DRAM LCD Motherboard Solution for Monochrome/Color Notebook Computers" in the *CL-GD6245 Application Book*.

Table 1-5. Miscellaneous Pins

CL-GD6245 Pin			Description
Number	Name	Type	
72	BUSCONF*	I	Bus configuration select (used with LBT0 and LBT1)
77	INTCLK*	I	Internal clock enable
78	DUALCAS	I	Dual-CAS* or dual-WE* DRAM select
80	TWR*	I	Test write enable (used for testing only)

Table 1-6. Power Management Pins

CL-GD6245 Pin			Description
Number	Name	Type	
91	FPVCC	O	Panel power-on enable
90	FPBACK	O	Backlight power-on enable
89	FPVEE	O	Bias power-on enable
76	NPD	I	No power-down (disable power-down timers)
75	STANDBY	I/O	Standby mode control/standby status
74	SUSPEND	I	Suspend mode control (close-cover power sequence)
71	ACTI	I	Activity indicator (reset power-down timers)

Table 1-7. Dual-Frequency Synthesizer Interface Pins

CL-GD6245 Pin			Description
Number	Name	Type	
69	OSC	I	Oscillator input for dual-frequency synthesizer
73	CLK32K	I	Optional 32-kHz clock input for video RAM refresh during Suspend mode
157	MFILTER	Analog Out	Memory clock filter connection
67	VFILTER	Analog Out	Video clock filter connection

Table 1-8. Power and Ground Pins

CL-GD6245 Pin		Connect to Rail	Bypass Capacitor	Video Controller Section Serviced by Power Pins
Number	Name			
59	BVDD1	VDD(VCC)	0.1 µF	Digital voltage for bus interface section
33	BVDD2	VDD(VCC)	0.1 µF	
45	CVDD1	VDD(VCC)	0.1 µF	Digital voltage for core logic of controller
173	CVDD2	VDD(VCC)	0.1 µF	
83	CRTVDD	VDD(VCC)	10 µF	Digital voltage for CRT output pins
81	DACVDD1	VDD(VCC)	10 µF	Analog voltage for palette DAC
98	DACVDD2	VDD(VCC)	10 µF	
156	MAVDD	VDD(VCC) through 33 Ω	10 µF to MAVSS	Analog voltage for memory clock synthesizer
126	MVDD1	VDD(VCC)	0.1 µF	Digital voltage for memory interface section
145	MVDD2	VDD(VCC)	0.1 µF	
92	PVDD1	VDD(VCC)	0.1 µF	Digital voltage for LCD panel interface section
68	VAVDD	VDD(VCC) through 33 Ω	10 µF to VAVSS	Analog voltage for video clock synthesizer
79	DACVSS1	Analog ground		The analog ground plane should be isolated from the VSS (digital) ground plane to prevent noise and crosstalk.
100	DACVSS2	Analog ground		
158	MAVSS	Analog ground		
66	VAVSS	Analog ground		
1	VSS1	Digital ground		
28	VSS2	Digital ground		
44	VSS3	Digital ground		
53	VSS4	Digital ground		
70	VSS5	Digital ground		
88	VSS6	Digital ground		
105	VSS7	Digital ground		
120	VSS8	Digital ground		
139	VSS9	Digital ground		
154	VSS10	Digital ground		
163	VSS11	Digital ground		

2. DETAILED PIN DESCRIPTIONS

These abbreviations are used for pin types in the following sections:

- (I) indicates input pin.
- (O) indicates output pin.
- (I/O) indicates either an input or output pin, depending on the mode.
- (OC) indicates open-collector output pin.
- (3-S) indicates three-state output pin.
- (#) indicates an active-low pin for the host local bus, and (*) indicates an active-low pin for other interfaces.
- Programmable levels '1' and '0' are equivalent to logic levels high and low, respectively.

2.1 Host Interface Pins

The CL-GD6245 can interface directly with the ISA bus, the local buses for the '386SX, '386DX, and '486SX/DX, and the VESA VL-Bus. The bus type is selected with the BUSCONF*, LBT0, and LBT1 pins, as shown in Table 2-1.

Table 2-1. Host-Bus Configurations

Bus Type	BUSCONF* (Pin 72)	LBT0 (Pin 169)	LBT1 (Pin 168)
ISA bus	Tie to BVDD1	Tie to ISA bus REFRESH*	Tie to ISA bus SMEMW*
'386SX	Tie to ground	Tie to BVDD1	Tie to ground
'386DX	Tie to ground	Tie to ground	Tie to BVDD1
'486SX/DX	Tie to ground	Tie to BVDD1	Tie to BVDD1
VL-Bus™	Tie to ground	Tie to BVDD1	Tie to BVDD1

Pin descriptions for the host bus interface is divided into two sections, depending on the setting of the BUSCONF* pin, for either local or ISA bus.

2.1.1 ISA-Bus-Mode Host Interface Pins

Pin Name	ISA Signal Name	Pin No.	Type	Description
BUSCONF*	–	72	I	**BUS CONFIGURATION*:** This active-low pin is used with the LBT0 and LBT1 pins to choose the CL-GD6245 host-bus type. ISA bus configuration is set according to the following table.
ADR[23:17]	LA[23:17]	25:19	I	**ADDRESS [23:17]:** These inputs extend the system address to 24 bits. They are used, along with ADR[16:2], BE3#, and BE2#, to select the resource to be accessed during memory and I/O operations. Data on the ADR[23:17] pins is loaded into the internal address latch while ADS# (BALE) is high, and is stored in the latch during the logic high-to-low transition of ADS# (BALE).
ADR[16:2]	SA[16:2]	18:4	I	**ADDRESS [16:2]:** These inputs are used, along with ADR[23:17], BE3#, and BE2#, to select the resource to be accessed during memory and I/O operations. These address bits are not latched by the CL-GD6245, and therefore *must* remain stable throughout the cycle.
BE3#, BE2#	SA[1:0]	176:175	I	**BYTE ENABLE [3:2]#:** When ISA bus is selected, these bits are used as address inputs, along with ADR[23:17] and ADR[16:2], to select the resource to be accessed during memory and I/O operations. These address bits are not latched by the CL-GD6245, and therefore *must* remain stable throughout the cycle.

Table 2-2. ISA Host-Bus Configuration

Bus Type	BUSCONF* (Pin 72)	LBT0 (Pin 169)	LBT1 (Pin 168)
ISA bus	Tie to BVDD1	Tie to ISA bus REFRESH*	Tie to ISA bus SMEMW*

2.1.1 ISA-Bus-Mode Host Interface Pins *(cont.)*

Pin Name	ISA Signal Name	Pin No.	Type	Description
BE1#	SBHE*	2	I	**BYTE ENABLE 1#:** This active-low input is used, along with BE2#, to determine the width and alignment of a data transfer. BE1# and BE2# are decoded as shown in Table 2-3. In an 8-bit environment, tie BE1# high.
BE0#	EROM*	3	O	**BYTE ENABLE 0#:** When the ISA bus is selected, BE0# is an active-low *output* gated with LBT1 to control the Output Enable pins of up to two 8-bit bus drivers. These drivers are used to connect the data pins of the optional BIOS EPROMs to the system data bus. This output goes active only for memory-read cycles to the address range C000:0–C7FF:F. The BE0# output is forced to high-impedence when RESET is high.
DAT[15:8]	SD[15:8]	48–52, 54–56	I/O	**DATA [15:8]:** These bidirectional pins are used to transfer data during 16-bit memory or I/O operations. These pins can be connected directly to the corresponding ISA bus pins. The DAT[15:8] pins have internal pull-up resistors to guarantee a valid input level when not connected.
DAT[7:0]	SD[7:0]	57–58 60–65	I/O	**DATA [7:0]:** These bidirectional pins are used to transfer data during memory or I/O operations. These pins can be connected directly to the corresponding ISA bus pins.
CPU-RESET	AEN	167	I	**CPU RESET:** When this input is high, it indicates that the current cycle is a DMA cycle. In this case, the CL-GD6245 will not respond to I/O cycles. There is no effect on the memory interface, which still performs refresh cycles.
ADS#	BALE	170	I	**ADDRESS DATA STROBE:** Data on the ADR[23:17] pins is loaded into the internal address latch while ADS# is high. During the logic high-to-low transition of ADS#, the data on the ADR[23:17] pins is stored in the address latch.

Table 2-3. BE1#/BE2# Decoding

BE1#	BE2#	Function
low	low	16-bit transfer
low	high	Upper-byte transfer
high	low	Lower-byte transfer

2.1.1 ISA-Bus-Mode Host Interface Pins *(cont.)*

Pin Name	ISA Signal Name	Pin No.	Type	Description
RDY#	IOCHRDY	162	3-S	**READY#:** This output is high during I/O and BIOS read cycles. During a display-memory *read* cycle, this output is always driven low as soon as M/IO# (SMEMR*) goes low. When the data bits are ready to be placed on the System Data bus, this output goes high. It remains high until M/IO# (SMEMR*) goes high. It then goes high-impedance. During a display-memory *write* cycle, if there is space in the Write Buffer, this output is driven high when LBT1 (SMEMW*) goes low. If the Write Buffer is full when LBT1 (SMEMW*) goes low, LDEV# is driven low and remains low until there is space in the buffer. This output, when low, indicates that additional wait states must be inserted into the current display-memory read or write cycle. Once there is space in the Write Buffer, RDY# goes high, and remains high, until LBT1 (SMEMW*) goes high. It then goes high-impedance.
LDEV#	IOCS16*	160	OC	**LOCAL BUS DEVICE#:** This open-collector output is driven low to indicate the CL-GD6245 can execute a 16-bit I/O operation at the address currently on the bus. This output is generated from a decode of ADR[16:2], BE3#, BE2#, and CPU-RESET (AEN). Table 2-4 shows the range of I/O addresses for which LDEV# will go low. In an 8-bit environment, this pin is not connected.
W/R#	IOR*	171	I	**WRITE/READ#:** This active-low input is forced low by the host to request an I/O data transfer. When the address on ADR[16:2], BE3#, and BE2# is within the range of the CL-GD6245, the CL-GD6245 responds by placing the contents of the appropriate register on the System Data bus.

Table 2-4. LDEV# I/O Addresses

I/O Addresses	Function
3C4, 3C5	Sequencer
3CE, 3CF	Graphics controller
3B4/3D4, 3B5/3D5	CRT controller
3BA/3DA	Input Status register 1

2.1.1 ISA-Bus-Mode Host Interface Pins *(cont.)*

Pin Name	ISA Signal Name	Pin No.	Type	Description
RDYRTN#	IOW*	164	I	**READY RETURN#:** This active-low input is forced low by the host to initiate an I/O data write to the CL-GD6245. When the address on ADR[16:2], BE3#, and BE2# is within the range of the CL-GD6245, the contents of the System Data bus is written into the addressed register during the logic low-to-high transition of RDYRTN#. A list of I/O addresses that the CL-GD6245 responds to appears in Table 2-4. When a 16-bit I/O write is performed, the specified address is typically the Index register for one of the VGA groups. In this case, the index should appear on DAT[7:0], and the data should appear on DAT[15:8].
IRQ	IRQ9	159	3-S	**INTERRUPT REQUEST:** This output is typically unused in an ISA-bus design, but it can be connected to IRQ9 if needed. Register CR11 controls the interrupt function.
LBS16#	MEMCS16*	161	OC	**LOCAL BUS SIZE 16#:** This open-collector output is driven low to indicate that the CL-GD6245 can execute a 16-bit memory operation at the address currently on the bus. Table 2-5 summarizes the conditions for which LBS16# goes low. In an 8-bit environment, this pin is not connected.
LBT0	REFRESH*	169	I	**LOCAL BUS TYPE 0:** When used with the ISA bus, this active-low input is driven low by the host to initiate a DRAM refresh cycle. System memory read operations, occurring when LBT0 is low, are ignored.

Table 2-5. LBS16# Addresses

Resource	Address Bits	Address Range	Qualifier
Display Mode 3	ADR[23:17]	B800:0–BFFF:F	SR8[6] = high (no other VGA card)
Display Mode 7	ADR[23:17]	B000:0–B7FF:F	SR8[6] = high (no other VGA card)
All other display modes	ADR[23:17]	A000:0–BFFF:F	SR8[6] = high (no other VGA card)

2.1.1 ISA-Bus-Mode Host Interface Pins *(cont.)*

Pin Name	ISA Signal Name	Pin No.	Type	Description
RESET	RESET	174	I	**RESET:** This input is used to initialize the CL-GD6245. When high, it forces all outputs to a high-impedance state, and initializes all registers to their reset state. When RESET goes low, normal operation is enabled.
M/IO#	SMEMR*	172	I	**MEMORY I/O#:** This active-low input is forced low by the host to initiate a data transfer (read) from the CL-GD6245 to system memory. When a BIOS read is occurring, which is determined by decoding ADR[23:17], the BE0# output goes low when M/IO# is low.
LBT1	SMEMW*	168	I	**LOCAL BUS TYPE 1:** This active-low input is forced low by the host to initiate a data transfer (write) from system memory to the CL-GD6245. The data bits are stored in the write latch on the logic low-to-high transition of this signal and transferred to display memory later.

2.1.2 Local-Bus-Mode Host Interface Pins

Pin Name	'386/'486 Signal Name	Pin No.	Type	Description
BUSCONF*	–	72	I	**BUS CONFIGURATION*:** This input is used with the LBT0 and LBT1 pins to choose the CL-GD6245 host-bus type. Table 2-6 shows the available local-bus configurations (for ISA-bus configuration see Table 2-2).
LBT1	–	168	I	**LOCAL BUS TYPE:** This input is used in conjunction with LBT0 and BUSCONF* to select the bus type. See Table 2-6.
LBT0	–	169	I	**LOCAL BUS TYPE:** This input is used in conjunction with LBT1 and BUSCONF* to select the bus type. See Table 2-6.
ADR[25:24]	A[25:24]	27:26	I	**ADDRESS [25:24]:** These inputs are used to select the resource to be accessed during memory or I/O operations. For the **'386SX** these pins should be tied to ground.
ADR[23:17]	A[23:17]	25:19	I	**ADDRESS [23:17]:** These inputs are used to select the resource to be accessed during memory or I/O operations.
ADR[16:2]	A[16:2]	18:4	I	**ADDRESS [16:2]:** These inputs are used to select the resource to be accessed during memory or I/O operations.
BE3#	A1/BE3#	175	I	**BYTE ENABLE 3#:** For the **'386SX** this active-low signal is connected directly to the corresponding '386SX byte enable output. For the **'386DX** and the **'486** this active-low input is connected directly to the corresponding CPU byte enable output.

Table 2-6. Local Host-Bus Configurations

Bus Type	BUSCONF* (Pin 72)	LBT0 (Pin 168)	LBT1 (Pin 169)
'386SX	Tie to ground	Tie to BVDD1	Tie to ground
'386DX	Tie to ground	Tie to ground	Tie to BVDD1
'486SX/DX	Tie to ground	Tie to BVDD1	Tie to BVDD1
VL-Bus™	Tie to ground	Tie to BVDD1	Tie to BVDD1

2.1.2 Local-Bus-Mode Host Interface Pins *(cont.)*

Pin Name	'386/'486 Signal Name	Pin No.	Type	Description
BE2#	BLE#/BE2#	176	I	**BYTE ENABLE 2#:** For the **'386SX**, this active-low signal is connected directly to the corresponding '386SX low-byte enable output. For the **'386DX** and the **'486**, this active-low input is connected directly to the corresponding CPU byte-enable output.
BE1#	BHE#/BE1#	2	I	**BYTE ENABLE 1#:** For the **'386SX**, this active-low input is connected directly to the corresponding '386SX high-byte enable output. For the **'386DX** and the **'486**, this active-low input is connected directly to the corresponding CPU byte-enable output.
BE0#	BE0#	3	I	**BYTE ENABLE 0#:** For the **'386DX** and the **'486**, this active-low input is connected directly to the '386DX/'486 BE0# pin. For the **'386SX** this pin is unused and *must* be tied to ground.
DAT[31:16]	D[31:16]	29–32 34–43 46–47	I/O	**DATA [31:16]:** These bidirectional pins are used to transfer data during any memory or I/O operation. In a **'386DX** or **'486** local bus system, these pins are connected directly to D[31:16]. For the **'386SX** these pins are not connected.
DAT[15:0]	D[15:0]	48–52 54–58 60–65	I/O	**DATA [15:0]:** These bidirectional pins are used to transfer data during any memory or I/O operation. These pins are connected directly to D[15:0].
ADS#	ADS#	170	I	**ADDRESS STROBE#:** This active-low input indicates that a new cycle has begun. It *must* be connected directly to the ADS# pin on the CPU.
LBS16#	BS16#	160	OC	**LOCAL BUS SIZE 16#:** This active-low output is used by the **'386DX/'486** local bus. It is driven by the CL-GD6245 to indicate that the current cycle addresses a 16-bit resource. The '386DX/'486 will convert the cycle to an appropriate number of 16-bit transfers. This output is not used in a **'386SX** system.

2.1.2 Local-Bus-Mode Host Interface Pins *(cont.)*

Pin Name	'386/'486 Signal Name	Pin No.	Type	Description
RDYRTN#	CLK2/RDY#	164	I	**READY RETURN#:** When connected to the **'386SX** or **'386DX** local bus, this input is the clock source for the device. For **'486** local bus, this signal must be connected to the RDY# pin of the '486.
CLK1X	CLK	165	I	**CLOCK 1X:** This is the timing reference for the device when it is connected to a **'486** local bus. This pin *must* be connected directly to the CLK pin of the '486. If no CLK is available from the '486, the CLK2 signal can be divided by two and tied to the CL-GD6245 CLK1X pin, but the clock skew must be less than 2 ns. In a **'386** system, this pin is unused and *must* be grounded.
CPU-RESET	CPU-RESET/ RESET	167	I	**CPU-RESET:** A high on this input is used to synchronize the CL-GD6245 to the CPU. In a **'386** system, this pin *must* be connected to the '386 CPU-RESET output to synchronize the CL-GD6245 to CLK2. In a **'486** system, this input is not used, but it must be connected to the '486 RESET pin and CL-GD6245 RESET pin.
IRQ	INTR	159	3-S	**INTERRUPT REQUEST:** This output is typically unused in a local-bus design, but it can be connected to the INTR input if necessary. Register CR11 controls the interrupt function.
LDEV#	LDEV#	160	OC	**LOCAL BUS DEVICE#:** This open-collector output is driven low to indicate that the CL-GD6245 will respond to the current cycle. This signal is generated from a decode of the CPU output signals, A[23:2] and M/IO#. This output will be low before the middle of the first timing (T2) cycle after ADS# goes low.
M/IO#	M/IO#	172	I	**MEMORY I/O:** This input indicates whether a memory or I/O operation is to occur. It *must* be connected directly to the M/IO# pin on the CPU. When M/IO# is high, a memory operation will occur. When M/IO# is low, an I/O operation will occur.

2.1.2 Local-Bus-Mode Host Interface Pins *(cont.)*

Pin Name	'386/'486 Signal Name	Pin No.	Type	Description
RDY#	READY#/ RDY#	162	I or O	**READY#:** For the **'386**, this pin *must* be connected to a pull-up resistor and the READY# pin of the '386. This active-low **input** is used to track bus activity for pipelined cycles. It is used as an **output** to terminate a CL-GD6245 cycle. For the **'486**, this pin *must* be connected to a pull-up resistor and the RDY# pin of the '486. On the '486, this active-low **output** is used to terminate a CL-GD6245 cycle.
RESET	RESET	174	I	**RESET:** This input is used to initialize the CL-GD6245. When high, it forces all outputs to a high-impedance state and initializes all registers to their reset state. When RESET goes low, normal operation is enabled.
W/R#	W/R#	171	I	**WRITE/READ#:** This input indicates whether a write or read operation is selected by the CPU. It *must* be connected directly to the W/R# pin on the CPU. When W/R# is high, a **write** will occur; when WR# is low, a **read** will occur.

2.2 CRT Interface Pins

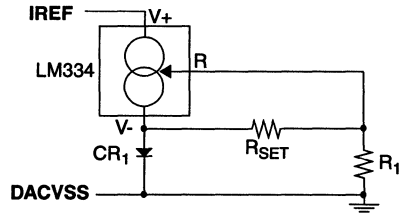
Pin Name	Pin No.	Type	Description
HSYNC	82	3-S	**HORIZONTAL SYNC:** This output supplies the horizontal synchronization pulse to the monitor. The polarity of this output is programmable. This pin can be connected directly to the corresponding pin on the monitor connector.
VSYNC	84	3-S	**VERTICAL SYNC:** This output supplies the vertical synchronization pulse to the monitor. The polarity of this output is programmable. This pin can be connected directly to the corresponding pin on the monitor connector.
BLUE	85	O	**BLUE VIDEO:** This analog output supplies current corresponding to the blue value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, the 6-bit value from the lookup table is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to IREF as follows: $I_{full\text{-}scale} = (63/31) \times IREF$ For more information on determining the value for IREF for a particular system application, refer to the application note "IREF Current Source for the CL-GD6245" in the *CL-GD6245 Application Book*. To maintain IBM VGA-compatibility, each DAC output is typically terminated to monitor ground with a 150-Ω, 2% resistor. This resistor, in parallel with the 75-Ω resistor in the monitor, will yield a 50-Ω impedance to ground. For a full-scale voltage of 700 mV, the full-scale current output should be 14 mA.
GREEN	86	O	**GREEN VIDEO:** This analog output supplies current corresponding to the green value of the pixel being displayed. See the description above of the BLUE pin for information regarding the termination of this pin.
RED	87	O	**RED VIDEO:** This analog output supplies current corresponding to the red value of the pixel being displayed. See the description above of the BLUE pin for information regarding the termination of this pin.

2.2 CRT Interface Pins *(cont.)*

Pin Name	Pin No.	Type	Description
IREF	99	I	**DAC CURRENT REFERENCE:** The current drawn from DACVDD1/DACVDD2 through this pin determines the full-scale output of each DAC. This pin should be connected to a constant-current source. To calculate the IREF current, see the application note "IREF Current Source for the CL-GD6245" in the *CL-GD6245 Applications Book.*

Example:

V_{CC}/V_{DD}	$R_{SET} \pm 1\%$	$R_1 \pm 1\%$	Diode CR_1
5.0 V	20 Ω	200 Ω	1N4148 or equivalent
3.3 V	15 Ω	150 Ω	Schottky diode ($V_{full\text{-}scale}$ < 0.4 volts)



2.3 LCD Flat-Panel Interface Pins

The LCD flat-panel interface is panel and CL-GD6245–controller dependent.

NOTE: Refer to the "Cirrus Logic Flat-Panel Interface Connection Table" in the *CL-GD6245 Applications Book* for specific panel-connection information. Also, see Table 1-3 to cross reference CL-GD6245 pins with panel pins.

2.3.1 General Flat-Panel Interface Pins

Pin Name	Pin No.	Type	Description
MOD	97	O	**MODULATION:** This output provides AC inversion. It should be connected to the appropriate MOD, FR, or DF inputs of the panel. Some panel manufacturers provide this function in the panel circuitry.
FPVDCLK	96	O	**FLAT PANEL VIDEO CLOCK:** This signal is used to drive the flat-panel shift clock. This signal is also named CP2 by some panel manufacturers.
FPDE	95	O	**FLAT PANEL DISPLAY ENABLE:** For those flat panels that require an external display enable, this pin is used to provide a data enable. It is also used as the second shift clock output for STN single-scan, dual-clock color panels.
LLCLK	94	O	**LCD LINE CLOCK:** This output is used to drive the LCD-panel line clock. This signal is also named LP or CP1 by some panel manufacturers.
LFS	93	O	**LCD FRAME START:** This output provides a pulse to start a new frame on flat panels.

2.3.2 Monochrome Flat-Panel Interface Pins

Pin Name	Mono. Signal Name	Pin No.	Type	Description
UD[3:0]	UD[3:0]	109:106	O	**UPPER DATA [3:0]:** The upper data bits [3:0] are typically used with monochrome dual-scan flat panels to provide 4-bit parallel data for the upper portion of the panel.
LD[3:0]	LD[3:0]	104:101	O	**LOWER DATA [3:0]:** The lower data bits [3:0] are typically used with monochrome dual-scan flat panels to provide 4-bit parallel data for the lower portion of the panel.

2.3.3 STN Color Flat-Panel Interface Pins

Pin Name	STN Signal Name	Pin No.	Type	Description
SUD[7:0]	UD[7:0]	117:110	O	**STN UPPER DATA [7:0]:** The upper data bits [7:0] are for use with color STN LCD panels.
UD[3:0], LD[3:0]	LD[7:0]	109:106 104:101	O	**STN LOWER DATA [7:0]:** The lower data bits [7:0] are for use with color STN LCD panels.

2.3.4 TFT Color Flat-Panel Interface Pins

Pin Name	TFT Signal Name	Pin No.	Type	Description
R5, R4, SUD[7:6], UD[3:2]	R[5:0]	119:116 109:108	O	**RED BITS [5:0]:** These bits contain RED color data for TFT color flat panels. Refer to the note at the beginning of this section.
SUD[5:3], UD[1:0], LD3	G[5:0]	115:113 107,106 104	O	**GREEN BITS [5:0]:** These bits contain GREEN color data for TFT color flat panels. Refer to the note at the beginning of this section.
SUD[2:0], LD[2:0]	B[5:0]	112:110 103:101	O	**BLUE BITS [5:0]:** These bits contain BLUE color data for TFT color flat panels. Refer to the note at the beginning of this section.

2.4 Display Memory Interface Pins

Pin Name	Pin No.	Type	Description
DUALCAS	78	I	**DUALCAS:** This input is used to select between a dual-CAS*-type DRAM and a dual-WE*-type DRAM. When DUALCAS = low (dual-WE* DRAMs are selected), pin 130 is defined as WE1*, pin 140 is defined as WE0*, and pin 141 is defined as CAS*. When DUALCAS is high (dual-CAS* DRAMs are selected), pin 130 is defined as CAS1*, pin 140 is defined as CAS0*, and pin 141 is defined as WE*.
MA[9:0]	143, 146:153, 155	O	**MEMORY ADDRESS [9:0]:** These outputs drive the address inputs of the DRAMs, and must be connected to their corresponding address pins. MA0 and MA8 are often swapped to make the interface to symmetric and asymmetric DRAMs consistent. On asymmetrical DRAMs, MA0 and MA9 are used only to drive row addresses (not column addresses). For a detailed explanation, see the CL-GD6245 application note "A Single-DRAM LCD Motherboard Solution for Monochrome/Color Notebook Computers" in the *CL-GD6245 Application Book.*
MD[15:0]	121:125, 127:129, 131:138	I/O	**MEMORY DATA [15:0]:** These pins are used to transfer data between the CL-GD6245 and the display memory. These pins must be connected to the data pins of the DRAMs.
OE*	144	O	**OUTPUT ENABLE*:** This active-low output is used to control the DRAM output enables. For 256K × 4 DRAMs and 256K × 16 DRAMs with dual-write enables, this pin must be connected to the OE* pins of all the DRAMs in the display-memory array.
RAS*	142	O	**ROW ADDRESS STROBE*:** This active-low output is used to latch the row address from MA[9:0] into the DRAMs. This pin must be connected to the RAS* pins of all the DRAMs in the display-memory array.
CAS*/WE*	141	O	**COLUMN ADDRESS STROBE*:** This active-low output is used to latch the column address from MA[9:0] into the DRAMs. When DUALCAS (pin 78) is low (dual-WE* DRAMs are selected), this pin is defined as CAS* and must be connected to the CAS* inputs of the DRAMs. When DUALCAS is high, this pin is defined as WE* and is connected to the WE* inputs of the DRAMs.

2.4 Display Memory Interface Pins *(cont.)*

Pin Name	Pin No.	Type	Description
WE1*/CAS1*	130	O	**WRITE ENABLE 1*:** This active-low output is used to control the WE* or CAS* inputs of the DRAMs, depending on the state of the DUALCAS input. When DUALCAS (pin 78) is low (dual-WE* DRAMs are selected), this pin is defined as WE1* and is connected to the WE1* input of the display-memory array. When DUALCAS is high (dual-CAS* DRAMs are selected), this pin is defined as CAS1* and is connected to the CAS1* input of the display-memory array.
WE0*/CAS0*	140	O	**WRITE ENABLE 0*:** This active-low output is used to control the WE* or CAS* inputs of the DRAMs, depending on the state of the DUALCAS input. When DUALCAS (pin 78) is low (dual-WE* DRAMs are selected), this pin is defined as WE0* and is connected to the WE0* input of the display-memory array. When DUALCAS is high (dual-CAS* DRAMs are selected), this pin is defined as CAS0* and is connected to the CAS0* input of the display-memory array.

2.5 Miscellaneous Pins

Pin Name	Pin No.	Type	Description
INTCLK*	77	I	**INTERNAL CLOCK*:** This input can be set high at Reset, so that externally supplied clocks can be used for testing. This pin should normally be connected to ground for internal voltage-controlled oscillator operations.
TWR*	80	I	**TEST WRITE*:** This active-low input is for factory testing and *must not be connected* to the system for normal operation. It has internal pull-up resistors.

2.6 Power Management Pins

Pin Name	Pin No.	Type	Description
ACTI	71	I	**ACTIVITY:** This pin is an optional activity-sense input. Any logic low-to-high transition on this input can be used, with register masking, to reset the internal power-down timers. When not used, connect ACTI to ground.
FPBACK	90	O	**FLAT PANEL BACKLIGHT:** This output is part of the panel power sequencing. It should be connected to the panel backlight enable.
FPVCC	91	O	**FLAT PANEL VCC:** This output is part of the panel power sequencing. It should be connected to the panel logic power enable.
FPVEE	89	O	**FLAT PANEL VEE:** This output is part of the panel power sequencing. It should be connected to the panel power enable.
NPD	76	I	**NO POWER DOWN:** This input can be used to indicate the presence of AC power. When NPD is high, the internal power-down timers will be stopped and prevented from initiating a panel power-down sequence. When this input goes low, the timers will resume. This pin has an internal pull-down resistor. This pin can be left disconnected if not used.
STANDBY	75	I or O	**STANDBY:** This pin can be programmed to be either an input or an output with register CR20[7]. When programmed as an **input** (CR20[7] = '0') it is the hardware control for the Standby mode. When STANDBY goes high, the power-down sequence that starts the Standby mode is initiated. When programmed as an **output** (CR20[7] = '1') this pin indicates the Standby mode status. When this pin goes high, the CL-GD6245 is in Standby mode.
SUSPEND	74	I	**SUSPEND:** This input is programmable in polarity, by using SR8[3], and is monitored by an internal timer, CR21[3:0], for de-bounce. It can be used to initiate Hardware-Controlled Suspend mode or turn off the flat-panel display. The Hardware-Controlled Suspend mode is the most efficient power-saving mode for the system. The default polarity is active-high.

2.7 Dual-Frequency Synthesizer Interface Pins

Pin Name	Pin No.	Type	Description
CLK32K	73	I	**32-kHz CLOCK:** This input can be connected to an externally supplied 32-kHz clock signal to be used for memory refresh during Suspend mode. If not used, this pin should be tied to ground.
MFILTER	157	O	**MEMORY CLOCK FILTER:** This pin *must* be connected to a π-RC filter, which is returned to MAVSS. The filter components, especially the input capacitor and the resistor, *must* be placed as close as possible to the MFILTER pin.
OSC	69	I	**OSCILLATOR INPUT:** This TTL input pin supplies the reference frequency for the dual-frequency synthesizer. It requires an input frequency of 14.31818 MHz ± 0.01% with a duty cycle of 50% ± 10%. This input can be supplied from the appropriate pin on the ISA bus, or from an oscillator.
VFILTER	67	O	**VIDEO CLOCK FILTER:** This pin *must* be connected to a π-RC filter, which is returned to VAVSS. The filter components, especially the input capacitor and the resistor, *must* be placed as close as possible to the VFILTER pin.

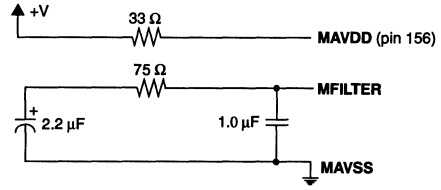


Figure 2-1. Typical Memory-Clock Filter

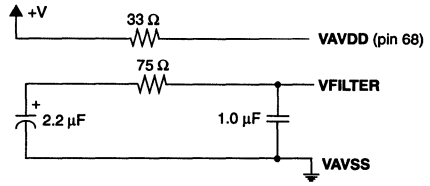


Figure 2-2. Typical Video-Clock Filter

2.8 Power and Ground Pins

Pin Name	Pin No.	Type	Description
BVDD1 BVDD2	59 33	Power	**BUS VDD:** These two pins are used to supply +3.3 or +5.0 V to the bus interface pin group of the CL-GD6245. Both pins *must* be connected to the same voltage. Each pin *must* be connected directly to the VCC rail. Each pin *must* be bypassed with a 0.1-µF capacitor with proper high-frequency characteristics, as close to the pin as possible. When a multi-layer board is used, connect each BVDD pin to the power plane.
CVDD1 CVDD2	45 173	Power	**CORE VDD:** These two pins are used to supply +3.3 or +5.0 V to the internal core logic of the CL-GD6245. Each pin *must* be connected directly to the VCC rail. Each pin *must* be bypassed with a 0.1-µF capacitor with proper high-frequency characteristics, as close to the pin as possible. When a multi-layer board is used, connect each CVDD pin to the power plane.
CRTVDD	83	Power	**CRT VDD:** This pin is used to supply +3.3 or +5.0 V to the CRT interface pin group of the CL-GD6245. This pin *must* be connected directly to the VCC rail. This pin *must* be bypassed with a 0.1-µF capacitor with proper high-frequency characteristics, as close to the pin as possible. When a multi-layer board is used, connect this CRTVDD pin to the power plane.
DACVDD1 DACVDD2	81 98	Power	**DAC ANALOG VDD:** These two pins are used to supply +3.3 or +5.0 V to the palette DAC of the CL-GD6245. Both pins *must* be connected to the same voltage as CVDD. Each pin *must* be connected directly to the VCC rail and bypassed with 0.1-µF and 10-µF capacitors, with proper high-frequency characteristics, placed as close to the pin as possible. When a multi-layer board is used, connect each DACVDD pin to the power plane.
MAVDD	156	Power	**MCLK ANALOG VDD:** This pin is used to supply +3.3 or +5.0 V to the memory clock synthesizer of the CL-GD6245. The same voltage as CVDD *must* be used. This pin *must* be connected to the VCC rail via a 33-Ω resistor and bypassed to MAVSS with 0.1-µF and 10-µF capacitors.

2.8 Power and Ground Pins *(cont.)*

Pin Name	Pin No.	Type	Description
MVDD1 MVDD2	126 145	Power	**MEMORY VDD:** These two pins are used to supply +3.3 or +5.0 V to the internal DRAM interface pin group of the CL-GD6245. Each pin *must* be connected directly to the VCC rail. Each pin *must* be bypassed with a 0.1-µF capacitor with proper high-frequency characteristics, as close to the pin as possible. When a multi-layer board is used, connect each MVDD pin to the power plane.
PVDD1	92	Power	**PANEL VDD:** This pin is used to supply +3.3 or +5.0 V to the LCD flat-panel interface pin group of the CL-GD6245. This pin *must* be connected directly to the VCC rail. This pin *must* be bypassed with a 0.1-µF capacitor with proper high-frequency characteristics, as close to the pin as possible. When a multi-layer board is used, connect this PVDD pin to the power plane.
VAVDD	68	Power	**VCLK ANALOG VDD:** This pin is used to supply +3.3 or +5.0 V to the video clock synthesizer of the CL-GD6245. The same voltage as CVDD *must* be used. This pin *must* be connected to the VCC rail via a 33-Ω resistor and bypassed to VAVSS with 0.1-µF and 10-µF capacitors.
DACVSS1 DACVSS2	79 100	Ground	**DAC ANALOG VSS:** These two pins are used to supply ground reference to the palette DAC of the CL-GD6245. Each pin *must* be connected to the analog ground rail, which should be isolated from VSS (digital) ground.
MAVSS	158	Ground	**MCLK ANALOG VSS:** This pin is used to supply ground reference to the memory clock synthesizer of the CL-GD6245. This pin *must* be connected to the analog ground rail, which should be isolated from VSS (digital) ground.
VAVSS	66	Ground	**VCLK ANALOG VSS:** This pin is used to supply ground reference to the video clock synthesizer of the CL-GD6245. This pin *must* be connected to the analog ground rail, which should be isolated from VSS (digital) ground.
VSS1–VSS11	1,28,44 53,70,88 105,120 139,154 163	Ground	**VSS (Digital Ground):** These 11 pins are used to supply ground reference for the core logic and pin groups of the CL-GD6245. Each pin *must* be connected directly to the ground rail. When a multi-layer board is used, each VSS pin *must* be connected to the ground plane.

3. FUNCTIONAL DESCRIPTION

This section provides functional information and design guidelines on chip resources and interfaces of the CL-GD6245 VGA controller.

3.1 General

The CL-GD6245 VGA controller is a complete solution for LCD VGA subsystems. All necessary hardware for CPU updates to memory, screen refresh, and DRAM refresh is included in the CL-GD6245. A VGA motherboard solution can be implemented with only one 256K × 16 DRAM.

3.2 Functional Blocks

The following functional blocks have been integrated into the CL-GD6245:

3.2.1 CPU Interface

The CL-GD6245 connects directly to the ISA bus, VESA VL-Bus, or '386 and '486 local bus. No additional logic circuitry is required. The CL-GD6245 internally decodes a 16- or 24-bit address and responds to the applicable control lines. It executes both I/O and memory accesses as either an 8- or 16-bit device.

CPU Write Buffer

The CPU write buffer has a queue of CPU write accesses to display memory that have not been executed because of memory arbitration. Maintaining this queue allows the CL-GD6245 to release the CPU as soon as it records the address and data and then to execute the operation when display memory is available, thus increasing CPU performance.

3.2.2 Graphics Controller

The graphics controller is located between the CPU interface and the memory sequencer. It performs text manipulation, data rotation, color mapping, and other miscellaneous operations.

3.2.3 Display-Memory Interface

The display-memory interface consists of the memory arbitrator and the display-memory sequencer.

3.2.3.1 Display-Memory Arbitrator

The display-memory arbitrator allocates bandwidth to the three functions that compete for the limited bandwidth of display memory. These competing functions are CPU access, DRAM (display memory) refresh, and screen refresh. DRAM refresh is handled transparently by allocating a selectable number of CAS*-before-RAS* refresh cycles at the beginning of each scanline. Screen refresh and CPU access are allocated cycles according to the video FIFO-control parameters, with priority given to screen refresh.

3.2.3.2 Display-Memory Sequencer

The display-memory sequencer generates timing for display memory. This includes RAS*, CAS*, and multiplexed-address timing, as well as WE* and OE* timing. The memory sequencer generates CAS*-before-RAS* refresh cycles, random-read and random-early-write cycles, and Fast-Page mode read and early-write cycles. The display-memory sequencer generates multiple CAS* or WE* signals according to the memory type used.

3.2.4 Graphics Interface

The graphics interface consists of the CRT controller, LCD flat-panel controller, video FIFO, attribute controller, and palette DAC.

3.2.4.1 CRT Controller

The CRT controller generates the HSYNC and VSYNC signals required for the CRT monitor, as well as BLANK* signals required by the palette DAC.

3.2.4.2 LCD Flat-Panel Controller

The LCD flat-panel controller drives single-scan and dual-scan color STN and active-matrix color TFT panels. It also drives monochrome panels with multiple gray-shading options. Additionally, it provides all the power-sequencing controls needed by the panels.

3.2.4.3 Video FIFO

The video FIFO allows the memory sequencer to execute the display-memory accesses needed for screen refresh at the maximum memory speed rather than at the screen refresh rate. This makes it possible to collect the accesses for screen refresh near the beginning of the scanline, and thus to execute them in Fast-Page mode rather than Random-Read mode.

3.2.4.4 Attribute Controller

The attribute controller consists of the registers that format the display for the screen. Display color selection, text blinking, and underlining are performed by the attribute controller.

3.2.4.5 Palette DAC

The palette DAC contains the color palette and three 6-bit digital-to-analog converters. The color palette, with 256 18-bit entries, converts a color code that specifies the color of a pixel into three 6-bit values — one each for red, green, and blue.

3.2.5 Dual-Frequency Clock Synthesizer

The internal dual-frequency clock synthesizer generates the memory sequencer clock and the video-display clock from a single reference frequency. The frequency of each clock is programmable. The reference frequency can be generated with an internal crystal-controlled oscillator. Alternatively, it can be supplied from an external source.

3.3 Functional Operation

The four major operations controlled by the CL-GD6245 are discussed below.

3.3.1 CPU Access to Registers

The host CPU can be any processor controlling an ISA, VESA VL-Bus, or '386/'486 local bus. It accesses CL-GD6245 registers by setting up a 16- or 24-bit address and forcing IOR* or IOW* low. The CL-GD6245 responds either as an 8- or 16-bit peripheral, depending on the system configuration and the host bus interface.

CPU register access does not affect DRAM or screen refresh, which can occur concurrently with CPU access, unless the host is changing display parameters or has suppressed refresh.

3.3.2 CPU Access to Display Memory

All CPU host accesses to display memory are controlled by the CL-GD6245. The host first sets up parameters, such as color and write masks, and then generates a memory access in the programmed response range of the CL-GD6245.

3.3.3 Display-Memory Refresh

During each horizontal timing period, the CL-GD6245 automatically generates a selectable number of CAS*-before-RAS* refresh cycles.

3.3.4 Screen Refresh

The CRT monitor requires near-constant rewriting (refresh) since the only memory is the phosphor persistence of the screen. Phosphor persistence is typically only a few milliseconds. The CL-GD6245 fetches information from the display memory for each scanline as quickly as possible, using Fast-Page-mode cycles to fill the video FIFO. This allows the maximum possible time for the host to access the display memory.

3.4 Performance

The CL-GD6245 offers the following performance-enhancing features:

- 16-bit CPU interface to I/O registers for faster host access
- 16-bit CPU interface to display memory for faster host access in all modes, including Planar
- DRAM Fast-Page-mode operations for faster access to display memory
- CPU write buffer to accelerate CPU access for display writes
- Video FIFO minimizes memory contention
- 32 × 32 hardware cursor to improve Microsoft® Windows® performance
- Increased throughput with direct connection to 32-bit '386 and '486 local-bus interfaces

3.5 Compatibility

The CL-GD6245 includes all registers and data paths required for VGA controllers.

The CL-GD6245 supports extensions to VGA, including 1024 × 768 × 16 non-interlaced modes. Additionally, various 132-column text modes are supported.

The CL-GD6245 has programmable input threshold levels that support TTL or CMOS logic inputs (see register SR16[1:0]).

3.6 Bus Interface

The CL-GD6245 directly connects to a number of buses, including the data bus of 32-bit processors such as the '486.

3.6.1 '486 Burst Mode Support

The CL-GD6245 can request and respond to burst cycles for accesses that require more than a single cycle. By supporting '486 burst transfers, the CL-GD6245 delivers higher performance. During a CPU 32-bit write when LBS16# is low, a non-burstable CL-GD6245 signal would normally require two cycles to complete the transfer. The second cycle of a multiple transfer following the first cycle requires an additional clock to produce ADS# (T1 timing). In contrast, burst cycles eliminate the need for this additional clock. As a result of burst-mode support for 32-bit writes, one CPU clock is saved.

3.6.2 Address Decoding and Latching

The CL-GD6245 responds to cycles after decoding addresses A[25:2] and status line M/IO#. The CL-GD6245 indicates to the rest of the system that it owns the cycle by asserting LDEV# (LBA# by some naming conventions). Other devices should not respond when LDEV# goes low before the middle of the first T2 timing cycle. For the 32-bit address bus of the '386DX and '486 processors, the address lines ADR[25:24] must be externally decoded and a active-low signal (for a valid CL-GD6245 cycle) should be supplied to the ADR23 (upper address) input of the CL-GD6245. This decode must be performed in the minimum possible time (less than 10 ns is recommended).

Since the CL-GD6245 does not decode status line D/C#, it does not respond to special and interrupt acknowledge cycles. The address produced by the CPU during these cycles lies outside the memory and I/O range of the CL-GD6245. The CL-GD6245 will not respond to I/O locations 0002h-0005h because responding would cause an inappropriate reaction to certain special cycles.

Because AHOLD of the '486 may go high in the middle of a cycle, the CL-GD6245 latches the address at the end of the T1 timing cycle. The address latch allows the local bus address to change during an address-hold response without affecting the CL-GD6245 address decode for the current cycle.

3.6.3 Bus Cycle Restart

The CL-GD6245 does not support '486 bus restart cycles. Since the CL-GD6245 does not receive BOFF#, it does not sense bus cycle restarts and cannot respond appropriately.

3.6.4 Other Bus Considerations

- **For a '386SX:** CPU-RESET is used with CLK2 to generate an internal synchronous 1x system clock. The '386SX output signal NA# (for pipelined cycles) is not an input to the CL-GD6245, but the controller automatically detects and responds to system-initiated pipelined cycles.
- **For a '386DX:** CPU-RESET is used with CLK2 to generate an internal synchronous 1x system clock. LBS16# is always set low for CL-GD6245 bus cycles. Pipelined cycles are not supported for '386DX.
- **For a '486:** LBS16# is always set low for CL-GD6245 bus cycles.

The RDY# line for local bus support is normally 'off' (high-impedance). As a result, a system pull-up resistor is needed. When the CL-GD6245 decodes a valid address, the RDY# line remains 'off' until it can be driven active-low for one clock period to end the bus cycle. RDY# is then driven high for about 5 ns before returning to 'off'. For memory-read cycles, the RDY# output does not go low until the read data is valid. Memory-write cycles are performed in the minimum time possible, as long as the system write buffer is not full. I/O read and write cycles (except DAC) have a RDY# delay of four CPU clock periods for data cycle requirements. All I/O to the internal video DAC have a RDY# delay of four VCLK periods to meet the DAC minimum cycle-time requirements.

The local bus is always 16-bit. All registers are compatible with 16-bit bus cycles. They use D[7:0] for even-byte addresses and D[15:8] for odd-byte addresses. RDY# goes low for any I/O read or write to any decoded address in the CL-GD6245 I/O address range (even the unused addresses). The unused locations at decoded CL-GD6245 I/O addresses will always be read as 00h and will ignore any write data.

3.7 LCD Flat-Panel Interface

The CL-GD6245 directly interfaces with a variety of LCDs, including the following:

- Monochrome 640 × 480 dual- and single-scan STN LCDs with SimulSCAN.
- Color 640 × 480 dual- and single-scan STN LCDs (with 8- and 16-bit interfaces) with SimulSCAN.
- Color 640 × 480 TFT LCDs with SimulSCAN and the following interfaces:
  - — 9-bit (3 bits each for red, green, and blue)
  - — 12-bit (4 bits each for red, green, and blue)
  - — 18-bit (6 bits each for red, green, and blue)

3.7.1 LCD Resolution Compensation for 640 × 480 LCDs

The CL-GD6245 allows a full spectrum of PC applications written for analog CRT monitors (using various VGA modes) to run transparently on LCDs. Unlike CRTs, LCDs have a fixed horizontal and vertical resolution. When VGA modes that use a resolution lower than the fixed resolution of the LCD are selected, a section of the LCD screen is left blank. For example, if VGA text mode 3 (which has a vertical resolution of 400 lines) is displayed without enhancement on a 640 × 480 LCD, 80 blank lines remain at the bottom of the LCD. (Refer to Table 4-1 for a listing of the horizontal and vertical resolutions of the standard VGA modes.)

The CL-GD6245 provides the following three LCD resolution compensation options to display lower-resolution VGA text and graphics modes on a 640 × 480 LCD:

- **Automatic Text Expansion:** This makes the font consistent across the LCD and eliminates any breaks or artifacts in fonts that connect to adjacent fonts. Fonts that are 9 pixels wide (used in the popular VGA text modes 3 and 7) are horizontally displayed as 8 pixels so that 80 characters fill all 640 pixels of the LCD. Fonts that are 8 × 8 (200-line) are double-scanned and an extra top line and two extra bottom lines are added to each character row to vertically expand the font to 19 lines to fill 475 lines on the LCD. For fonts that are 8 × 14 (350-line), two extra top lines and three extra bottom lines are added to each character row to vertically expand the font to 19 lines to fill 475 lines on the LCD. For fonts that are 8 × 16 (400-line), one extra top line and two extra bottom lines are added to each character row to vertically expand the font to 19 lines to fill 475 lines on the LCD.
- **Automatic Vertical Graphics Expansion:** This allows application programs that use lower-resolution VGA graphics modes to automatically run on a 640 × 480 LCD. Graphics modes of 200 lines are vertically expanded to 475 lines by expanding every 8 lines to 19 lines using a pattern of 2,2,3,2,2,3,2,3 (double- and triple-scan). Graphics modes of 350 lines are vertically expanded to 475 lines by expanding every 14 lines to 19 lines using a pattern of 1,1,2,1,1,2,1,2,1,1,2,1,1,2 (single- and double-scan). Note that popular GUI-based applications, such as Windows® or OS/2®, use a CL-GD6245 driver that selects the proper VGA graphics mode (such as 640 × 480 with 2-, 16-, or 256-color modes) to run the application programs at the full 640 × 480 resolution of the LCD.
- **Automatic Vertical Centering:** The 475 lines resulting from automatic text and graphics expansion can be vertically centered on the 480 line LCD. If automatic expansion is not used, the 200-, 350-, or 400-line text or graphics modes can also be vertically centered on the 480-line LCD.

3.7.2 Frame Rate Modulation

The CL-GD6245 uses an improved FRM (frame rate modulation) algorithm to create grayscales on monochrome and color STN LCDs. The FRM algorithm modulates the 'on' and 'off' times of individual pixels on the LCD over time in such a way that the eye integrates the superimposed pixels as grayscales. Proprietary techniques reduce or eliminate the grayscale artifacts (such as flicker, noise, and pattern motion) to provide outstanding display quality on state-of-the-art STN LCDs with fast response times (~100 ms).

The CL-GD6245 provides the following three FRM options:

- **16-Frame FRM:** This modulates the pixel over 16 frames in time to create 16 shades per primary color — RGB (red, green, and blue) — for a total of 4,096 (16^3) colors. This option is intended to support STN LCDs currently available and in development, including STN LCDs with very fast response times (~100 ms). This algorithm allows undesirable grayscales — those that flicker or have pattern motion — to be

masked out. Grayscales 7 and 9 can be converted to grayscales 6 and 8, respectively, by setting RBX[4]. Grayscales 5 and 11 can be converted to grayscales 4 and 10, respectively, by setting RBX[3]. If two grayscales are masked out, the FRM algorithm produces 2,744 (14^3) colors. If four grayscales are masked out, the FRM algorithm produces 1,728 (12^3) colors.

- **8-Frame FRM:** This modulates the pixel over 8 frames in time to create 8 grayscales per primary color (RGB) for a total of 512 (8^3) colors. This option is intended to support future STN LCDs that may have response times that are too fast for the 16-frame FRM option.
- **4-Frame FRM:** This modulates the pixel over 4 frames in time to create 4 grayscales per primary color (RGB) for a total of 64 (4^3) colors. This option is intended to support future STN LCDs that may have response times that are too fast for the 8- and 16-frame FRM options.

In summary, the FRM algorithm produces 2, 3, or 4 bits of color depth for each primary color (RGB) on STN LCDs. In addition, the CL-GD6245 dithering engine can be used with the FRM algorithm to add up to 4 bits of color depth to each primary color. A total of 6 bits per primary color (or 64 grayscales each for RGB) can be produced for a total of 256K colors, even when only a 4-frame FRM algorithm is used.

3.7.3 Dithering Engine

The CL-GD6245 dithering engine increases the number of perceived colors displayed on the LCD. A proprietary intercalating spatial dithering technique preserves the spatial resolution of the displayed image. For example, when a 640 × 480 resolution image is dithered, the 640 × 480 resolution is maintained on the display, rather than being reduced to 320 × 240.

The dithering engine can increase the number of displayed colors relative to what the display can physically produce without dithering. The dithering engine automatically selects one of the dithering patterns shown in Table 3-1 to increase the number of displayed bits per primary color (RGB) depending on the color depth of the image.

This very flexible dithering engine can add 2, 3, or 4 bits per primary color and can be used on color and monochrome STN LCDs and TFT LCDs. Dithering is programed by register CR9X[3:2]. Table 3-1 shows the effective increase in numbers of bits of shading per primary color available.

Table 3-1. Effective Dithering Patterns

Effective Dithering Pattern	Increased Number of Displayed Bits per Primary Color
2 × 1	1 bit
2 × 2	2 bits
2 × 4	3 bits
4 × 4	4 bits

Table 3-3 shows the number of displayed grayscales on a monochrome STN LCD with various FRM and dithering options. The 4-frame FRM option produces only 4 grayscales (2 bits/pixel), which is insufficient for displaying 32- or 64-grayscale images. The various dithering options can add up to 4 bits/pixel, depending on the color depth of the displayed image. To display a 32-grayscale image (5 bits), the dithering engine adds 3 bits to the 2 bits produced by FRM. To display a 64-grayscale image (6 bits), the dithering engine adds 4 bits to the 2 bits produced by FRM.

Table 3-2. Number of Grayscales on Monochrome STN LCDs

Frame Rate Modulation	Effective Dithering Pattern	Image	
		32 Grayscales (5 bits)	64 Grayscales (6 bits)
4 frames (2 bits)	None	4 (2^2)	
	2 × 1 (1 bit)	8 (2^3)	
	2 × 2 (2 bits)	16 (2^4)	
	2 × 4 (3 bits)	32 (2^5)	
	4 × 4 (4 bits)	32 (2^5)	64 (2^6)
8 frames (3 bits)	None	8 (2^3)	
	2 × 1 (1 bit)	16 (2^4)	
	2 × 2 (2 bits)	32 (2^5)	
	2 × 4 (3 bits)	32 (2^5)	64 (2^6)
16 frames (4 bits)	None	16 (2^4)	
	2 × 1 (1 bit)	32 (2^5)	
	2 × 2 (2 bits)	32 (2^5)	64 (2^6)

Table 3-3 shows the number of displayed colors on a color STN LCD with various FRM and dithering options. Each FRM/dithering option produces the same number of color shades per primary color (shown in Table 3-3) as grayscales for monochrome LCDs shown in Table 3-3. Note that total number of colors is equal to three times the number of colors per primary color (RGB). for example, a 4-frame FRM and a 4 × 4 dithering pattern produces 64 grayscales on monochrome STN LCDs and 256K colors on color STN LCDs.

Table 3-3. Number of Colors on Color STN LCDs

Per Primary Color (RGB)		Image	
Frame Rate Modulation	Effective Dithering Pattern	32K Colors (15 bits)	256K Colors (18 bits)
4 frames (2 bits)	None	64 (2^6)	
	2 × 2 (2 bits)	4K (2^{12})	
	2 × 4 (3 bits)	32K (2^{15})	
	4 × 4 (4 bits)	32K (2^{15})	256K (2^{18})
8 frames (3 bits)	None	512 (2^9)	
	2 × 2 (2 bits)	32K (2^{15})	
	2 × 4 (3 bits)	32K (2^{15})	256K (2^{18})
16 frames (4 bits)	None	4K (2^{12})	
	2 × 2 (2 bits)	32K (2^{15})	256K (2^{18})

Table 3-4 shows the number of colors that the dithering patterns produce on 512-, 4K-, and 256K-color TFT LCDs. For example, if an image that uses the standard VGA 18-bit color palette is displayed on a 512-color TFT LCD (which has only a 9-bit color palette), significant banding or contour lines appear. The dithering engine automatically uses a 2 × 4 pattern to increase the number of displayed colors from the 3 bits per primary color that the LCD produces to the full 6 bits per primary color that the 18-bit VGA color palette requires.

Table 3-4. Number of Colors on 512-, 4K-, and 256K-Color TFT LCDs

Per Primary Color (RGB)		Image		
Bits per Primary Color Available	**Effective Dithering Pattern**	**32K Colors (15 bits)**	**256K Colors (18 bits)**	**16.8M Colors (24 bits)**
3 bits	None	512 (2^9)		
	2 × 2 (2 bits)	32K (2^{15})		
	2 × 4 (3 bits)	32K (2^{15})	256K (2^{18})	
	4 × 4 (4 bits)		256K (2^{18})	256K[a] (2^{18})
4 bits	None	4K (2^{12})		
	2 × 2 (2 bits)	32K (2^{15})	256K (2^{18})	
	2 × 4 (3 bits)		256K (2^{18})	256K[a] (2^{18})
6 bits	None	32K (2^{15})	256K (2^{18})	
	2 × 2 (2 bits)		256K (2^{18})	256K[a] (2^{18})

[a] The CL-GD6245 does not support color modes requiring more colors than the 256K (2^{18}) colors provided by the standard VGA palette.

3.8 Power Management and Sequencing

Notebook and laptop computers have stringent power limitations due to battery operation and heat dissipation. To support these needs, the CL-GD6245 VGA controller is designed with its own power-saving features as well as efficient power management of the display system. The device is manufactured with low-power CMOS technology and provides the following power-saving capabilities:

- Operates at either 3.3 or 5.0 V
- Minimizes video DAC power
- Stops or slows on-chip oscillators and related circuitry to reduce power
- Slows down video-memory refresh
- Turns off I/O circuitry to reduce power

In addition, the CL-GD6245 provides efficient power management of the display system by turning off the LCD flat panel and CRT when they are not being used. The controllers offer both hardware methods (using device pins) and software methods (using programmable timers and on-chip registers) to control the LCD flat panel and CRT.

NOTE: The CL-GD6245 does not support dynamic power switching from 3.3 to 5.0 V or from 5.0 to 3.3 V. When operating at 5.0-V CVCC, it is recommended that a 330-Ω current-limit resistor be added to the AVDD line. When operating at 3.3-V CVCC, it is recommended that a 33-Ω current-limit resistor be added to the AVDD line.

3.8.1 Normal Mode

In the Normal mode, the LCD flat panel and/or the CRT are being used. During the Normal mode, the following occur:

- Display(s) are active and receive power
- Full-screen refresh occurs
- CPU can access:
  - — Display memory
  - — RAMDAC
  - — I/O registers
- Refresh is provided to display memory
- V_{DD} = 3.3 V, when performance permits

Because the power consumption is proportional to the square of the supply voltage, using 3.3 V whenever possible reduces power consumption considerably.

Because power consumption is directly proportional to the frequency at which the controller is operated, the CL-GD6245 uses a proprietary on-chip frame-accelerator. The frame accelerator is used only with dual-scan LCD panels to maintain the maximum screen refresh rate while the internal video clock to the CL-GD6245 functions at 25 MHz or less.

3.8.2 Power-Management Pins

Several dedicated pins have been assigned to facilitate power management while the CL-GD6245 is in LCD-only or CRT-only modes.

- The FPVCC, FPVEE, and FPBACK pins are used to control or enable external voltage-generation circuitry during power sequencing.
- The STANDBY and SUSPEND pins can be connected to external sources to force the system into power-down modes.
- The NPD pin, when high, stops the power-down counters from decrementing. This pin is used to inhibit automatic power-down when the system is supplied from an AC power source.

3.8.3 Standby Mode

Standby mode stops power to the LCD panel (and/or CRT) when the panel is not being used. As a result, since there is no screen refresh, normal clock rates can be stopped or slowed to further reduce power consumption. During Standby mode, the following occurs:

- LCD panel power-down sequence occurs automatically when this mode is entered
- VCLK oscillator is turned off
- MCLK frequency is divided by six
- No clock is provided to the CRT controller
- Video DAC is in low-power mode
- Display-memory refresh is maintained
- The CPU can access and modify the display memory and DAC palette
- When Standby mode is exited, the system returns to the same state it was in before Standby mode was entered

3.8.3.1 Entering Standby Mode

The CL-GD6245 provides three methods for entering Standby mode — two are software-initiated and one is hardware-initiated. All methods offer the features itemized above. One or more of these methods can be used simultaneously to start and/or maintain Standby mode.

- Standby mode can be initiated using software by programming the Standby Mode Timer (CR21[3:0]), in increments of one minute, up to 15 minutes. If the timer is allowed to count down to zero, the Standby-mode power-down sequence is started.
- Standby mode can be initiated using software by setting CR20[4] to '1', starting the Standby-mode power-down sequence.
- Standby mode can be initiated using hardware by connecting the STANDBY input (pin 83) to an external source. When the STANDBY pin is driven high, the Standby-mode power-down sequence starts.

All active methods must be removed to terminate Standby mode and start the power-up sequence.

3.8.3.2 Exiting Standby Mode

The LCD panel power-up sequence occurs automatically when the Standby mode is terminated, which occurs when all of the methods that initiated the mode are removed.

- Reset the Standby Mode Timer in one or more of the following ways:
  - — Use activity on the ACTI input pin, which is enabled by setting CR1D[6] to '1'.
  - — Use any VGA access (memory or I/O), which is enabled by setting CR1D[5] to '1'.
  - — Use any keyboard access, which is enabled by setting SR8[5] to '1'.
- Terminate software-initiated Standby mode by setting CR20[4] to '0'.
- Terminate hardware-initiated Standby mode by driving the STANDBY input pin low.

If a power-up or power-down sequence is in progress when there is a request to enter or exit Standby mode, the power-up/down sequence is allowed to complete before the new request is performed.

3.8.4 Suspend Mode

The CL-GD6245 Suspend mode is used to save power when the system is not actively used for a long time. Suspend mode turns off the screen(s) and suspends operation of application programs. In the case of Hardware-Controlled Suspend mode, this mode prohibits the CPU from accessing display memory, I/O registers, or RAMDAC. In Hardware-Controlled Suspend mode, even though application programs cease to run in either the foreground or background, all the register states are saved. When the Suspend mode is exited, the system returns to the same operational state it was in before Suspend mode was entered.

3.8.4.1 Hardware-Controlled Suspend Mode

Hardware-Controlled Suspend mode is the most efficient means of saving power with the CL-GD6245. Hardware-Controlled Suspend mode is initiated using the SUSPEND input pin. This pin has programmable polarity (using SR8[3]), and it uses a debounce timer (CR23[7:4]) to minimize accidental attempts to initiate Suspend mode. In this mode, power to the input pads and the bus interface is turned off. All I/O pins, except the dedicated Suspend-mode input, are de-activated to further reduce power consumption. Additional power savings occur because CPU host access to display memory is denied, and a slower 32-kHz clock refreshes the display memory by performing CAS*-before-RAS* refresh. This slow-clock input comes from one of two sources:

- By setting CR1D[4] to '1', a 32-kHz clock output results by dividing the 14.318-MHz clock by 432.
- By setting CR1D[4] to '0', an external 32-kHz clock input can be provided via the CLK32K input pin. Further power reduction is thus possible by disabling the 14.318-MHz clock by setting SR16[2] to '1'.

When the system is in Hardware-Controlled Suspend mode, the following occur:

- The LCD panel power-up/down sequence occurs automatically when Suspend mode is entered or exited.
- The VCLK and MCLK oscillators are turned off if CR1C[2] is '1' and CR20[3] is '0'.
- No CPU access is allowed to the following:
  - — Display memory
  - — RAMDAC
  - — I/O registers
- Although display memory cannot be accessed by the CPU during Suspend mode, the contents are preserved. (This action is useful when a system remains inactive for a relatively long time.)
- Register data contents are retained.
- The CL-GD6245 refresh clock for display memory is set to 8 or 64 ms, unless DRAMs are self-refresh (this is controlled by CR20[2:1]).

CAUTION: In local-bus systems, CPU attempts to access the CL-GD6245 can cause a system-hang condition.

3.8.4.2 Software-Controlled Suspend Mode

This mode is initiated by setting CR20[3] to '1'. In contrast to the Hardware-Controlled Suspend mode, Software-Controlled Suspend mode allows the CPU to access video RAM, the I/O bus, and the RAMDAC.

3.8.4.3 Entering Suspend Mode

The following methods are used to initiate Suspend mode. To minimize power consumption, the Hardware-Controlled Suspend mode is recommended.

- The Software-Controlled Suspend mode is entered by setting CR20[3] to '1'. In this mode, CPU access is still active and the SUSPEND pin is disabled. Software-Controlled Suspend mode is not recommended because it requires more power than Hardware-Controlled Suspend mode.
- To enter Hardware-Controlled Suspend mode, connect the dedicated SUSPEND input pin to an external source. The SUSPEND input is programmable in polarity. The CL-GD6245 internal debounce timer (register CR23[7:4]) monitors the input for accidental activation.
- The SUSPEND input pin can also be used to indicate a 'cover-closed' condition by programming CR1C[2] to '0'. This condition prohibits power-down of the MCLK and VCLK. Since CPU access is not disabled in this mode, more power is required.

3.8.4.4 Exiting Suspend Mode

Suspend mode must be terminated/exited in the same manner that it was entered. When the SUSPEND input is driven 'inactive' (high or low

depending on programmed polarity), Suspend mode is terminated. In software, Suspend mode is terminated by clearing CR20[3] to '0'. When Suspend mode is terminated, the system returns to the same operational state it was in before Suspend mode was entered.

3.8.5 Power Sequencing

The CL-GD6245 internal logic controls the sequencing of the LCD contrast voltage, logic power, data inputs, and control inputs. To minimize the possibility of damaging the LCD panel, the CL-GD6245 provides the recommended power-up/down sequences shown below. These sequences meet most panel manufacturer specifications.

3.8.5.1 LCD Panel Power-Up Sequence

1) Drive FPVCC high.
2) Delay 32 ms.
3) Enable the CL-GD6245 LCD panel data and control signals (Data, FPVDCLK, LFS, LLCLK, and MOD).
4) Delay 32 ms.
5) Drive FPVEE and FPBACK high.

3.8.5.2 LCD Panel Power-Down Sequence

1) Drive FPVEE and FPBACK low.
2) Delay 32 ms minimum.
3) Force all CL-GD6245 LCD panel data and control signals low.
4) Delay 32 ms.
5) Drive FPVCC low.

3.8.6 Additional Power Management Features

3.8.6.1 LCD-Only Operation (CRT Disabled)

During LCD-only operation, the CRT is disabled. In this mode, DAC analog power is off, and the HSYNC and VSYNC drive is off.

NOTE: When the CRT is disabled and Text mode is selected, power is removed from the video DAC and LUT. CPU access to the LUT is available by using the I/O read/write to 3C6–3C9. Graphics modes can use the LUT for shading.

3.8.6.2 CRT-Only Operation (LCD Panel Disabled)

During CRT-only operation, the LCD panel is disabled. In this mode, panel-drive signals are all inactive and automatic power-down sequencing occurs.

3.8.6.3 Backlight Timer

An additional internal timer allows the LCD panel backlight to be controlled independently of any power-down modes. Extension register CR21[7:4] can be programmed from 1–15 minutes to activate the backlight timer. When the timer counts down to zero, the FPBACK output will go low and can thus be used to turn off the panel backlight. Programming CR21[7:4] to 0h disables the backlight timer. This timer can be reset to extend the time-out by detecting either activity on the ACTI input or a VGA access. Extension register CR1D controls these choices.

3.8.6.4 ACTI Function

This input pin can be used to reset both the Standby and Backlight internal timers. For example, this pin can be connected to the keyboard interrupt from the system logic. Extension register CR1D[6,3] controls which timers are reset by activity on this pin.

3.9 Analog Outputs

The DAC outputs produce a 0.7-V peak white amplitude when the palette DAC is provided with a constant reference current (I_{REF}). To provide the I_{REF} current, use the circuit shown in the IREF pin description in Section 2.2. For all values of I_{REF} and output loading:

$$V_{black\ level} = 0 \text{ volts}$$

$$V_{max\ white} = 0.7 \text{ volts}$$

3.10 Color Lookup Table

3.10.1 Writing to the Color Lookup Table

To write a color definition to the lookup table, a value specifying an address location in the lookup table is first written to the Write Mode Address register. The color values for the red, green, and blue intensities are then written in succession to the Color Value register. After the blue data is latched, this new color data is then written into the lookup table at the defined

address, and the Write Mode Address register is incremented automatically.

Since the Address register increments after each transfer of data to the lookup table, it is best to write a set of consecutive locations at once. The start address of the set of locations is first written to the Write Mode Address register. The color data for each address location is then sequentially written to the Color Value register. The RAMDAC automatically writes data to the lookup table and increments the Address register after each host transfer of three bytes of color data.

3.10.2 Reading from the Color Lookup Table

To read color data from the lookup table, a value specifying the address location of the data is written to the Read Mode Address register. After the address is latched, the data from this location is automatically read out to the Color Value register and the Read Mode Address register automatically increments.

The color intensity values are then read from the Color Value register by the sequence of three read (RD*) commands. After the blue value is transferred out, new data is read from the lookup table at the current address to the Color Value register and the Address register automatically increments again.

If the Address register is loaded with a new starting address while an unfinished sequence is in progress, the system resets and starts a new sequence. This occurs for both read and write operations.

4. CL-GD6245 VIDEO MODE TABLES

This section presents tables for configuring the CL-GD6245 for various CRT and flat-panel video modes. For detailed information on specific LCD panels that the CL-GD6245 device can drive, refer to the "Panel Interface Guides" section of the *CL-GD6245 Applications Book*.

4.1 CRT Video Modes

Table 4-1. IBM® Standard VGA Video Modes

Mode No. (hex)	No. of Colors	Characters × Rows	Char. Cell (pixels)	Screen Format (pixels)	Display Mode	Video Clock (MHz)	Horizontal Frequency (kHz)	Vertical Frequency (Hz)
0, 1	16/256K	40 × 25	9 × 16	360 × 400	Text	28	31.5	70
2, 3	16/256K	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
4, 5	4/256K	40 × 25	8 × 8	320 × 200	Graphics	25	31.5	70
6	2/256K	80 × 25	8 × 8	640 × 200	Graphics	25	31.5	70
7	Monochrome	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
D	16/256K	40 × 25	8 × 8	320 × 200	Graphics	25	31.5	70
E	16/256K	80 × 25	8 × 8	640 × 200	Graphics	25	31.5	70
F	Monochrome	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
10	16/256K	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
12	16/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
12 [a]	16/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.9	72
13	256/256K	40 × 25	8 × 8	320 × 200	Graphics	25	31.5	70

[a] This mode is an IBM standard VGA mode that has been enhanced by Cirrus Logic for a higher vertical frequency.

The following extended CRT video modes are supported by the Cirrus Logic BIOS. Modes may differ if another BIOS is used.

Table 4-2. Cirrus Logic Extended CRT Video Modes

Mode[a] No. (hex)	VESA® No. (hex)	No. of Colors	Characters × Rows	Character Cell (pixels)	Screen Format (pixels)	Display Mode	Video Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)
14	–	16/256K	132 × 25	8 × 16	1056 × 400	Text	41.5	31.5	70
54	10A	16/256K	132 × 43	8 × 8	1056 × 350	Text	41.5	31.5	70
55	109	16/256K	132 × 25	8 × 14	1056 × 350	Text	41.5	31.5	70
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	40	37.8	60
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	50	48.1	72
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	40	37.9	60
5C[b]	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	50[b]	48.1	72
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	65	48.3	60
5D[c]	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	44.9	35.5	87
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	72

[a] Some modes are not supported by all monitors. The best-quality vertical refresh rate for the monitor type selected will be automatically used.

[b] Mode 5C with 72-Hz vertical frequency is available only when high-performance memory has been enabled with function 9Eh, and the dot clock is at least 50 MHz. If high-performance memory is disabled, a refresh rate of 60 Hz will be substituted.

[c] Mode 5D with a vertical frequency of 87 Hz is an interlaced mode.

4.2 LCD Flat-Panel Video Modes

Table 4-3. IBM® Standard VGA Video Modes

Mode No. (hex)	Mono. STN Number of Shades	Color STN Number of Colors	Color TFT Number of Colors	Characters × Rows	Character Cell (pixels)	CRT Screen Format (pixels)	Display Mode	Expanded Size (pixels)
0, 1	16/16	16/256K	16/256K	40 × 25	8 × 16	360 × 400	Text	640 × 475
2, 3	16/16	16/256K	16/256K	80 × 25	8 × 16	720 × 400	Text	640 × 475
4, 5	4/64	4/256K	4/256K	40 × 25	8 × 8	320 × 200	Graphics	640 × 475
6	2/16	2/256K	2/256K	80 × 25	8 × 8	640 × 200	Graphics	640 × 475
7	2/16	Mono.	Mono.	80 × 25	8 × 16	720 × 400	Text	640 × 475
D	16/64	16/256K	16/256K	40 × 25	8 × 8	320 × 200	Graphics	640 × 475
E	16/16	16/256K	16/256K	80 × 25	8 × 8	640 × 200	Graphics	640 × 475
F	2/16	Mono.	Mono.	80 × 25	8 × 14	640 × 350	Graphics	640 × 475
10	16/16	16/256K	16/256K	80 × 25	8 × 14	640 × 350	Graphics	640 × 475
11	2/16	2/256K	2/256K	80 × 30	8 × 16	640 × 480	Graphics	640 × 480
12	16/16	16/256K	16/256K	80 × 30	8 × 16	640 × 480	Graphics	640 × 480
13	64/256K	256/256K	256/256K	40 × 25	8 × 8	320 × 200	Graphics	640 × 480

The following extended LCD video mode is supported by the Cirrus Logic BIOS. Modes may differ if another BIOS is used.

Table 4-4. Cirrus Logic Extended LCD Video Mode

Mode No. (hex)	Mono. STN Number of Shades	Color STN Number of Colors	Color TFT Number of Colors	Characters × Rows	Character Cell (pixels)	CRT Screen Format (pixels)	Display Mode	Expanded Size (pixels)
5F	64/256K	256/256K	256/256K	80 × 30	8 × 16	640 × 480	Graphics	640 × 480

5. VGA REGISTER PORT MAP

Table 5-1. VGA Register Port Map

Address	Port	Port Type
3?4[a]	CRT controller index	Read/Write
3?5[a]	CRT controller data	Read/Write
3BA	Feature control — monochrome	Write
	Input Status register 1 — monochrome	Read
3C0	Attribute controller index/data	Write
3C1	Attribute controller index/data	Read
3C2	Miscellaneous output	Write
	Input Status register 0	Read
3C3	VGA enable	Read/Write
3C4	Sequencer index	Read/Write
3C5	Sequencer data	Read/Write
3C6	Video DAC pixel mask	Read/Write
3C7	Pixel Address Read mode	Write
	DAC state	Read
3C8	Pixel Mask Write mode	Read/Write
3C9	Pixel data	Read/Write
3CA	Feature control readback	Read
3CC	Miscellaneous output readback	Read
3CE	Graphics controller index	Read/Write
3CF	Graphics controller data	Read/Write
3DA	Feature control — color	Write
	Input Status register 1 — color	Read

[a] The '?' in an address is 'B' for monochrome and 'D' for color.

6. REGISTER INFORMATION

The following tables list VGA registers and extension registers contained in the CL-GD6245. The CL-GD6245 extension registers are fully explained later in this section. Page cross-references to the detailed register descriptions are provided where applicable. For standard VGA register information, see IBM (and other) documentation.

6.1 Register Summary Tables

External/General Registers

Abbreviation	Register Name	Index	Port	Page
MISC	Miscellaneous Output	–	3C2 (W)	
MISC	Miscellaneous Input	–	3CC (R)	
FC	Feature Control	–	3?A (W)	
FC	Feature Control	–	3CA (R)	
FEAT	Input Status Register 0	–	3C2	
STAT	Input Status Register 1	–	3?A	55
3C6	Pixel Mask	–	3C6	
3C7	Pixel Address Read Mode	–	3C7 (W)	
3C7	DAC State	–	3C7 (R)	
3C8	Pixel Address Write Mode	–	3C8	
3C9	Pixel Data	–	3C9	

The *?* in the port address is *B* for monochrome mode and *D* for color mode.

VGA Sequencer Registers

Abbreviation	Register Name	Index	Port
SRX	Sequencer Index	–	3C4
SR0	Reset	0	3C5
SR1	Clocking Mode	1	3C5
SR2	Plane Mask	2	3C5
SR3	Character Map Select	3	3C5
SR4	Memory Mode	4	3C5

CRT Controller Registers

Abbreviation	Register Name	Index	Port
CRX	CRTC Index	–	3?4
CR0	Horizontal Total	0	3?5
CR1	Horizontal Display End	1	3?5
CR2	Horizontal Blanking Start	2	3?5
CR3	Horizontal Blanking End	3	3?5
CR4	Horizontal Sync Start	4	3?5
CR5	Horizontal Sync End	5	3?5
CR6	Vertical Total	6	3?5
CR7	Overflow	7	3?5
CR8	Screen A Preset Row Scan	8	3?5
CR9	Character Cell Height	9	3?5
CRA	Text Cursor Start	A	3?5
CRB	Text Cursor End	B	3?5
CRC	Screen Start Address High	C	3?5
CRD	Screen Start Address Low	D	3?5
CRE	Text Cursor Location High	E	3?5
CRF	Text Cursor Location Low	F	3?5
CR10	Vertical Sync Start	10	3?5
CR11	Vertical Sync End	11	3?5
CR12	Vertical Display End	12	3?5
CR13	Offset	13	3?5
CR14	Underline Row Scan	14	3?5
CR15	Vertical Blanking Start	15	3?5
CR16	Vertical Blanking End	16	3?5
CR17	CRTC Mode Control	17	3?5
CR18	Line Compare	18	3?5
CR22	Graphics Data Latches Readback	22	3?5
CR24	Attribute Controller Toggle Readback	24	3?5
CR26	Attribute Controller Index Readback	26	3?5
CR28	Reserved		
CR2A–CR3F	Reserved		

The *?* in the port address is *B* for monochrome mode and *D* for color mode.

VGA Graphics Controller Registers

Abbreviation	Register Name	Index	Port	Page
GRX	Graphics Controller Index	–	3CE	
GR0	Set/Reset	0	3CF	56
GR1	Set/Reset Enable	1	3CF	57
GR2	Color Compare	2	3CF	
GR3	Data Rotate	3	3CF	
GR4	Read Map Select	4	3CF	
GR5	Mode	5	3CF	58
GR6	Miscellaneous	6	3CF	
GR7	Color Don't Care	7	3CF	
GR8	Bit Mask	8	3CF	

VGA Attribute Controller Registers

Abbreviation	Register Name	Index	Port	Page
ARX	Attribute Controller Index	–	3C0/3C1	
AR0–ARF	Attribute Controller Palette	0–F	3C0/3C1	
AR10	Attribute Controller Mode Control	10	3C0/3C1	
AR11	Overscan (Border) Color	11	3C0/3C1	
AR12	Color Plane Enable	12	3C0/3C1	
AR13	Pixel Panning	13	3C0/3C1	
AR14	Color Select	14	3C0/3C1	

NOTES:

1) VGA Attribute Controller Data registers (AR0–ARF and AR10–AR14) are read from port 3C1 and written to port 3C0.

2) After initialization, I/O writes to 3C0 toggle between the Attribute Controller Index register (ARX) and the VGA Attribute Controller Data registers.

CL-GD6245 Extension Registers

Abbreviation	Register Name	Index	Port	Page
SR6	Unlock All Register Extensions	6	3C5	59
SR7	Extended Sequencer Modes	7	3C5	60
SR8	Miscellaneous Control 1	8	3C5	61
SR9	Scratchpad 0	9	3C5	63
SRA	Scratchpad 1	A	3C5	63
SRB	VCLK0 Numerator Value	B	3C5	64
SRC	VCLK1 Numerator Value	C	3C5	64
SRD	VCLK2 Numerator Value	D	3C5	64
SRE	VCLK3 Numerator Value	E	3C5	64
SRF	DRAM Control	F	3C5	66
SR10	Graphics Cursor X Position 0	10	3C5	68
SR11	Graphics Cursor Y Position 0	11	3C5	69
SR12	Graphics Cursor Attributes	12	3C5	70
SR13	Graphics Cursor Pattern Address Offset	13	3C5	71
SR14	Scratchpad 2	14	3C5	63
SR15	Scratchpad 3	15	3C5	63
SR16	Miscellaneous Control 2	16	3C5	72
SR19	Scratchpad 4	19	3C5	63
SR1A	Dual-Scan Color Control	1A	3C5	73
SR1B	VCLK0 Denominator and Post-scalar Values	1B	3C5	74
SR1C	VCLK1 Denominator and Post-scalar Values	1C	3C5	74
SR1D	VCLK2 Denominator and Post-scalar Values	1D	3C5	74
SR1E	VCLK3 Denominator and Post-scalar Values	1E	3C5	74
SR1F	Memory Clock Frequency Programming	1F	3C5	76
SR30	Graphics Cursor X Position 1	30	3C5	68
SR31	Graphics Cursor Y Position 1	31	3C5	69
SR50	Graphics Cursor X Position 2	50	3C5	68
SR51	Graphics Cursor Y Position 2	51	3C5	69
SR70	Graphics Cursor X Position 3	70	3C5	68
SR71	Graphics Cursor Y Position 3	71	3C5	69
SR90	Graphics Cursor X Position 4	90	3C5	68
SR91	Graphics Cursor Y Position 4	91	3C5	69
SRB0	Graphics Cursor X Position 5	B0	3C5	68
SRB1	Graphics Cursor Y Position 5	B1	3C5	69
SRD0	Graphics Cursor X Position 6	D0	3C5	68
SRD1	Graphics Cursor Y Position 6	D1	3C5	69
SRF0	Graphics Cursor X Position 7	F0	3C5	68
SRF1	Graphics Cursor Y Position 7	F1	3C5	69
GR9	Offset 0	9	3CF	77
GRA	Offset 1	A	3CF	78
GRB	Graphics Controller Mode Extensions	B	3CF	79
CR19	Interlace End	19	3?5	80
CR1A	Interlace Control	1A	3?5	81
CR1B	Extended Display Controls	1B	3?5	82
CR1C	Flat-Panel Interface	1C	3?5	84

CL-GD6245 Extension Registers (cont.)

Abbreviation	Register Name	Index	Port	Page
CR1D	Flat-Panel Display Controls	1D	3?5	86
CR1E	Flat-Panel Shading	1E	3?5	88
CR1F	Flat-Panel Modulation Control	1F	3?5	90
CR20	Power Management	20	3?5	91
CR21	Power-Down Timers Control	21	3?5	93
CR23	FPVCC/FPBACK Control and SUSPEND Timer	23	3?5	94
CR25	Part Status	25	3?5	95
CR27	Chip ID	27	3?5	96
CR29	Part Configuration	29	3?5	97

The *?* in the port address is *B* for monochrome mode and *D* for color mode.

CL-GD6245 LCD Timing Registers

Abbreviation	Register Name	Index	Port	Page
CR0X	Horizontal Total for 80-Column Display	1D	3?5	99
CR1X	Horizontal Total for 40-Column Display	1D	3?5	100
CR2X	LFS Vertical Counter Value Compare (MISC[7:6] = '11')	1D	3?5	101
CR3X	LFS Vertical Counter Value Compare (MISC[7:6] = '10')	1D	3?5	102
CR4X	LFS Vertical Counter Value Compare (MISC[7:6] = '01')	1D	3?5	103
CR5X	LFS Vertical Counter Value Compare (MISC[7:6] = '00')	1D	3?5	104
CR6X	LFS Vertical Counter Value Compare Overflow	1D	3?5	105
CR7X	Panel Signal Control for Color TFT Panels	1D	3?5	106
CR8X	STN Color Panel Data Format	1D	3?5	107
CR9X	TFT Panel Data Format	1D	3?5	108
CRAX	TFT Panel HSYNC Position Control	1D	3?5	109
CRBX	Special Functions	1D	3?5	110

The *?* in the port address is *B* for monochrome mode and *D* for color mode.

6.2 Extended External/General and VGA Graphics Controller Registers

NOTE: *Reserved* and *Unused* bits are initialized to '0' at Reset, unless otherwise specified.

6.2.1 STAT: Input Status Register 1

I/O Port Address: 3?A

Index: 1

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved/Interlaced Field Status	R	'0'
5	Diagnostic 1	R	'0'
4	Diagnostic 0	R	'0'
3	Vertical Retrace	R	'0'
2	Reserved		
1	Reserved		
0(LSB)	Display Enable	R	'0'

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit — **Description**

7 — Reserved

6 — **Reserved** in VGA-compatible mode.
Interlaced Field Status: If Interlaced mode is programmed by setting the CRTC register, CR1A[0] = '1', then this bit reflects the interlaced-frame field number.

5:4 — **Diagnostic [1:0]:** These bits are used for diagnostic testing. They reflect the state of bits 5:4 of the Color Plane Enable register (AR12[5:4]), as indicated in the following table. (The color values for pixel bits P[7] and P[6] depend on how many colors are used.)

AR12[5]	AR12[4]	STAT[5]	STAT[4]
'0'	'0'	P[2] pixel bit 2 (red)	P[0] pixel bit 0 (blue)
'0'	'1'	P[3] pixel bit 3 (secondary blue)	P[1] pixel bit 1 (green)
'1'	'0'	P[5] pixel bit 5 (secondary red)	P[4] pixel bit 4 (secondary green)
'1'	'1'	P[7] pixel bit 7	P[6] pixel bit 6

3 — **Vertical Retrace:** A '1' indicates that vertical retrace is in progress.

2:1 — Reserved

0 — **Display Enable:** If this bit is read as a '0', video is being serialized and displayed. If this bit is read as a '1', vertical or horizontal blanking is active.

6.2.2 GR0: Set/Reset (CL-GD6245 Extensions)

I/O Port Address: 3CF

Index: 0

Bit	VGA Write Mode 0/3	Extended Write Mode 5	Reset State
7(MSB)	Set/Reset Map 7	Background Color Bit 7	'0'
6	Set/Reset Map 6	Background Color Bit 6	'0'
5	Set/Reset Map 5	Background Color Bit 5	'0'
4	Set/Reset Map 4	Background Color Bit 4	'0'
3	Set/Reset Map 3	Background Color Bit 3	'0'
2	Set/Reset Map 2	Background Color Bit 2	'0'
1	Set/Reset Map 1	Background Color Bit 1	'0'
0(LSB)	Set/Reset Map 0	Background Color Bit 0	'0'

The function of these bits is changed from the normal VGA Set/Reset definition. These bits define the *background* color if the CL-GD6245 Extended Write mode 5 is selected as described in the GR5 and GRB register descriptions.

Bit	Description
7:0	**Set/Reset Map for Background Color:** If GRB[2] = '1', then bits [7:4] of this register are set to '1's and are read/write, but VGA Write modes 0 through 3 use only bits [3:0] of this register. If GRB[2] = '0', then bits [7:4] of this register are set to '0's and are read only.

6.2.3 GR1: Set/Reset Enable (CL-GD6245 Extensions)

I/O Port Address: 3CF

Index: 1

Bit	VGA Write Mode 0	Extended Write Mode 4/5	Reset State
7(MSB)	Enable Set/Reset Map 7	Foreground Color Bit 7	'0'
6	Enable Set/Reset Map 6	Foreground Color Bit 6	'0'
5	Enable Set/Reset Map 5	Foreground Color Bit 5	'0'
4	Enable Set/Reset Map 4	Foreground Color Bit 4	'0'
3	Enable Set/Reset Map 3	Foreground Color Bit 3	'0'
2	Enable Set/Reset Map 2	Foreground Color Bit 2	'0'
1	Enable Set/Reset Map 1	Foreground Color Bit 1	'0'
0(LSB)	Enable Set/Reset Map 0	Foreground Color Bit 0	'0'

The function of these bits is changed from the normal VGA Set/Reset Enable definition. These bits define the *foreground* color if the CL-GD6245 Extended Write mode 4 or 5 is selected as described in the GR5 and GRB register descriptions.

Bit	Description
7:0	**Set/Reset Map Enable for Foreground Color:** If GRB[2] = '1', then bits [7:4] of this register are set to '1's and are read/write, but VGA Write mode 0 uses only bits [3:0] of this register. If GRB[2] = '0', then bits [7:4] of this register are set to '0's and are read only.

6.2.4 GR5: Mode (CL-GD6245 Extensions)

I/O Port Address: 3CF

Index: 5

Bit	Description	Mode	Reset State
7(MSB)	Reserved		
6	256-Color Mode (used in all 256-color modes)	VGA	n/a
5	Shift Register Mode	VGA	n/a
4	Odd/Even	VGA	n/a
3	Read Type	VGA	n/a
2	Extended Write Mode Select 2	CL-GD6245	n/a
1	Write Mode Select 1	VGA	n/a
0(LSB)	Write Mode Select 0	VGA	n/a

Bit	Description
7	Reserved
6:3	These are normal VGA functions and are not explained here.
2	**Extended Write Mode Select [2]:** When GRB[2] = '1', then this is a third write mode select bit that can be used in conjunction with GR5[1:0] (Write Mode Select [1:0]). Clearing GRB[2] to '0' directly clears GR5[2] to '0', and makes it read-only.
1:0	**Write Mode Select [1:0]:** When GRB[2] = '0' and GR5[2] = '0', these bits select standard VGA Write Modes 3 through 0. When GRB[2] = '1' and GR5[2] = '1', these two bits select Extended Write modes 4 and 5 (explained below). Extended Write modes 6 and 7 are not implemented.

Extended write modes 4 and 5 expand data as follows. If a single bit of a 4-bit nibble of a data byte is 'on', then the extended write mode expands that single bit to eight 'on' bits. If a single bit of a data nibble is 'off', then the extended write mode does not change that bit.

The extended write modes can be used for text writing, line drawing, or pattern filling. Both extended write modes should be used with GRB[1] set to '1', which selects x8 addressing.

Extended Write Mode 4: 256-Color Expansion with Background Unchanged

With this mode, if a single bit of a 4-bit nibble of a data byte is 'on', then that single bit expands to 8 bits and the Set/Reset Enable register (GR1) selects the foreground color for this expansion. If, however, a single bit of a 4-bit nibble of a data byte is 'off', then GR1 does not expand the bit or change the bit's color.

NOTE: The Set/Reset Enable register (GR1) and the Plane Mask register (SR2) are both normally 4 bits, for 4-bit nibbles. To extend both GR1 and SR2 to 8 bits (for 8-bit bytes), set GRB[2] to '1'.

Extended Write Mode 5: 256-Color Expansion with Background Changed

With this mode, if a single bit of a 4-bit nibble of a data byte is 'off', then that single bit expands to 8 bits and the Set/Reset register (GR0) selects the background color over which the expanded 8 bits will appear.

NOTE: The Set/Reset register (GR0) and the Plane Mask register (SR2) are both normally 4 bits, for 4-bit nibbles. To extend both GR0 and SR2 to 8 bits (for 8-bit bytes), set GRB[2] to '1'.

6.3 CL-GD6245 Extension Registers

NOTE: *Reserved* and *Unused* bits are initialized to '0' at Reset, unless otherwise specified.

6.3.1 SR6: Unlock All Register Extensions

I/O Port Address: 3C5

Index: 6

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Extension Register Access Value 4	R/W	'0'
3	Extension Register Access Value 3	R/W	'0'
2	Extension Register Access Value 2	R/W	'0'
1	Extension Register Access Value 1	R/W	'0'
0(LSB)	Extension Register Access Value 0	R/W	'0'

This register is used to enable or disable access to all the Extension registers, including the LCD Timing registers at CR0X to CRBX. Note that the LCD Timing registers also have an enable bit at extension register CR1D[7].

Bit	Description
7:5	Reserved
4:0	**Extension Register Access Value [4:0]:** If this field is programmed with 'XXX1X010', it will be read as '00010010' (12h), and the Extension registers are enabled for read and write access. If this field is programmed with any other value, it will be read as '00001111' (0Fh), and the Extension registers are disabled for read and write access.

6.3.2 SR7: Extended Sequencer Modes

I/O Port Address: 3C5

Index: 7

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Select LCD Panel 2	R	= MD14
5	Select LCD Panel 1	R	= MD13
4	Select LCD Panel 0	R	= MD12
3	Reserved		
2	Reserved		
1	Reserved		
0(LSB)	256-Color Mode and Packed-Pixel	R/W	'0'

Bit	Description
7	Reserved
6:4	**Select LCD Panel [2:0]:** The state of memory data lines MD[14:12] is latched at system reset and stored in bits 6:4. The Cirrus Logic BIOS uses these bits to select an LCD panel class.
3:1	Reserved
0	**256-Color Mode and Packed-Pixel:** If this bit is programmed to a '1', the Video Shift registers are configured so that one character clock is equal to eight pixels. At the same time, true packed-pixel memory addressing is enabled. If this bit is programmed to '0', this mode is 'don't care'. **NOTE:** With true packed-pixel addressing, consecutive pixels are stored at consecutive addresses in display memory. In contrast, with Chain-4 addressing, consecutive pixels are stored at every fourth address.

6.3.3 SR8: Miscellaneous Control 1

I/O Port Address: 3C5

Index: 8

Bit	Description	Access	Reset State
7(MSB)	Symmetrical DRAM Addressing	R/W	= DUALCAS
6	Disable MEMCS16* for Display Memory	R/W	'0'
5	Reset Standby Timer	R/W	'0'
4	Reset Backlight Timer	R/W	'0'
3	SUSPEND Active Polarity	R/W	'0'
2	Select LCD Panel 2 (duplicate)	R	= MD14
1	Select LCD Panel 1 (duplicate)	R	= MD13
0(LSB)	Select LCD Panel 0 (duplicate)	R	= MD12

Bit	Description
7	**Symmetrical DRAM Addressing:** This bit selects symmetrical DRAM addressing for page-mode text on a CRT. This bit is set to '1' only if using the CL-GD6245 with dual-WE* DRAMs that support 9-bit addressing (symmetrical DRAM) *and* the CRT is set for 132-column text mode (CR1B[6] = '1'). The Reset state of this bit is determined by the setup of the DUALCAS input (pin 78). If dual-CAS* DRAM is selected (pin 78 is connected to VDD), then bit 7 defaults to '1' and symmetrical addressing is automatically set. To enable asymmetrical dual-CAS* DRAM, bit 7 must be programmed manually to '0'. If dual-WE* DRAM is selected (pin 78 is connected to VSS), then bit 7 defaults to '0' and asymmetrical addressing is automatically set. To enable symmetrical dual-WE* DRAM, bit 7 must be programmed manually to '1'. For a 256K × 4 DRAM environment (that is, pin 78 is connected to VSS), then bit 7 defaults to '0' and asymmetrical addressing is automatically set. However, because all 256K × 4 DRAMs are symmetrical, bit 7 must be programmed manually to '1'.
6	**Disable MEMCS16* for Display Memory:** If this bit is programmed to '1', accesses to display memory will not cause MEMCS16* to become active. This option prevents interference when two video subsystems are installed (that is, a portable computer is mounted in a docking station). This bit functions only when the CL-GD6245 is installed on an ISA-bus adapter. For all other bus configurations, this bit must be programmed to '0'.

6.3.3 SR8: Miscellaneous Control 1 *(cont.)*

Bit	Description
5	**Reset Standby Timer:** This bit is used to reset the internal Standby mode timer when there is an I/O read to the keyboard controller (port 60h).
4	**Reset Backlight Timer:** This bit is used to reset the internal Backlight timer when there is an I/O read to the keyboard controller (port 60h).
3	**SUSPEND Active Polarity:** This bit selects the polarity of the SUSPEND input pin, which activates Suspend mode. This bit must be set to match the input state of the SUSPEND input before activating the MCLK and VCLK power-down operation with register CR1C[2]. If this bit is set to a '0', then SUSPEND pin is active high (reset state). If this bit is set to a '1', then SUSPEND pin is active low.
2:0	**Select LCD Panel [2:0] (duplicate):** These bits duplicate the MD[14:12] data values of SR7[6:4]. This duplication is to ensure consistency with the CL-GD62XX family of VGA controllers.

6.3.4 SR9, SRA, SR14, SR15, SR19: Scratchpad [0, 1, 2, 3, 4]

I/O Port Address: 3C5

Index: 9, A, 14, 15, 19

Bit	Description	Access	Reset State
7(MSB)	R/W Data 7	R/W	'0'
6	R/W Data 6	R/W	'0'
5	R/W Data 5	R/W	'0'
4	R/W Data 4	R/W	'0'
3	R/W Data 3	R/W	'0'
2	R/W Data 2	R/W	'0'
1	R/W Data 1	R/W	'0'
0(LSB)	R/W Data 0	R/W	'0'

CAUTION: These registers are reserved for the CL-GD6245 BIOS and must *never* be written by an application program. They are listed here only to indicate their purpose.

Bit	Description
7:0	**R/W Data [7:0]:** These bits are reserved for Cirrus Logic video BIOS.

6.3.5 SRB, SRC, SRD, SRE: VCLK[0, 1, 2, 3] Numerator Value

I/O Port Address: 3C5

Index: B, C, D, E

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	VCLK Numerator 6	R/W	See table below
5	VCLK Numerator 5	R/W	See table below
4	VCLK Numerator 4	R/W	See table below
3	VCLK Numerator 3	R/W	See table below
2	VCLK Numerator 2	R/W	See table below
1	VCLK Numerator 1	R/W	See table below
0(LSB)	VCLK Numerator 0	R/W	See table below

These registers are used in conjunction with SR1B–SR1E (Section 6.3.13) to establish the frequency of the four possible video clocks. The video clock used is selected by register MISC[3:2]. Each video clock frequency is determined using the following equation:

$$\text{VCLKn frequency} = \frac{OSC \times N}{D \times (P + 1)}$$

Where:

OSC = input clock frequency (14.318 MHz)
N = numerator = value of bits SRi[6:0], where i = B, C, D, E
D = denominator = value of bits SR1i[5:1], where i = B, C, D, E
P = post-scalar = value of bits SR1i[0], where i = B, C, D, E
If n = 0, then i = B
If n = 1, then i = C
If n = 2, then i = D
If n = 3, then i = E

These registers (SRB–SRE) determine the numerator (*N*). For information on the denominator (*D*) and post-scalar (*P*) values, see the discussion on registers SR1B–SR1E (Section 6.3.13).

The following table shows the reset values of the registers that determine the video clock frequency. The table also shows the corresponding video clock frequency at system reset.

6.3.5 SRB, SRC, SRD, SRE: VCLK[0, 1, 2, 3] Numerator Value *(cont.)*

Video Clock (VCLKn)	VCLKn Numerator Value			VCLKn Denominator and Post-scalar Value[a]				Reset Freq. (MHz)
	Register (SRi)	At Reset:		Register (SR1i)	At Reset:			
		Register Value (hex)	*N* = Numerator (decimal)		Register Value (hex)	*D* = Denominator (decimal)	*P* = Post-scalar (decimal)[b]	
VCLK0	SRB	66h	102	SR1B	3Bh	29	1	25.180
VCLK1	SRC	5Bh	91	SR1C	2Fh	23	1	28.325
VCLK2	SRD	45h	69	SR1D	30h	24	0	41.165
VCLK3	SRE	7Eh	126	SR1E	33h	25	1	36.082

[a] See Section 6.3.13 for discussion on register SR1i and setting the decimal value of the denominator (*D*) and post-scalar (*P*).

[b] Note that if the post-scalar (*P*) is '1', then the VCO (voltage controlled oscillator) is running at two times the input clock frequency (*OSC*).

Bit	Description
7	Reserved
6:0	**VCLK Numerator [6:0]:** These bits determine the numerator value (*N*) used to determine the video clock frequency.

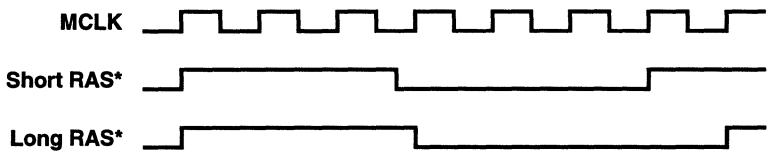
6.3.6 SRF: DRAM Control

I/O Port Address: 3C5

Index: F

Bit	Description	Access	Reset State
7(MSB)	Extended Frame-Accelerator Enable	R/W	'0'
6	Reserved		
5	CPU Write Buffer Depth Control	R/W	'0'
4	Reserved		
3	Reserved		
2	RAS* Timing Select	R/W	'1'
1	MCLK Frequency Select 1	R/W	'1'
0(LSB)	MCLK Frequency Select 0	R/W	'1'

Bit	Description
7	**Extended Frame-Accelerator Enable:** When this bit is '1', the internal refresh mechanism provides only half the normal refresh cycles, thereby reducing power in dual-scan monochrome LCD-only mode.
6	Reserved
5	**CPU Write Buffer Depth Control:** When this bit is programmed to a '0', the CPU Write Buffer depth is set to one level (16 bits/level), and this is the default. This setting is typically used for standard video modes and Extended 16-Color modes. When this bit is programmed to a '1', the CPU Write Buffer depth is set to four levels (16 bits/level). This setting should never be used for any Text mode. This setting is typically used for any Extended 8-bit Pixel modes. In local-bus mode, this bit has no effect. The depth is always set to one level.
4:3	Reserved
2	**RAS* Timing Select:** When this bit is programmed to '1' (the default), RAS* timing for **short-RAS* DRAMs** is selected. In this mode, the RAS* output (pin 142) is high for 2.5+ MCLK cycles, and low for 3.0+ MCLK cycles, for a total period of 6.0 MCLK cycles. When this bit is programmed to '0', RAS* timing for **long-RAS* DRAMs** is selected. In this mode, the RAS* output is high for 3 MCLK cycles, and low for 4 MCLK cycles. **NOTE:** The long-RAS* timing option allows faster MCLKs with DRAMs that have a better CAS* cycle time without violating RAS* access-time requirements.



6.3.6 SRF: DRAM Control *(cont.)*

Bit	Description
1:0	**MCLK Frequency Select [1:0]:** These bits select the active memory clock frequency according to the table below. These bits also set the value that is automatically programmed into SR1F[5:0].

Clock	SRF[1]	SRF[0]	MCLK Frequency (MHz)	Corresponding Value Automatically Programmed in SR1F[5:0]
MCLK0	'0'	'0'	50.1	1Ch
MCLK1	'0'	'1'	44.7	19h
MCLK2[a]	'1'	'0'	25.0	1Ch
MCLK3 (default at reset)	'1'	'1'	37.5	15h

[a] MCLK2 is a special case that enables the MCLK frequency to be divided by two.

CAUTION: Do not select an MCLK frequency that is slower than the VCLK frequency.

6.3.7 SR10, SR30, SR50, SR70, SR90, SRB0, SRD0, SRF0: Graphics Cursor X Position [0-7]

I/O Port Address: 3C5

Index: 10, 30, 50, 70, 90, B0, D0, F0

Bit	Description	Access	Reset State
7(MSB)	Cursor X 10	R/W	'0'
6	Cursor X 9	R/W	'0'
5	Cursor X 8	R/W	'0'
4	Cursor X 7	R/W	'0'
3	Cursor X 6	R/W	'0'
2	Cursor X 5	R/W	'0'
1	Cursor X 4	R/W	'0'
0(LSB)	Cursor X 3	R/W	'0'

This register, and bits 7:5 of the index used to access it, define the horizontal (X) pixel-offset of the graphics cursor.

The data forms the upper 8 bits of the 11-bit position, and bits 7:5 of the index form the lower 3 bits. As a result of this definition, the entire 11-bit cursor offset can be written in a single 16-bit I/O write. The offset must be placed in CPU register AX[15:5]. Also, CPU register AX[4:0] must be '10000', and CPU register DX must be 03C4. If 10, 30, 50, 70, 90, B0, D0, or F0 is written to 3C4 without writing to 3C5 (a byte write), then a read of 3C4 will return the *previously* stored 3 bits of the cursor position.

Bit	Description
7:0	**Cursor X [10:3]:** This 8-bit field forms the upper 8 bits of the 11-bit horizontal offset of the graphics cursor. The index used to access this register forms the lower 3 bits of the 11-bit offset.

6.3.8 SR11, SR31, SR51, SR71, SR91, SRB1, SRD1, SRF1: Graphics Cursor Y Position [0-7]

I/O Port Address: 3C5

Index: 11, 31, 51, 71, 91, B1, D1, F1

Bit	Description	Access	Reset State
7(MSB)	Cursor Y 10	R/W	'0'
6	Cursor Y 9	R/W	'0'
5	Cursor Y 8	R/W	'0'
4	Cursor Y 7	R/W	'0'
3	Cursor Y 6	R/W	'0'
2	Cursor Y 5	R/W	'0'
1	Cursor Y 4	R/W	'0'
0(LSB)	Cursor Y 3	R/W	'0'

This register, and bits 7:5 of the index used to access it, define the vertical (Y) pixel offset of the graphics cursor.

The data forms the upper 8 bits of the 11-bit position, and bits 7:5 of the index form the lower 3 bits. As a result of this definition, the entire 11-bit cursor offset can be written in a single 16-bit I/O write. The offset must be placed in CPU register AX[15:5]. Also, CPU register AX[4:0] must be '10000', and CPU register DX must be 03C4. If 11, 31, 51, 71, 91, B1, D1, or F1 is written to 3C4 without writing to 3C5 (a byte write), then a read of 3C4 will return the *previously* stored 3 bits of the cursor position.

Bit	Description
7:0	**Cursor Y [10:3]:** This 8-bit field forms the upper 8 bits of the 11-bit vertical offset of the graphics cursor. The index used to access this register forms the lower 3 bits of the 11-bit offset.

6.3.9 SR12: Graphics Cursor Attributes

I/O Port Address: 3C5

Index: 12

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Allow Access to DAC Extended Colors	R/W	'0'
0(LSB)	Graphics Hardware Cursor Enable	R/W	'0'

Bit — **Description**

7:2 — Reserved

1 — **Allow Access to DAC Extended Colors:** The table below shows the result of programming this bit:

SR12[1]	Result		
	DAC Lookup Table (LUT) Entry	How LUT Table Entry Is Used	How LUT Entry Is Accessible
'0'	Entire LUT	Entire LUT is VGA-compatible.	Entire LUT is accessible
'1'	256 [a]	Used as hardware cursor background.	Accessible as Location X0h.
	257 [a]	Used as hardware cursor foreground.	Accessible as Location XFh.
	258	Provides selected overscan color.	Accessible as Location X2h.

[a] When SR12[1] = '1', DAC lookup table entries 256 and 257 provide a cursor that is completely independent of the display data colors.

0 — **Graphics Hardware Cursor Enable:** If this bit is set to a '1', the graphics hardware cursor is enabled and will appear on the screen. If this bit is programmed to '0' (the default), the graphics hardware cursor is disabled and will not appear on the screen. See SR13[1:0] for cursor pattern select options.

6.3.10 SR13: Graphics Cursor Pattern Address Offset

I/O Port Address: 3C5

Index: 13

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Cursor Pattern Select 1	R/W	'0'
0(LSB)	Cursor Pattern Select 0	R/W	'0'

Bit	Description
7:2	Reserved
1:0	**Cursor Pattern Select [1:0]:** When SR12[0] = '1', this 2-bit field is used to select one of four possible 32 × 32 bit cursor patterns stored at the top (highest addressed 8 Kbytes) of the display memory.

6.3.11 SR16: Miscellaneous Control 2

I/O Port Address: 3C5

Index: 16

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Select Minimum-Delayed RDY#	R/W	'0'
4	Timing Adjust for '486 COMMAND Pin	R/W	'0'
3	Divide VCLK by Four		
2	OSC Input Disable in Suspend Mode	W	'0'
1	DRAM Interface-Input Threshold Select	W	'0'
0(LSB)	CPU-Bus Interface-Input Threshold Select	W	'0'

This register is reserved exclusively for the CL-GD6245 BIOS and must never be written by an application program. It is listed here only for completeness.

Bit	Description
7:6	Reserved
5	**Select Minimum-Delayed RDY#:** When this bit is set to '0', the minimum signal delay for RDY# (pin 162) for memory cycles is selected. This is the normal setting for this bit. When this bit is set to '1', the RDY# output pin is delayed by three wait states. This setting is for test mode *only*.
4	**Timing Adjust for '486 COMMAND Pin:** This bit should be set to '0' for normal operation. When this bit is set to '1', an additional $\frac{1}{2}$ CPU clock delay is selected for the '486 COMMAND pin. This setting is for test mode *only*.
3	**Divide VCLK by Four:** When this bit is set to '1', the VCLK frequency is divided by four.
2	**OSC Input Disable in Suspend Mode:** When this bit is '1', the oscillator input pad is disabled during Hardware-Controlled Suspend mode, thus turning off internal clocks and their associated power dissipation. This bit should be set to '1' only when an external 32-kHz source (CR1D[4] = '0') is supplied for memory refresh during Suspend mode. When this bit is '0', the oscillator input pad is always enabled.
1	**DRAM Interface-Input Threshold Select:** When this bit is '0', the DRAM interface-input thresholds are set for TTL levels. When this bit is '1', the DRAM interface-input thresholds are set for CMOS levels.
0	**CPU-bus Interface-Input Threshold Select:** When this bit is '0', the CPU-bus interface-input thresholds are set for TTL levels. When this bit is '1', the CPU-bus interface-input thresholds are set for CMOS levels

6.3.12 SR1A: Dual-Scan Color Control

I/O Port Address: 3C5

Index: 1A

Bit	Description	Access	Reset State
7(MSB)	Refresh Per Line Select	R/W	'0'
6	Dual-Scan Color STN Select	R/W	'0'
5	Video Memory/CPU Bandwidth	R/W	'0'
4	Reserved		
3	Reserved		
2	Reserved		
1	Reserved		
0(LSB)	Reserved		

Bit	Description
7	**Refresh per Line Select:** When this bit is set to '1', one refresh cycle per scanline is selected. When this bit is set to '0' (default), register CR11[5] selects three or five refresh cycles per scanline.
6	**Dual-Scan Color STN Select:** When this bit is set to '1', dual-scan color STN mode is selected. Also, register CR1C[7:6] must be programmed to '10' to select color STN panels. If CR1C[7:6] is programmed to other than '10', this bit is a 'don't care'.
5	**Video Memory/CPU Bandwidth:** When this bit is set to '1', the CPU has more access to the memory bus by reducing the FIFO latency. When set to '0', the CPU access uses normal FIFO latency.
4:0	Reserved.

6.3.13 SR1B, SR1C, SR1D, SR1E: VCLK[0, 1, 2, 3] Denominator and Post-scalar Values

I/O Port Address: 3C5

Index: 1B, 1C, 1D, 1E

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	VCLK Denominator 4	R/W	See table below
4	VCLK Denominator 3	R/W	See table below
3	VCLK Denominator 2	R/W	See table below
2	VCLK Denominator 1	R/W	See table below
1	VCLK Denominator 0	R/W	See table below
0(LSB)	VCLK Post-scalar	R/W	See table below

These registers are used in conjunction with SRB–SRE (Section 6.3.5) to establish the frequency of the four possible video clocks. The video clock used is selected by register MISC[3:2]. Each video clock frequency is determined using the following equation:

$$\text{VCLKn frequency} = \frac{OSC \times N}{D \times (P + 1)}$$

Where:

OSC = input clock frequency (14.31818 MHz)
N = numerator = value of bits SRi[6:0], where i = B, C, D, E
D = denominator = value of bits SR1i[5:1], where i = B, C, D, E
P = post-scalar = value of bits SR1i[0], where i = B, C, D, E
If n = 0, then i = B
If n = 1, then i = C
If n = 2, then i = D
If n = 3, then i = E

This register establishes the denominator (*D*) and post-scalar values (*P*). For information on the numerator (*N*) value, see the discussion on registers SRB–SRE (Section 6.3.5).

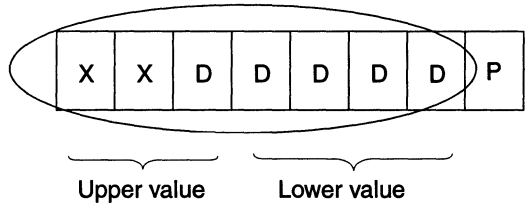
The following table shows the reset values of this register and the other registers that determine the video clock frequency. The table also shows the corresponding video clock frequency at system reset.

6.3.13 SR1B, SR1C, SR1D, SR1E: VCLK[0, 1, 2, 3] Denominator and Post-scalar Values *(cont.)*

Video Clock (VCLKn)	VCLKn Numerator Value			VCLKn Denominator and Post-scalar Value[a]				Reset Freq. (MHz)
	Register (SRi)	At Reset:		Register (SR1i)	At Reset:			
		Register Value (hex)	*N* = Numerator (decimal)		Register Value (hex)	*D* = Denominator (decimal)	*P* = Post-scalar (decimal)[b]	
VCLK0	SRB	66h	102	SR1B	3Bh	29	1	25.180
VCLK1	SRC	5Bh	91	SR1C	2Fh	23	1	28.325
VCLK2	SRD	45h	69	SR1D	30h	24	0	41.165
VCLK3	SRE	7Eh	126	SR1E	33h	25	1	36.082

[a] See discussion below about setting the decimal value of the denominator (*D*) and post-scalar (*P*).

[b] Note that if the post-scalar (*P*) is '1', then the VCO (voltage controlled oscillator) is running at two times the input clock frequency (*OSC*).

Bit	Description
7:6	Reserved
5:1	**VCLK Denominator [4:0]:** These bits determine the denominator value (*D*) used to determine the video clock frequency. For the equation, the post-scalar bit (P) bit is ignored, which has the effect of shifting all bits in the register to the right.  The circled area is what is actually used in the equation. (Upper value = values in XXD. Lower value = values in DDDD.)
0	**VCLK Post-scalar:** This bit determine the post-scalar value (*P*) used to determine the video clock frequency. This bit defines a divide-by-one or divide-by-two operator in the denominator.

6.3.14 SR1F: Memory Clock Frequency Programming

I/O Port Address: 3C5

Index: 1F

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	MCLK Frequency 5	R/W	See table below
4	MCLK Frequency 4	R/W	See table below
3	MCLK Frequency 3	R/W	See table below
2	MCLK Frequency 2	R/W	See table below
1	MCLK Frequency 1	R/W	See table below
0(LSB)	MCLK Frequency 0	R/W	See table below

Bit	Description
7:6	Reserved
5:0	**MCLK Frequency [5:0]:** If the MCLK-frequency values provided by register SRF[1:0] are not sufficient, these bits can directly adjust the frequency of MCLK. These bits adjust the frequency according to the following equation: MCLK frequency = $(OSC \div 8) \times F$ Where: ***OSC*** = input clock frequency (14.318 MHz) ***F*** = frequency factor = value of bits SR1F[5:0] This field can be programmed with any value from 21 to 28 (15h to 1Ch). The MCLK table below provides sample values when a reference *(OSC)* frequency of 14.318 MHz is used.

SR1F[5:0]	*F*	MCLK Frequency (MHz)
15h	21	37.585
17h	23	41.165
19h	25	44.744
1Ah	26	46.534
1Ch	28	50.114

6.3.15 GR9: Offset 0

I/O Port Address: 3CF

Index: 9

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Offset 0 [6]	R/W	'0'
5	Offset 0 [5]	R/W	'0'
4	Offset 0 [4]	R/W	'0'
3	Offset 0 [3]	R/W	'0'
2	Offset 0 [2]	R/W	'0'
1	Offset 0 [1]	R/W	'0'
0(LSB)	Offset 0 [0]	R/W	'0'

This register provides access for up to 512 Kbytes of display memory with 4-Kbyte granularity.

Bit	Description
7	Reserved
6:0	**Offset 0 [6:0]:** This value is added to the system address A[18:12] to provide the address into display memory. This Offset register is selected when GRB[0] = '0', or when GRB[0] = '1' and the system address A[15] = '0'.

The display memory address, prior to being modified by address wrap controls, is called XMA. XMA is the sum of CPU segment bits XA and Offset register bits. XA is the address on the bus, with bits 16 and 15 possibly forced to a '0', as indicated in the following table:

Configuration	XA[16]	XA[15]	XA[14:0]
128K memory: GR6[3:2] = '00'	A[16]	A[15]	A[14:0]
64K memory: GR6[3:2] = '01' ***and*** Offset 1 disabled: GRB[0] = '0'	'0'	A[15]	A[14:0]
64K memory: GR6[3:2] = '01' ***or*** Offset 1 enabled: GRB[0] = '1'	'0'	'0'	A[14:0]

The XA address is summed with the contents of an Offset register with one relative alignment according to the configuration. This is indicated in the mapping that follows:

Table 6-1. 512-Kbyte Memory with 4-Kbyte Granularity and VGA Mapping

CPU Segment Bits	'0'	'0'	XA[16]	XA[15]	XA[14] = A[14]	XA[13] = A[13]	XA[12] = A[12]
Offset register bits	OFF[6]	OFF[5]	OFF[4]	OFF[3]	OFF[2]	OFF[1]	OFF[0]
Display memory address	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

6.3.16 GRA: Offset 1

I/O Port Address: 3CF

Index: A

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Offset 1 [6]	R/W	'0'
5	Offset 1 [5]	R/W	'0'
4	Offset 1 [4]	R/W	'0'
3	Offset 1 [3]	R/W	'0'
2	Offset 1 [2]	R/W	'0'
1	Offset 1 [1]	R/W	'0'
0(LSB)	Offset 1 [0]	R/W	'0'

This register provides access to up to 512 Kbytes of display memory with 4-Kbyte granularity.

Bit	Description
7	Reserved
6:0	**Offset 1 [6:0]:** This value is added to system address A[18:12] to provide the address into display memory. This Offset register is selected when GRB[0] = '1' and the system address A[15] = '1'. If GRB[0] = '0', this register is unused.

For an understanding of Offset registers, see discussion of register GR9 on the preceding page.

6.3.17 GRB: Graphics Controller Mode Extensions

I/O Port Address: 3CF

Index: B

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Enable 8-Byte Data Latches	R/W	'0'
2	Enable Extended Write Modes	R/W	'0'
1	Enable ×8 Addressing	R/W	'0'
0(LSB)	Enable Offset Register 1	R/W	'0'

Bit	Description
7:4	Reserved
3	**Enable 8-byte Data Latches:** If this bit is '1', the display-memory latches are 8 bytes wide, rather than the normal 4. Write mode 1 is selected by writing '01' to GR5[1:0]. If this bit is '0' and GRB[1] = '0' (that is, ×8 addressing is not selected), then Write mode 1 moves 4 latched pixels from display memory, as in normal VGA operation.
2	**Enable Extended Write Modes:** If this bit is '1', the CL-GD6245 will execute Extended mode write. In particular: • **8-Byte Transfer Enabled:** Up to 8 bytes (8 pixels) can be written into display memory for each CPU byte transferred. • **GR5[2] Enabled:** Extended Write modes 4 and 5 can be enabled • **GR0 Extended:** Register GR0 is extended from 4 bits to 8 bits • **GR1 Extended:** Register GR1 is extended from 4 bits to 8 bits • **SR2 Extended:** Register SR2 is extended from 4 bits to 8 bits
1	**Enable ×8 Addressing:** When this bit is '1', the system address is shifted by three relative to true packed-pixel addressing, so that each system-byte address points to a different 8-pixel (8-byte) block in display memory. When this bit is '0', normal addressing is used.
0	**Enable Offset Register 1:** When this bit is '1', then CPU address A[15] will be used to choose between Offset 0 register (GR9) and Offset 1 register (GRA). When this bit is '0', then Offset 0 register (GR9) will always be chosen, regardless of the value of CPU address A[15]. For 1-Mbyte linear addressing, this bit must be set to '0'.

6.3.18 CR19: Interlace End

I/O Port Address: 3?5

Index: 19

Bit	Description	Access	Reset State
7(MSB)	Interlace End 7	R/W	'0'
6	Interlace End 6	R/W	'0'
5	Interlace End 5	R/W	'0'
4	Interlace End 4	R/W	'0'
3	Interlace End 3	R/W	'0'
2	Interlace End 2	R/W	'0'
1	Interlace End 1	R/W	'0'
0(LSB)	Interlace End 0	R/W	'0'

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

This register specifies the ending horizontal character count for the odd-field VSYNC.

Bit	Description
7:0	**Interlace End [7:0]:** This value is the number of characters in the last scanline of the odd field in interlaced timing. This value can be adjusted to center the scanlines in the odd field halfway between scanlines in the even field. Typically, this register is programmed to approximately half the horizontal total.

6.3.19 CR1A: Interlace Control

I/O Port Address: 3?5

Index: 1A

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Enable Double-Buffered Display Start Address	R/W	'0'
0(LSB)	Enable Interlaced	R/W	'0'

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit	Description
7:2	Reserved
1	**Enable Double-Buffered Display Start Address:** If this bit is programmed to a '1', the Display Start address will be updated on the VSYNC that follows a write to Start Address Low. This action provides control of display-frame switching without the need to monitor VSYNC.
0	**Enable Interlaced:** If this bit is programmed to a '1', interlaced timing is enabled (i.e., interlaced sync in Text mode, and interlaced sync and video data in Graphics mode). In addition, IRQ requests are generated only at the end of odd fields, i.e., at the end of a frame. For interlaced sync and data in Graphics mode, the CRTC Scan Double (CR9[7]) must be set to '0'. Graphics modes 4 and 6 must always be non-interlaced.

6.3.20 CR1B: Extended Display Controls

I/O Port Address: 3?5

Index: 1B

Bit	Description	Access	Reset State
7(MSB)	Disable Text Cursor Blink	R/W	'0'
6	Enable Text Mode Fast-Page	R/W	'0'
5	Blanking Control	R/W	'0'
4	Reserved		
3	Reserved		
2	Enable Vertical Blanking Display	R/W	'0'
1	Enable Extended Address Wrap	R/W	'0'
0(LSB)	Extended Display Start Address Bit 16	R/W	'0'

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit	Description
7	**Disable Text Cursor Blink:** Setting this bit to '1' disables the text cursor blink.
6	**Enable Text Mode Fast-Page**: If this bit is set to '0', all font-fetch cycles occur as random-read cycles. This bit must be set to '0' for standard VGA dual-font operation. If this bit is set to '1', Fast-Page Text mode cycles will be used to fetch font data. This allows for text modes with a VCLK greater than 30 MHz, as is required for 132-column modes. (See Section 6.5 at the end of this chapter for more details on 132-column modes).
5	**Blanking Control:** If this bit is set to '0', the DAC blanking will be controlled by the blanking signal generated by the CRTC. In this case, the border can be used (register AR11). If this bit is set to '1', the DAC blanking will be controlled by Display Enable. The DAC will be blanked during the time when the border is normally displayed.
4:3	Reserved
2	**Enable Vertical Blanking Display**: If this bit is set to '0', it selects Vertical Blanking Display Enable, which controls the vertical blanking output from the Display Enable pin (FPDE — pin 95). (This bit setting is used for panels that require 480 vertical lines at all times.) If this bit is set to '1', it enables vertical blanking for TFT-type panels.

6.3.20 CR1B: Extended Display Controls *(cont.)*

Bit	Description
1	**Enable Extended Address Wrap:** If this bit is set to '0', the CL-GD6245 is VGA-compatible for two reasons. First, the display-memory address wraps at 64K maps (256 Kbytes of total memory). Second, the CRT controller Character Address counter is 16 bits. As a result, even with 512-Kbyte-wide memory installed, the Character Address counter does not access the second 256 Kbytes. If this bit is set to a '1', two changes occur. First, the display memory address wraps at the total available memory size. Second, the CRT controller Character Address counter is 17 bits. In addition, the following features become available: a. If this bit is '1' and SR4[3] = '1' (Chain-4 addressing is selected), then DRAM addresses A0 and A1 (which are normally supplied by CPU addresses XMA[14] and XMA[15]) are supplied by CPU addresses XMA[16] and XMA[17]. The XMA[18:12] addresses are the sum of CPU address XA[16:12] and either Offset register (0 or 1). Refer to the description of register bit GR9 for explanations of XMA and XA. b. If this bit is set to a '1' and CR14[6] = '1' (CL-GD6245's CRT controller Double-Word Addressing is selected), then DRAM Addresses A0 and A1(which are normally supplied by CRTC Character Counter addresses CA[12] and CA[13]) are supplied by addresses CA[14] and CA[15]. As a result, mode 13h provides four displayable pages. If four DRAMs are installed, Character Counter address CA[16] is added, allowing a 128-Kbyte displayable page.
0	**Extended Display Start Address Bit 16:** This is bit 16 of the Extended-display Start address.

6.3.21 CR1C: Flat-Panel Interface

I/O Port Address: 3?5

Index: 1C

Bit	Description	Access	Reset State
7(MSB)	LCD Flat Panel Class Select 1	R/W	'0'
6	LCD Flat Panel Class Select 0	R/W	'0'
5	Reserved		
4	Reserved		
3	Protect CRTC Registers for LCD	R/W	'0'
2	MCLK and VCLK Suspend Mode Power-Down	R/W	'0'
1	Invert LLCLK Control	R/W	'0'
0(LSB)	Invert LFS Control	R/W	'0'

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit **Description**

7:6 **LCD Flat Panel Class Select [1:0]:** These two bits select the class of LCD flat panel to be connected. The following table lists available choices:

Bit [7]	Bit [6]	Panel Class Selected
'0'	'0'	Single- or dual-scan/dual-data monochrome panels. CR8X[5] = '0' for dual scan. CR8X[5] = '1' for single scan. UD[3:0] and LD[3:0] = two sets of four shaded pixels with frame modulation.
'0'	'1'	LD[3:0] = one unshaded 4-bit video pixel.
'1'	'0'	STN color panels. SR1A[6] = '0' for single-scan color STN. SR1A[6] = '1' for dual-scan color STN.
'1'	'1'	TFT color panels. CR9X[1:0] determines the setting for a 9-, 12-, or 18-bit color TFT panel. CR1B[2] = '1' for vertical blanking of TFT panel.

5:4 Reserved

6.3.21 CR1C: Flat-Panel Interface *(cont.)*

Bit	Description
3	**Protect CRTC Registers for LCD:** If this bit is set to '1', the CRTC registers are write protected for LCD panel timing. The last data bits written are used for CRTC timing control, and a read/write 'shadow' register is enabled for any subsequent I/O. CRTC registers that are protected are as follows: CR6: [7:0], Vertical Total (protected value is used) CR7: [7,5,2,0], Vertical Overflow bits for total and sync start CR10: [7:0], Vertical Retrace Start (protected value used for CRT Vsync) CR11: [7:0], Vertical Retrace End (protected value used for CRT Vsync) CR15: [7:0], Vertical Blanking Start CR16: [7:0], Vertical Blanking End
2	**MCLK and VCLK Suspend Mode Power-Down:** If this bit is '0', the MCLK and VCLK voltage-controlled oscillators (VCOs) will *not* power down in either Hardware- or Software-Controlled Suspend mode. If this bit is '0', then the SUSPEND input will force LCD and Backlight power-down sequencing, but CPU access is still allowed and the CRT outputs remain active. This mode is actually a 'cover-closed' condition that turns off only the LCD display. If this bit is '1', the MCLK and VCLK VCOs will power down in Hardware-Controlled Suspend mode, but not in Software-Controlled Suspend mode. If this bit is '1' and CR20[3] = '0', then Hardware-Controlled Suspend mode (using the SUSPEND input pin) will power down both the MCLK and VCLK VCOs, and access by the CPU will not be allowed. Software-Controlled Suspend mode (CR20[3] = '1') will force LCD and Backlight power-down sequencing, but CPU access is still allowed.
1	**Invert LLCLK Control:** Setting this bit to '1' inverts the LLCLK signal.
0	**Invert LFS Control:** Setting this bit to '1' inverts the LFS signal.

6.3.22 CR1D: Flat-Panel Display Controls

I/O Port Address: 3?5

Index: 1D

Bit	Description	Access	Reset State
7(MSB)	Enable LCD Timing Registers	R/W	'0'
6	Enable ACTI to Reset Standby Timer	R/W	'0'
5	Enable VGA Access to Reset Standby Timer	R/W	'0'
4	Suspend Mode Clock Source	R/W	'0'
3	Enable ACTI to Reset Backlight Timer	R/W	'0'
2	Enable VGA Access to Reset Backlight Timer	R/W	'0'
1	Enable Automatic Expand	R/W	'0'
0(LSB)	Enable Automatic Centering	R/W	'0'

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit	Description
7	**Enable LCD Timing Registers:** This bit acts as an extra CRTC Index bit. When this bit is '1', it enables read/write of the hidden LCD Timing registers, CR0X through CRBX, which are mapped at the standard CRTC locations. These special registers are used to control LLCLK, LFS, panel data format, and other LCD panel control signals.
6	**Enable ACTI to Reset Standby Timer:** When this bit is set to '1', activity on the ACTI input resets the internal Standby timer.
5	**Enable VGA Access to Reset Standby Timer:** When this bit is set to '1', any valid VGA memory access resets the internal Standby timer.
4	**Suspend Mode Clock Source:** This bit selects the source for the clock used during Suspend mode. If this bit is set to '0', a 32-kHz clock is expected on the CLK32K pin. If this bit is set to '1', the 14.318-MHz clock, required on the input OSC, will be divided by 432 to derive the 32-kHz clock.
3	**Enable ACTI to Reset Backlight Timer:** When this bit is set to '1', activity on the ACTI input resets the Backlight control timer for the LCD.
2	**Enable VGA Access to Reset Backlight Timer:** When this bit is set to '1', any valid VGA memory access resets the Backlight control timer for the LCD.

6.3.22 CR1D: Flat-Panel Display Controls *(cont.)*

Bit	Description
1	**Enable Automatic Expand:** The automatic vertical expansion feature is controlled by the programming of the two sync polarity bits in port MISC[7:6]: '00' = Reserved (Flat panel defaults to '11' condition: 480 lines, graphics only, no vertical expansion) '01' = 400-line/200-line modes (400-line mode is for text only, 200-line mode is for double-scanned graphics only) '10' = 350-line modes (text or graphics) '11' = 480-line mode (graphics only, no vertical expansion) ***Expansion Method for Graphics Modes:*** **200 lines:** A pattern of 2,2,3,2,3,2,2,3 (double-scan and triple-scan) expands 200 lines to 475 lines by expanding every 8 lines to 19 lines. **350 lines:** A pattern of 1,1,2,1,1,2,1,2,1,1,2,1,1,2 (single-scan and double-scan) expands 350 lines to 475 lines by expanding every 14 lines to 19 lines. ***Expansion Method for Text Modes:*** **200 line, 8 × 8 font:** Normal double-scan is applied, and an extra top line and two extra bottom lines are added to each character row (only if Max Row Scan is set for 7 lines). **350 line, 8 × 14 font:** Two extra top lines and three extra bottom lines are added to each character row (only if Max Row Scan is set for 14 lines). **400 line, 8 × 16 font:** An extra top line and two extra bottom lines are added to each character row (only if Max Row Scan is set for 16 lines).
0	**Enable Automatic Centering:** Setting this bit to '1' shifts LCD centering if the auto-expand bit CR1D[1] is '0' (based on sync polarities). This uses the alternate LFS (Line-Frame Start) timing as programmed in LCD Timing registers CR2X, CR3X, CR4X, CR5X, and CR6X.

6.3.23 CR1E: Flat-Panel Shading

I/O Port Address: 3?5

Index: 1E

Bit	Description	Access	Reset State
7(MSB)	Shade Mapping 1	R/W	'0'
6	Shade Mapping 0	R/W	'0'
5	Reverse Video for Text Modes	R/W	'0'
4	Reverse Video for Graphics Modes	R/W	'0'
3	Maximum Generated Grayshades 1	R/W	'0'
2	Maximum Generated Grayshades 0	R/W	'0'
1	Contrast Enhancement	R/W	'0'
0(LSB)	Enable Planar Graphics Mode Dithering	R/W	'0'

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit — **Description**

7:6 **Shade Mapping [1:0]:** These two bits are used to program monochrome gray-scale mapping (shading) according to the following table:

Bit[7]	Bit[6]	Shade Map
'0'	'0'	18-bit output of LUT converted to 64 shades, with NTSC weighting
'0'	'1'	Green output of LUT only; 6-bit output converted to 64 shades
'1'	'0'	Direct display pixel data (4-bit planar, or lower 6-of-8 bits packed pixel) to 16 or 64 shades
'1'	'1'	6-bit output of Attribute Controller converted to 64 shades

5 **Reverse Video for Text Modes:** If this bit is set to '1', all text modes are displayed in reverse video.

4 **Reverse Video for Graphics Modes:** If this bit is set to '1', all graphics modes are displayed in reverse video.

3:2 **Maximum Generated Grayshades [1:0]:** With these two bits, grayshades are generated according to the following tables:

Table 6-2. CR1C[7:6] = '00' — Monochrome Grayshades

CR1E[3]	CR1E[2]	Number of Shades for Monochrome	
'0'	'0'	16	16 frame with no dithering
'0'	'1'	64	4 frame × 16 dithering[a]
'1'	'0'	64	8 frame × 8 dithering[a]
'1'	'1'	64	16 frame × 4 dithering

[a] Must set CR1E[1] = '1' and CR8X[7] = '1'.

6.3.23 CR1E: Flat-Panel Shading *(cont.)*

Bit — **Description**

3:2*(cont.)* **Maximum Generated Grayshades [1:0]** *(cont.)*:

Table 6-3. CR1C[7:6] = '10' — STN Color

CR1E[3]	CR1E[2]	Number of Colors per Gun	
'0'	'0'	16	16 frame modulation only (4096 colors)
'0'	'1'	64	4 frame × 16 dithering (64 text, 256K graphics)
'1'	'0'	64	8 frame × 8 dithering (512 text, 256K graphics)
'1'	'1'	64	16 frame × 4 dithering (4096 text, 256K graphics)

NOTE: More dithering options are available with CR9X[3:2].

1 **Contrast Enhancement:** This bit is used along with CR8X[4] to enable text-mode contrast enhancement.

CR1E[1]	CR8X[4]	Enhancement Characteristics
'0'	'0'	No enhancement
'0'	'1'	Foreground-only enhancement If BG > FG then BGC = BG; FGC = '0' If BG < FG then BGC = BG; FGC = '1'
'1'	'0'	Foreground and contrast enhancement If BG > FG then BGC = BG; FGC = '0' If BG< FG then BGC = '0'; FGC = FG

BG = Background, FG = Foreground, xxC = Color

0 **Enable Planar Graphics Mode Dithering**: This bit is set to '0' to disable dithering in Non-Packed-Pixel Graphics mode.

6.3.24 CR1F: Flat-Panel Modulation Control

I/O Port Address: 3?5

Index: 1F

Bit	Description	Access	Reset State
7(MSB)	Internal or External Modulation Control	R/W	'0'
6	MOD or Retrace LLCLK Control 6	R/W	'0'
5	MOD or Retrace LLCLK Control 5	R/W	'0'
4	MOD or Retrace LLCLK Control 4	R/W	'0'
3	MOD or Retrace LLCLK Control 3	R/W	'0'
2	MOD or Retrace LLCLK Control 2	R/W	'0'
1	MOD or Retrace LLCLK Control 1	R/W	'0'
0(LSB)	MOD or Retrace LLCLK Control 0	R/W	'0'

NOTES: 1) The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.
2) A value ***must*** be programmed into this register.

This register is used to control the characteristics of the Modulation (MOD) signal for the flat panel. This function is useful for those dual-scan flat panels that generate the MOD signal based on the number of LLCLKs that appear during retrace on the lower half of the panel. When using single-scan panels, using these bits will increase the line clock count for the entire panel.

Bit	Description
7	**Internal or External Modulation Control:** This bit controls the source of the modulation signal (MOD) for the flat panel. If this bit is '0', the external modulation signal is selected for the flat panel. In this case, bits 6:0 of this register can select up to 128 scanlines before the MOD signal changes polarity. If this bit is '1', the internal modulation signal is provided through the MOD pin to the flat panel. In this case, the total number of LLCLKs is determined by this register (see bits 6:0 below).
6:0	**MOD or Retrace LLCLK Control [6:0]:** If bit 7 is '0', then these bits select up to 128 scanlines before the MOD signal changes polarity. If bit 7 is '1', then the total number of LLCLKs is determined by adding the content of these bits 6:0 in this register to 180h (or 384 decimal) as follows: Number of LLCLKs = 180h + (value of bits 6:0)h

6.3.25 CR20: Power Management

I/O Port Address: 3?5

Index: 20

Bit	Description	Access	Reset State
7(MSB)	Enable STANDBY	R/W	'0'
6	CRT Enable	R/W	'0'
5	LCD Enable	R/W	'0'
4	Activate Standby Mode	R/W	'0'
3	Activate Suspend Mode	R/W	'0'
2	Refresh Select 1	R/W	'0'
1	Refresh Select 0	R/W	'0'
0(LSB)	Text Mode Shading Control	R/W	'0'

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit	Description
7	**Enable STANDBY:** When this bit is set to '1', the STANDBY I/O pin becomes an *output* used to indicate the status of Standby mode: the STANDBY pin is low when the CL-GD6245 is in Standby mode. When this bit is set to '0', the STANDBY pin is an *input* that when high initiates the Standby mode.
6	**CRT Enable:** Setting this bit to '1' enables the analog output from the video DAC.
5	**LCD Enable:** This bit must be set to '1' to enable the LCD interface. Unlike the Standby mode, when the LCD is disabled, VCLK is still running and with normal power operation. Transitions of this bit cause the panel power-up (low-to-high) and power-down (high-to-low) sequence to occur starting from VCLK or up to the point of VCLK shutdown. That is, the panel bias, backlight, logic supply, and drive signals become enabled or disabled. When this bit is '1', the Line Frame Signal (LFS) and LCD Line Clock (LLCLK) LCD Timing signals for monochrome panels are generated. These bits are generated from the LCD Timing registers CR0X through CRBX. For TFT color panels, the CRTC-programmed sync timing is used. Also, VSYNC and HSYNC signals are sent to the CRT outputs and to the LFS and LLCLK outputs. In addition, when LCD operation is enabled, the Display Enable signal controls the display data. Therefore, border is *not* supported.

6.3.25 CR20: Power Management *(cont.)*

Bit | **Description**

5 *(cont.)* When this bit is '1', some of the VGA register bits are redefined for LCDs as follows:

SR1, SR2, SR3 VCLK/2: The LCD always gets a shift clock at $^1/_4$ the VCLK rate. This bit selects the horizontally locked timing for 40- or 80-column modes (except for mode 13h).

SR1[0] 8/9 Dot Characters: 'Locked' and set for 8-dots/character.

AR13: Pixel Panning: If SR1[0] is '0', then the effect of AR13[4] is masked, and a value of either '8h' or '0h' is equal to 'no shift'.

MISC Output (3C2): CRT Sync Polarity will always be negative/negative. Sync polarity bits control Vertical Expansion/Vertical Centering.

NOTE: Clock Select bits do not need to be locked. All the clock programming registers should be set to produce the same frequency (as required by the LCD).

4 **Activate Standby Mode:** Setting this bit to '1' overrides the current internal Standby timer setting and immediately places the device into Standby mode.

3 **Activate Suspend Mode:** Setting this bit to '1' initiates Software-Controlled Suspend mode. In this mode, the power-down sequence is started to blank the panel, but the CPU can still access video memory, RAMDAC, and I/O registers. Note that setting this bit is '0', enables the Hardware-Controlled Suspend mode (using the SUSPEND input pin).

NOTE: Hardware-Controlled Suspend mode also requires CR1C[2] to be '1'.

2:1 **Refresh Select [1:0]:** The programming of these two bits control the type of refresh applied to the video DRAMs during Suspend mode as follows.

Bit [2]	Bit [1]	Refresh Type
'0'	'0'	8-ms refresh cycle, CAS*-before-RAS* refresh.
'0'	'1'	64-ms refresh cycle, CAS*-before-RAS* refresh.
'1'	'0'	Self-refresh.
'1'	'1'	No refresh. All clocks inputs are disabled, and RAS*/CAS* outputs are 'high'.

0 **Text Mode Shading Control:** If this bit is set to '0', text shades are derived directly from foreground/background data. If this bit is set to '1', text shades are derived in the same way that graphics shades are derived, that is, using CR1E[7:6].

6.3.26 CR21: Power-Down Timer Control

I/O Port Address: 3?5

Index: 21

Bit	Description	Access	Reset State
7(MSB)	Timer for Backlight Control (FPBACK) 3	R/W	'0'
6	Timer for Backlight Control (FPBACK) 2	R/W	'0'
5	Timer for Backlight Control (FPBACK) 1	R/W	'0'
4	Timer for Backlight Control (FPBACK) 0	R/W	'0'
3	Timer for Standby Mode Control 3	R/W	'0'
2	Timer for Standby Mode Control 2	R/W	'0'
1	Timer for Standby Mode Control 1	R/W	'0'
0(LSB)	Timer for Standby Mode Control 0	R/W	'0'

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

These two 4-bit timer fields determine the countdown times before the backlight powers off and Standby mode begins. Both 4-bit timer fields are set with values from 1 (1h) to 15 (Fh), corresponding to approximately 1 to 15 minutes. A value of 0h disables each timer. The exact countdown times for each timer are determined as follows:

Countdown time = (field value x 64 sec.) – 32 sec.

Therefore, a setting of 15 (Fh) results in an actual time of 15 minutes 28 seconds. See the table below for typical timer settings.

Bit	Description
7:4	**Timer for Backlight Control (FPBACK) [3:0]:** This is the programmed value for the internal Backlight timer. (The backlight can be programmed to power off without the CL-GD6245 being in Standby mode.) Countdown time = (value x 64 sec.) – 32 sec.
3:0	**Timer for Standby Mode Control [3:0]:** This is the programmed value for the internal Standby-mode timer. Countdown time = (value x 64 sec.) – 32 sec.

Table 6-4. Typical Backlight and Standby Timer Settings

Backlight Control Bits				Value in Hex	Exact Delay Programmed (Seconds)	Approximate Delay (Minutes)
[7]	[6]	[5]	[4]			
Standby Control Bits						
[3]	[2]	[1]	[0]			
'0'	'0'	'0'	'0'	0h	disabled	disabled
'0'	'0'	'0'	'1'	1h	32	0.5
'0'	'1'	'0'	'1'	5h	288	4.8
'0'	'1'	'1'	'1'	7h	416	6.9
'1'	'0'	'1'	'0'	Ah	608	10.1
'1'	'1'	'1'	'1'	Fh	928	15.5

6.3.27 CR23: FPVCC/FPBACK Control and SUSPEND Timer

I/O Port Address: 3?5

Index: 23

Bit	Description	Access	Reset State
7(MSB)	SUSPEND Input Debounce Timer 3	R/W	'0'
6	SUSPEND Input Debounce Timer 2	R/W	'0'
5	SUSPEND Input Debounce Timer 1	R/W	'0'
4	SUSPEND Input Debounce Timer 0	R/W	'0'
3	FPBACK Control Override	R/W	'0'
2	FPBACK Output State	R/W	'0'
1	FPVCC Control Override	R/W	'0'
0(LSB)	FPVCC Output State	R/W	'0'

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit	Description
7:4	**SUSPEND Input Debounce Timer [3:0]:** These bits define the number of seconds the SUSPEND input must remain active (either high or low as defined by SR8[3]) and stable before the device can enter Hardware-Controlled Suspend mode. Set for 1 to 15 seconds in 1-second increments. A '0000' setting disables the debounce function, as well as Hardware-Controlled Suspend mode.
3	**FPBACK Control Override:** Setting this bit to '1' overrides the FPBACK Standby mode and enables CR23[2] to control the output state of FPBACK.
2	**FPBACK Output State:** If CR23[3] is '1', then this bit defines the '1' or '0' output state of FPBACK.
1	**FPVCC Control Override:** Setting this bit to '1' overrides the FPVCC Standby mode and enables CR23[0] to control the output state of FPVCC.
0	**FPVCC Output State:** If CR23[1] is '1', then this bit defines the '1' or '0' output state of FPVCC.

6.3.28 CR25: Part Status

I/O Port Address: 3?5

Index: 25

Bit	Description	Access	Reset State
7(MSB)	Part Status Value 7	R	'0'
6	Part Status Value 6	R	'0'
5	Part Status Value 5	R	'0'
4	Part Status Value 4	R	'0'
3	Part Status Value 3	R	'0'
2	Part Status Value 2	R	'0'
1	Part Status Value 1	R	'0'
0(LSB)	Part Status Value 0	R	'0'

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

This read-only register is used for factory testing and internal tracking. Application programs should not depend on a contents read from this register.

Bit	Description
7:0	**Part Status Value [7:0]:** These bits are used only for factory testing and internal tracking.

6.3.29 CR27: Chip ID

I/O Port Address: 3?5

Index: 27

Bit	Description	Access	Reset State
7(MSB)	Chip ID 7	R	'0'
6	Chip ID 6	R	'0'
5	Chip ID 5	R	'0'
4	Chip ID 4	R	'1'
3	Chip ID 3	R	'0'
2	Chip ID 2	R	'1'
1	Chip ID 1	R	'1'
0(LSB)	Chip ID 0	R	'0'

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

This read-only register returns a value that uniquely identifies the CL-GD6245 chip.

Bit	Description
7:0	**Chip ID [7:0]:** This 8-bit field reads the value 16h, which uniquely identifies the CL-GD6245 chip.

6.3.30 CR29: Part Configuration

I/O Port Address: 3?5

Index: 27

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	32-kHz Clock Status	R	See description below
5	Power-Up/-Down Cycling Activity	R	See description below
4	NPD Input Status	R	See description below
3	DRAM Type Selected	R	See description below
2	Local Bus Type 1 (LBT1) Status	R	See description below
1	Local Bus Type 0 (LBT0) Status	R	See description below
0	ISA/Local Bus (BUSCONF*) Status	R	See description below

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

This read-only register reflects the configuration of the chip interfaces after reset is completed.

Bit	Description
7	Reserved
6	**32-kHz Clock Status:** This bit reflects the state of the 32-kHz clock signal. This bit's status is determined by the input to the CLK32K pin (pin 73).
5	**Power-Up/-Down Cycling Activity:** This bit is '1' during a power-up or power-down sequence. It can be read in all modes except Hardware-Controlled Suspend mode, which locks out access to all registers.
4	**NPD Input Status**: When the NPD pin is high, this bit is '1', indicating that the internal Standby and Backlight power-down timers are disabled. This bit's status is determined by the input to the NPD pin (pin 76). If AC power is present, this bit is '1'.
3	**DRAM Type Selected**: This bit's status is determined by the input to the DUALCAS pin (pin 78). When the DUALCAS pin is low, this bit is '0', indicating dual-WE*-type DRAMs are selected. When the DUALCAS pin is high, this bit is '1', indicating dual-CAS*-type DRAMs are selected.
2	**Local Bus Type 1 (LBT1) Status**: This bit's status is determined by the input to the LBT1 pin (pin 168). The LBT1 pin is used with LBT0 and BUSCONF* pins to determine the CPU bus type (see Table 6-5, which follows). When an ISA bus is configured, this bit is a 'don't care'. If local buses are used, this bit is '1' if LBT1 is tied to BVDD1, and this bit is '0' if LBT1 is tied to ground.

6.3.30 CR29: Part Configuration *(cont.)*

Bit	Description
1	**Local Bus Type 0 (LBT0) Status**: This bit's status is determined by the input to the LBT0 pin (pin 169). The LBT0 pin is used with LBT1 and BUSCONF* pins to determine the CPU bus type (see Table 6-5). When an ISA bus is used, this bit is a 'don't care'. If local buses are used, this bit is '1' if LBT0 is tied to BVDD1 and this bit is '0' if LBT0 is tied to ground.
0	**ISA/Local Bus (BUSCONF*) Status**: This bit's status is determined by the input to the BUSCONF* pin (pin 72). The BUSCONF* pin is used with LBT1 and LBT0 pins to determine the CPU bus type (see Table 6-5). This bit is '1' if BUSCONF* is tied to BVDD1, and this bit is '0' if BUSCONF* is tied to ground.

Table 6-5. Status of CR29[2:0] for Bus Types

CR29[2] (LBT1)	CR29[1] (LBT0)	CR29[0] (BUSCONF*)	Bus Type
X	X	'1'	ISA bus
'0'	'1'	'0'	'386SX
'1'	'0'	'0'	'386DX
'1'	'1'	'0'	'486SX/DX or VESA® VL-Bus™

6.4 LCD Timing Registers

6.4.1 CR0X: Horizontal Total for 80-Column Display and Display Mode 13h

I/O Port Address: 3?5

Index: 0 — This register is accessible only when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS
6	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS
5	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS
4	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS
3	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS
2	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS
1	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS
0(LSB)	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit	Description
7:0	**Horizontal Total for 80-Column Display:** When CR1X[7] is '1', this register defines the horizontal total of an 80-column display. When CR1X[7] is '0', this register can be used as a scratchpad register. This register controls horizontal LCD flat-panel timing when SR1[3] is '0' or GR5[6] is '1'.

6.4.2 CR1X: Horizontal Total for 40-Column Display

I/O Port Address: 3?5

Index: 1 — This register is accessible only when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	Horizontal Total Enable	R/W	n/a — Set by BIOS
6	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS
5	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS
4	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS
3	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS
2	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS
1	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS
0(LSB)	Horizontal Total/Scratchpad	R/W	n/a — Set by BIOS

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit	Description
7	**Horizontal Total Enable**: When this bit is '1', CR0X[7:0] defines the horizontal total for an 80-column display, and CR1X[6:0] defines the horizontal total for a 40-column display. When this bit is '0', CR0X[7:0] and CR1X[6:0] can be used as scratchpad bits.
6:0	**Horizontal Total for 40-Column Display:** When CR1X[7] is '1', these 7 bits define the Horizontal Total of a 40-column display. When CR1X[7] is '0', these seven bits can be used as scratchpad bits. These bits control horizontal LCD flat-panel timing when SR1[3] is '1' (that is, when VCLK, the master clock, is divided by two to generate DCLK, the dot clock) and when GR5[6] is '0' (that is, when the video data shift registers are controlled for 16-, 4-, or 2-color video modes).

6.4.3 CR2X: LFS Vertical Counter Value Compare (MISC[7:6] = '11')

I/O Port Address: 3?5

Index: 2 — This register is accessible only when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	LFS Vert. Counter Value 7	R/W	n/a — Set by BIOS
6	LFS Vert. Counter Value 6	R/W	n/a — Set by BIOS
5	LFS Vert. Counter Value 5	R/W	n/a — Set by BIOS
4	LFS Vert. Counter Value 4	R/W	n/a — Set by BIOS
3	LFS Vert. Counter Value 3	R/W	n/a — Set by BIOS
2	LFS Vert. Counter Value 2	R/W	n/a — Set by BIOS
1	LFS Vert. Counter Value 1	R/W	n/a — Set by BIOS
0(LSB)	LFS Vert. Counter Value 0	R/W	n/a — Set by BIOS

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

This register defines the number of scanlines that data is delayed, as measured from the line frame start. These bits are the least-significant 8 bits of a 10-bit value. The most-significant 2 bits are stored in register CR6X[7:6].

Bit	Description
7:0	**LFS Vertical Counter Value [7:0]:** This register is used when 480-vertical-line display mode is selected (MISC[7:6] = '11'). That is, neither 350-vertical-line mode with Automatic Centering (used with register CR3X) nor 400-vertical-line mode with Automatic Centering (used with register CR4X) is selected.

6.4.4 CR3X: LFS Vertical Counter Value Compare (MISC[7:6] = '10')

I/O Port Address: 3?5

Index: 3 — This register is accessible only when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	LFS Vert. Counter Value 7	R/W	n/a — Set by BIOS
6	LFS Vert. Counter Value 6	R/W	n/a — Set by BIOS
5	LFS Vert. Counter Value 5	R/W	n/a — Set by BIOS
4	LFS Vert. Counter Value 4	R/W	n/a — Set by BIOS
3	LFS Vert. Counter Value 3	R/W	n/a — Set by BIOS
2	LFS Vert. Counter Value 2	R/W	n/a — Set by BIOS
1	LFS Vert. Counter Value 1	R/W	n/a — Set by BIOS
0(LSB)	LFS Vert. Counter Value 0	R/W	n/a — Set by BIOS

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

This register defines the number of scanlines that data is delayed, as measured from the line frame start. These bits are the least-significant 8 bits of a 10-bit value. The most-significant 2 bits are stored in register CR6X[5:4].

Bit	Description
7:0	**LFS Vertical Counter Value [7:0]**: This register is used when 350-vertical-line display mode is selected (MISC[7:6] = '10') and Automatic Centering is selected (CR1D[0] = '1'). Note that, when this register is used, Automatic Expand must be disabled (CR1D[1] = '0').

6.4.5 CR4X: LFS Vertical Counter Value Compare (MISC[7:6] = '01')

I/O Port Address: 3?5

Index: 4 — This register is accessible only when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	LFS Vert. Counter Value 7	R/W	n/a — Set by BIOS
6	LFS Vert. Counter Value 6	R/W	n/a — Set by BIOS
5	LFS Vert. Counter Value 5	R/W	n/a — Set by BIOS
4	LFS Vert. Counter Value 4	R/W	n/a — Set by BIOS
3	LFS Vert. Counter Value 3	R/W	n/a — Set by BIOS
2	LFS Vert. Counter Value 2	R/W	n/a — Set by BIOS
1	LFS Vert. Counter Value 1	R/W	n/a — Set by BIOS
0(LSB)	LFS Vert. Counter Value 0	R/W	n/a — Set by BIOS

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

This register defines the number of scanlines that data is delayed, as measured from the line frame start. These bits are the least-significant 8 bits of a 10-bit value. The most-significant 2 bits are stored in register CR6X[3:2].

Bit	Description
7:0	**LFS Vertical Counter Value [7:0]:** This register is used when 400-vertical-line display mode is selected (MISC[7:6] = '01') and Automatic Centering is selected (CR1D[0] = '1'). Note that Automatic Expand must be disabled (CR1D[1] = '0').

6.4.6 CR5X: LFS Vertical Counter Value Compare (MISC[7:6] = '00')

I/O Port Address: 3?5

Index: 5 — This register is accessible only when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	LFS Vert. Counter Value 7	R/W	n/a — Set by BIOS
6	LFS Vert. Counter Value 6	R/W	n/a — Set by BIOS
5	LFS Vert. Counter Value 5	R/W	n/a — Set by BIOS
4	LFS Vert. Counter Value 4	R/W	n/a — Set by BIOS
3	LFS Vert. Counter Value 3	R/W	n/a — Set by BIOS
2	LFS Vert. Counter Value 2	R/W	n/a — Set by BIOS
1	LFS Vert. Counter Value 1	R/W	n/a — Set by BIOS
0(LSB)	LFS Vert. Counter Value 0	R/W	n/a — Set by BIOS

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

This register defines the number of scanlines that data is delayed, as measured from the line frame start. These bits are the least-significant 8 bits of a 10-bit value. The most-significant 2 bits are stored in register CR6X[1:0].

Bit	Description
7:0	**LFS Vertical Counter Value [7:0]**: This register is used when MISC[7:6] is '00'. In this case, the flat panel defaults to the '11' condition on MISC[7:6], which is used when 480-vertical-line display mode is selected.

6.4.7 CR6X: LFS Vertical Counter Value Compare Overflow

I/O Port Address: 3?5

Index: 6 — This register is accessible only when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	LFS Vert. Counter Value 9 for CR2X	R/W	n/a — Set by BIOS
6	LFS Vert. Counter Value 8 for CR2X	R/W	n/a — Set by BIOS
5	LFS Vert. Counter Value 9 for CR3X	R/W	n/a — Set by BIOS
4	LFS Vert. Counter Value 8 for CR3X	R/W	n/a — Set by BIOS
3	LFS Vert. Counter Value 9 for CR4X	R/W	n/a — Set by BIOS
2	LFS Vert. Counter Value 8 for CR4X	R/W	n/a — Set by BIOS
1	LFS Vert. Counter Value 9 for CR5X	R/W	n/a — Set by BIOS
0(LSB)	LFS Vert. Counter Value 8 for CR5X	R/W	n/a — Set by BIOS

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

This register defines the most-significant two bits for the LFS Vertical Counter Value Compare registers.

Bit	Description
7:6	**LFS Vert. Counter Value 9:8 for CR2X:** When MISC[7:6] = '11', these bits are appended as the most-significant two bits of register CR2X, creating a 10-bit value.
5:4	**LFS Vert. Counter Value 9:8 for CR3X:** When MISC[7:6] = '10', these bits are appended as the most-significant two bits of register CR3X, creating a 10-bit value.
3:2	**LFS Vert. Counter Value 9:8 for CR4X:** When MISC[7:6] = '01', these bits are appended as the most-significant two bits of register CR4X, creating a 10-bit value.
1:0	**LFS Vert. Counter Value 9:8 for CR5X:** When MISC[7:6] = '00', these bits are appended as the most-significant two bits of register CR5X, creating a 10-bit value.

6.4.8 CR7X: Panel Signal Control for Color TFT Panels

I/O Port Address: 3?5

Index: 7 — This register is accessible only when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	Enable Standby/Suspend in CRT-Only	R/W	n/a — Set by BIOS
6	Reserved		
5	Reserved		
4	Reserved		
3	LFS Output	R/W	n/a — Set by BIOS
2	LLCLK Output	R/W	n/a — Set by BIOS
1	FPVDCLK Inversion	R/W	n/a — Set by BIOS
0(LSB)	FPVDCLK Enable	R/W	n/a — Set by BIOS

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit	Description
7	**Enable Standby/Suspend in CRT-Only:** When this bit is '1', Standby and Suspend modes are available in CRT-only mode, as well as LCD-only mode. When this bit is '0', Standby and Suspend modes are available only in LCD-only mode. (This bit does not affect the availability of Standby and Suspend in SimulSCAN.)
6:4	Reserved
3	**LFS Output:** When this bit is '0', the LFS output pin drives STN panels and DE-type TFT panels. When this bit is '1', the LFS output pin drives the VSYNC input for non-DE-type TFT panels.
2	**LLCLK Output:** When this bit is '0', the LLCLK output pin drives STN panels and DE-type TFT panels. When this bit is '1', the LLCLK output pin drives the HSYNC input for non-DE-type TFT panels.
1	**FPVDCLK Inversion:** When this bit is '1', the FPVDCLK is inverted, allowing panel data to be latched on the low-to-high transition of FPVDCLK. When this bit is '0', panel data is latched on the high-to-low transition of FPVDCLK.
0	**FPVDCLK Enable:** When this bit is '0', the FPVDCLK is gated by display enable, and it remains active only during display time. When this bit is '1', FPVDCLK is always active, which is required for most TFT panels.

6.4.9 CR8X: STN Color Panel Data Format

I/O Port Address: 3?5

Index: 8 — This register is accessible only when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	Alternate Grayscale Mode Select	R/W	n/a — Set by BIOS
6	Reserved		
5	Dual- or Single-Scan Mono. Panel Select	R/W	n/a — Set by BIOS
4	Foreground Text Enhancement	R/W	n/a — Set by BIOS
3	Line-Pulse Width Select	R/W	n/a — Set by BIOS
2	Dithering Option Select	R/W	n/a — Set by BIOS
1	Shift-Clock Select for STN Panels	R/W	n/a — Set by BIOS
0(LSB)	16- or 8-Bit Data Interface Select	R/W	n/a — Set by BIOS

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit — **Description**

7 — **Alternate Grayscale Mode Select:** When this bit is '1', the 'alternate' grayscale mode for monochrome panels is selected. This bit is '0' for normal operation.

6 — Reserved

5 — **Dual- or Single-Scan Monochrome Panel Select:** When this bit is '0', a dual-scan monochrome panel is selected. When this bit is '1', a single-scan monochrome panel is selected. This bit is valid only if CR1[7:6] = '00'.

4 — **Foreground Text Enhancement:** When this bit is '1', the foreground text enhancement is enabled (see CR1E[1] for details). When this bit is '0', normal text is displayed.

3 — **Line-Pulse Width Selection:** When this bit is '1' and CR7X[2] is '0', a shortened line-pulse width is selected. When this bit is '0', line-pulse width is controlled by other registers.

CR7X[2]	CR8X[3]	Line-Pulse Width Option
'0'	'0'	120-ns pulse
'0'	'1'	320-ns fixed pulse width = 1 character clock
'1'	'0'	1.8-µs fixed pulse width = 4 character clocks

2 — **Dithering Option Select:** When this bit is '0', use line counter bits 1:0. When this bit is '1', use line counter bits 5:4.

1 — **Shift-Clock Select for STN Panels:** When this bit is '0', a single-shift clock is supplied to an STN panel's FPVDCLK pin. When this bit is '1', dual-shift clocks are supplied to an STN panel's FPVDCLK pin. Setting this bit to '1' is all that is necessary to drive 8-bit, dual-clock STN panels.

0 — **16- or 8-Bit Data Interface Select:** When this bit is '0', 16-bit data interface is selected. Set this bit to '1' only to drive 8-bit, single-clock STN panels.

6.4.10 CR9X: TFT Panel Data Format

I/O Port Address: 3?5

Index: 9 — This register is accessible only when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Shift-Clock Delay 2	R/W	n/a — Set by BIOS
5	Shift-Clock Delay 1	R/W	n/a — Set by BIOS
4	Shift-Clock Delay 0	R/W	n/a — Set by BIOS
3	Dithering Option 1	R/W	n/a — Set by BIOS
2	Dithering Option 0	R/W	n/a — Set by BIOS
1	TFT-Panel Data Format 1	R/W	n/a — Set by BIOS
0(LSB)	TFT-Panel Data Format 0	R/W	n/a — Set by BIOS

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit — **Description**

7 — Reserved

6:4 — **Shift-Clock Delay [2:0]:** These bits select a 0-to-7-pixel shift clock delay from the internal character clock counter (8 VCLKs per character clock) to the TFT HSYNC (LLCLK) signal. Increasing this value moves the image on the LCD to the left.

3:2 — **Dithering Option [1:0]:** These bits select dithering options as follows:

CR8X[7]	CR1E[3]	CR1E[2]	CR1E[0]	CR9X[3]	CR9X[2]	Option Selected
0	0	0	X	X	X	16 frame mod., no dithering
0	1	1	1	0	0	16 frame mod. x4 dithering
0	1	1	1	0	1	16 frame mod. x2 dithering
1	1	0	0	X	X	8 frame mod., no dithering
1	1	0	1	0	0	8 frame mod. x8 dithering
1	1	0	1	0	1	8 frame mod. x4 dithering
1	1	0	1	1	1	8 frame mod. x2 dithering
1	0	1	0	X	X	4 frame mod., no dithering
1	0	1	1	0	0	4 frame mod. x16 dithering
1	0	1	1	0	1	4 frame mod. x8 dithering
1	0	1	1	1	1	4 frame mod. x4 dithering

1:0 — **TFT-Panel Data Format [1:0]**: These two bits select the data format for the TFT panels as shown in the table below. See the "Panel Interface Tables" section in the *CL-GD6245 Applications Book* for specific panel types and connection information.

CR9X[1:0]	TFT Panel Data Format
'00'	9-bit (333)
'10'	12-bit (444)
'X1'	18-bit direct (666)

6.4.11 CRAX: TFT Panel HSYNC Position Control

I/O Port Address: 3?5

Index: A — This register is accessible only when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	TFT-Panel HSYNC Counter 7	R/W	n/a — Set by BIOS
6	TFT-Panel HSYNC Counter 6	R/W	n/a — Set by BIOS
5	TFT-Panel HSYNC Counter 5	R/W	n/a — Set by BIOS
4	TFT-Panel HSYNC Counter 4	R/W	n/a — Set by BIOS
3	TFT-Panel HSYNC Counter 3	R/W	n/a — Set by BIOS
2	TFT-Panel HSYNC Counter 2	R/W	n/a — Set by BIOS
1	TFT-Panel HSYNC Counter 1	R/W	n/a — Set by BIOS
0(LSB)	TFT-Panel HSYNC Counter 0	R/W	n/a — Set by BIOS

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit	Description
7:0	**TFT-Panel HSYNC Counter [7:0]:** This register contains the 8-bit horizontal-counter value for generating the HSYNC output. This register is set in multiples of eight VCLKs (80-column character clocks). Increasing the value in this register moves the image on the LCD to the left. Note that bit 7 of this register is AND'ed with SR1[3] to delay the TFT-panel HSYNC counter by one character clock.

6.4.12 CRBX: Special Functions

I/O Port Address: 3?5

Index: B — This register is accessible only when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Disable Grayshades 7 and 9	R/W	'0'
3	Disable Grayshades 5 and 11	R/W	'0'
2	Reserved		
1	Reserved		
0(LSB)	Reserved		

NOTE: The '?' in the above register address is 'B' in monochrome mode and 'D' in color mode.

Bit	Description
7:5	Reserved
4	**Disable Grayshades 7 and 9:** For unacceptable shades, set this bit to '1' to disable shades 7 and 9.
3	**Disable Grayshades 5 and 11:** For unacceptable shades, set this bit to '1' to disable shades 5 and 11.
2:0	Reserved

6.5 132-Column Alphanumeric Mode

This extended video mode is for the CRT display only. It is selected by setting CR1B[6] to '1'. For a 31.5-kHz HSYNC rate, the video dot clock (VCLK) should be set to 41.164 MHz (registers SRB/C/D/E). The Sequencer is programmed for 8-dot character intervals with a non-divided dot clock.

The Character Map(s), SR3[5:0], should be loaded while the 132-column alphanumeric mode is selected because the memory organization of the Character Maps differs from the normal VGA case. Loading the Character Maps requires no special address translation because the CL-GD6245 re-maps video memory automatically when this mode is selected.

The Character Maps should be loaded by unchained (sequential) addressing, with the CL-GD6245 mapped into system address segment A0000 for 64-Kbyte locations, and with the Sequencer Map Mask register programmed to enable writing to Plane 2 (SR2[2] = '1'). Subsequently, the Sequencer Map Mask registers should be programmed for Chain-2 Addressing with Planes 0 and 1 enabled (SR2[1] and SR2[0] are both set to '1'), as is normally the case in an alphanumeric mode.

The 132-column alphanumeric mode does not support simultaneous display of two different character maps, as determined by character attribute bit 3 in the normal VGA operation. However, by programming the Sequencer Character Map Select register SR3[2:0] with a Character Map number, one of eight Character Maps can be selected for the entire screen display. The Character Map number represents one 8-Kbyte segment of the total available 64 Kbytes of Character Maps in this mode. Each Character Map number corresponds to an 8-Kbyte offset from the initial System Address segment where the Maps are loaded initially (Map 0 is loaded into A0000–A1FFF, Map 1 into A2000–A3FFF, etc.). Note the functional change of the Character Map Select register bits 2:0 when this mode is selected; the remaining bits (5:3) are not used.

In the 132-column alphanumeric mode, the CL-GD6245 uses both Plane 2 and Plane 3 physical DRAM pages for Character Map storage. However, the Character Maps appear to be loaded into Plane 2 only. The character-generator dot patterns of all lower 128 character codes are re-mapped into Plane 2, and all upper 128 character codes are re-mapped into Plane 3. Only half of each 64-Kbyte physical plane is used, providing a total of eight 8-Kbyte Character Maps.

While using the 132-column alphanumeric mode, the following CRT controller register settings are recommended:

Register	Register Name	Value
CR00	Horizontal Total	9Fh
CR01	Horizontal Display Enable End	83h
CR02	Start Horizontal Blanking	84h
CR03	End Horizontal Blanking	82h
CR04	Start Horizontal Retrace	8Ah
CR05	End Horizontal Retrace	9Eh
CR13	Offset	42h

6.6 Graphics Hardware Cursor

The CL-GD6245 supports a programmable 32 x 32 hardware cursor that replaces the software mouse pointer when using graphical user interfaces. The application software must initialize the hardware cursor and then needs only to update the cursor's position (x and y coordinates) as it moves.

When the hardware cursor is used in a 16-color planar mode or in a 256-color packed pixel mode, it improves the application's performance because it eliminates the software overhead needed to save and restore screen data as the cursor's position changes. As a result, the screen's appearance improves because the cursor moves more quickly and smoothly.

Table 6-6 provides information for programming the CL-GD6245 Extension registers for the graphics hardware cursor. For more information on the hardware cursor and its programming, refer to the application note "Microsoft® Windows™ Performance Enhancement Features" in the *CL-GD6245 Application Book*.

Table 6-6. Programming the Graphics Hardware Cursor

To:	Program:			
	Index or Extension Register	I/O Port Address	Register Bits	Bit Value
Disable graphics hardware cursor (the default)	SR12	3C5h	[0]	'0'
Enable the graphics hardware cursor	SR12	3C5h	[0]	'1'
Allow access to a graphics palette video DAC color lookup table that is VGA-compatible	SR12	3C5h	[1]	'0'
Allow for a cursor that is completely independent of the display data colors[a]	SR12	3C5h	[1]	'1'
Position the graphics hardware cursor[b] on the screen's horizontal X axis[c]	Indexes: 10, 30, 50, 70, 90, B0, D0, F0	3C4h/3C5h	[7:5]	2047...0
	Corresponding Extension registers: SR10, 30, 50, 70, 90, B0, D0, F0	3C4h/3C5h	[7:0]	2047...0
Position the graphics hardware cursor[b] on the screen's vertical Y axis[c]	Indexes: 11, 31, 51, 71, 91, B1, D1, F1	3C4h/3C5h	[7:5]	2047...0
	Corresponding Extension registers: SR11, 31, 51, 71, 91, B1, D1, F1	3C4h/3C5h	[7:0]	2047...0
Select the graphics hardware cursor pattern offset. (Four patterns available.)	SR13	3C5h	[1:0]	'00', '01' '10', '11'

[a] DAC LUT entries 256, 257, and 258 will be accessible as locations X0h, XFh, and X2h respectively.
Entry 256 will be used as the cursor background.
Entry 257 will be used as the cursor foreground.
Entry 258 will be used to provide a selected overscan color.

[b] The cursor position is defined relative to the upper-left corner of the active display screen (border is not included), and sets the upper-left corner of the 32 x 32-bit cursor.

[c] The cursor location X is in pixels. The cursor location Y is in scanlines.

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Ambient temperature while operating (T_A) ..... 0°C to 70°C

Storage temperature ..... –65°C to 150°C

Voltage on any pin ..... V_{SS} – 0.5 volts to $V_{CC/DD}$ + 0.5 volts

Operating power dissipation ..... 1.5 watts

Power supply voltage ..... 7.0 volts

Injection current (for latch-up testing) ..... 100 milliamperes

NOTES:

1) System components should be operated within the limits shown in the absolute maximum ratings. If system components are operated at or outside of these limits, the system components might be permanently damaged.
2) Functional operation at or outside of any of the limits indicated in the absolute maximum ratings is not implied.
3) Exposure to absolute maximum rating conditions for extended periods might affect system reliability.

7.2 DC Specifications (Digital)

($V_{CC} = V_{DD}$, V_{CC} = 5.0 ± 0.25 volts or 3.3 ± 0.3 volts, T_A = 0°C to 70°C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions	Note
V_{DD} (5 V)	Power Supply Voltage	4.75	5.25	Volts	Normal operation	
V_{DD} (3.3 V)	Power Supply Voltage	3.00	3.60	Volts	Normal operation	
V_{IL}	Input Low Voltage (TTL)	0	0.8	Volts	3.0 V < V_{DD} < 5.25 V	
V_{IH}	Input High Voltage (TTL)	2.0	1.05(V_{DD})	Volts	3.0 V < V_{DD} < 5.25 V	
V_{IHC}	Input High Voltage (CMOS)	0.7(V_{DD})	1.05(V_{DD})	Volts	3.0 V < V_{DD} < 5.25 V	
V_{ILC}	Input Low Voltage (CMOS)	–0.5	0.3(V_{DD})	Volts	3.0 V < V_{DD} < 5.25 V	
V_{OHC}	Output High Voltage (CMOS)	0.9(V_{DD})		Volts	I_{OHC} = –200 µA	
V_{OLC}	Output Low Voltage (CMOS)		0.1(V_{DD})	Volts	I_{OLC} = 3.2 mA	
V_{OL}	Output Low Voltage (TTL)		0.4	Volts	I_{OL} = (See Section 7.3)	1
V_{OH}	Output High Voltage (TTL)	2.4		Volts	I_{OH} = (See Section 7.3)	2
I_{CC1}	Power Supply Current		140	mA	CRT-only operation	3
I_{CC2}	Power Supply Current		50	mA	LCD-only operation	3
I_{CC3}	Power Supply Current		1.0	mA	Hardware-Controlled Suspend mode	3
I_{IL}	Input Low Current		–10	µA	V_{IN} = 0.0 V	
I_{IH}	Input High Current		10	µA	V_{IN} = V_{DD}	
I_{OZ}	Output Leakage Current	–10	10	µA	0 < V_{OUT} < V_{DD}	4
C_{IN}	Input Capacitance		10	pF		5
C_{OUT}	Output Capacitance		10	pF		5

NOTES:

1) Data outputs (DAT[15:0]), rated at I_{OL} = 12 mA at V_{OL} = 0.4 V, will sink I_{OL} = 24 mA at V_{OL} = 0.5 V.
2) Data outputs (DAT[15:0]), rated at I_{OH} = –3.0 mA at V_{OH} = 2.4 V, will source I_{OH} = –15 mA at V_{OH} = 2.0 V.
3) These current values are for V_{CC} = 3.3 V, FPVDCLK = 28 MHz, and MCLK = 33 MHz.
4) This current is the tristate output leakage current when in high-impedance (High-Z) mode.
5) This capacitance is periodically sampled and tested.

7.3 Output Loading Values

Output Pins	I_{OH} (mA)	I_{OL} (mA)	Load (pF)
DAT[31:0]	–3.0	8.0	100
RDY#	–3.0	8.0	100
LDEV#	–	8.0	100
LBS16#	–	8.0	100
IRQ	–3.0	8.0	100
HSYNC	–12	12	50
VSYNC	–12	12	50
SUD[7:0]	–12	12	50
R5, R4	–12	12	50
LD[3:0]	–12	12	50
UD[3:0]	–12	12	50
FPDE	–12	12	50
FPVDCLK	–12	12	250
LLCLK	–12	12	50
LFS	–12	12	50
MOD	–3.0	3.0	20
MA[9:0]	–6.0	6.0	35
MD[15:0]	–6.0	6.0	35
CAS*/WE*	–6.0	6.0	35
RAS*	–6.0	6.0	35
OE*	–6.0	6.0	35
WE1*/CAS1*	–6.0	6.0	35
WE0*/CAS0*	–6.0	6.0	35
FPVCC	–12	12	35
FPVEE	–12	12	35
FPBACK	–12	12	35
STANDBY	–6.0	6.0	35
BEO# (as output)	–6.0	6.0	35

7.4 DC Specifications (Palette DAC)

(V_{CC} = 3.3 ± 0.3 volts, T_A = 0°C to 70°C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions
DACVDD1, DACVDD2	DAC Supply Voltage	3.00	3.60	Volts	Normal operation
I_{DD}	Analog Supply Current		90	mA	DACVDD1, DACVDD2 = 3.6 V
I_{REF}	DAC Reference Current	–3	–10	mA	Note 1

NOTE:

1) See the detailed pin description in Section 2.2 for information on nominal I_{REF} .

7.5 DC Specifications (Clock Frequency Synthesizer)

(V_{CC} = 3.3 ± 0.3 volts, T_A = 0°C to 70°C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions
MAVDD, VAVDD	Synthesizer Supply Voltage	3.00	3.60	Volts	
I_{DD}	Analog Supply Current		to be determined	mA	MAVDD, VAVDD = 3.6 V

7.6 DAC Characteristics

(V_{CC} = 3.3 ± 0.3 volts, T_A = 0°C to 70°C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions	Note
R	Resolution		6	Bits		
I_O	Output Current		30	mA	V_O < 1 V	
t_D	Analog Output Delay		tbd	ns		1, 2, 3, 8
t_r, t_f	Analog Output Rise/Fall Time		8	ns		2, 3, 4
t_s	Analog Output Settling Time		15	ns		2, 3, 5
t_{SK}	Analog Output Skew		tbd	ns		2, 3, 6, 8
FT	Clock and Data Feed-through		tbd	dB		2, 3, 6, 8
DT	DAC-to-DAC Correlation		tbd	%		6, 7, 8
GI	Glitch Impulse		tbd	pV/sec.		2, 3, 6, 8
CT	DAC-to-DAC Crosstalk		tbd	dB		2, 3, 4, 8

NOTES:

1) t_D is measured from the 50% point of VCLK to 50% point of full-scale transition.
2) Load is 50 Ω and 30 pF per analog output.
3) The I_{REF} current value is calculated as discussed in the application note "IREF Current Source for the CL-GD6245" in the *CL-GD6245 Application Book.*
4) t_r and t_f are measured from 10% to 90% of full-scale value.
5) t_s is measured from 50% of full-scale transition to output remaining within 2% of final value.
6) Outputs are loaded identically.
7) This parameter is measured at the mid-point of the distribution of the three DACs when they are at full-scale output.
8) *tbd* = to be determined.

7.7 AC Specifications

7.7.1 List of Timing Diagrams

Table 7-1. Bus Signal Timing (ISA Bus)

Symbol	Parameter	MIN[a]	MAX[a]	Units
t_{1a} t_{1b}	MEMCS16* low delay from LA[23:17] valid MEMCS16* low delay from SA[16:15] valid	– –	20 14	ns ns
t_2	IOCS16* low delay from address	–	25	ns
t_3[b, c]	Address, SBHE* setup time to any command active	5.0	–	ns
t_4	Any command active to IOCHRDY low delay	–	28	ns
t_5	MEMCS16* high delay from address invalid	–	25	ns
t_6	IOW* pulse width IOR* pulse width SMEMW* pulse width SMEMR* pulse width	40 60 3 3	– – – [d]	ns ns MCLK[e] MCLK[e]
t_7	IOW* high setup time to any command active SMEMW* high setup time to next SMEMW* low	80 3	– –	ns MCLK[e]
t_8	Address, SBHE* hold time from any command inactive	0	–	ns
t_9	Data valid delay from SMEMW* low Data valid delay from IOW* low	– –	3 130	MCLK[e] ns
t_{10}	Data hold time from SMEMW* high Data hold time from IOW* high	10 0	– –	ns ns
t_{11}	Data setup time to IOW* high	5.0	–	ns
t_{12}	Data delay from IOR*,SMEMR* low	0	60	ns
t_{13}	Data delay from IOCHRDY high	–	15	ns
t_{14}	Data hold time from IOR*, SMEMR* high Data to high-impedance delay from IOR*, SMEMR* high	0 –	– 20	ns ns
t_{15}	AEN high (hold time) from IOR* or IOW* high	5.0	–	ns
t_{16}	REFRESH* setup time to SMEMR* low	20	–	ns
t_{17}	REFRESH* high (hold time) from SMEMR* low	0	–	ns
t_{18}	IOCHRDY low pulse width	10	–	ns

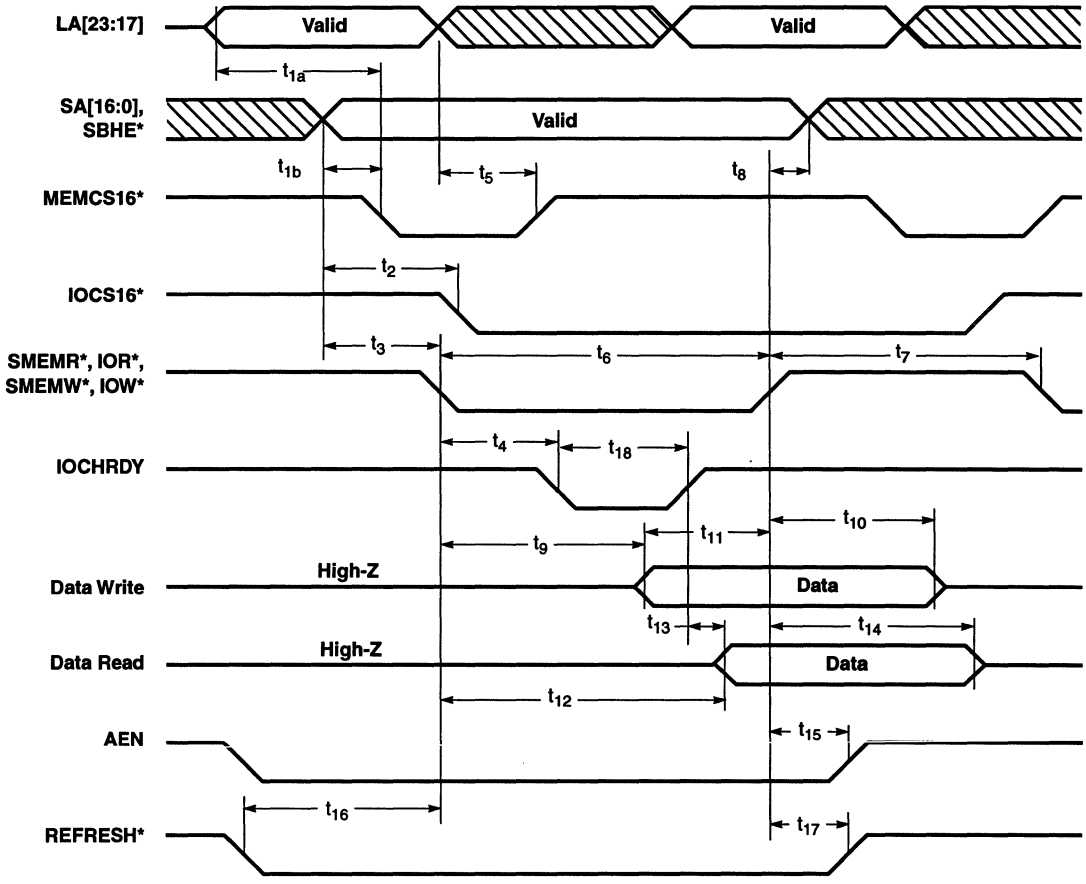
[a] The ISA-bus interface specifications are valid from 0°C to 70°C at operating voltages of 3.3 ± 0.3 V and 5.0 ± 0.25 V.

[b] AEN must be low for t_2, t_3, and t_6.

[c] Command is defined as IOR*, IOW*, SMEMR*, or SMEMW*.

[d] SMEMR* active-pulse width is determined by IOCHRDY.

[e] *MCLK*, when used as a unit in this table, refers to an MCLK period.

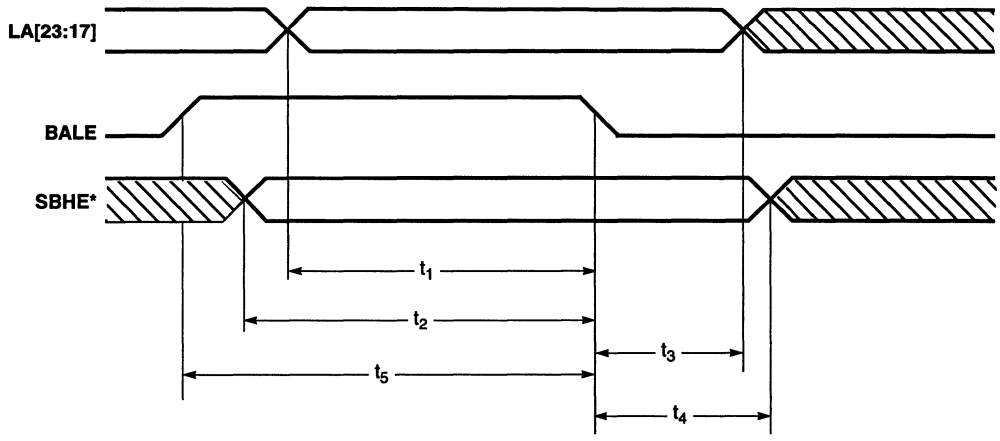


NOTE: All signals shown are from ISA bus.

Figure 7-1. Bus Signal Timing (ISA Bus)

Table 7-2. BALE Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	LA[23:17] setup time to BALE negative transition	20	–	ns
t_2	SBHE* setup time to BALE negative transition	20	–	ns
t_3	LA23:17 hold time from BALE negative transition	20	–	ns
t_4	SBHE* hold time from BALE negative transition	20	–	ns
t_5	BALE high pulse width	20		ns



NOTE: All signals shown are from ISA bus.

Figure 7-2. BALE Timing (ISA Bus)

Table 7-3. ROM Enable Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	BE0# (as EROM*) low delay from SMEMR* low	–	30	ns
t_2	BE0# (as EROM*) high delay from SMEMR* high	–	20	ns

NOTE: In ISA mode, BE0# is used as an optional BIOS EPROM enable.

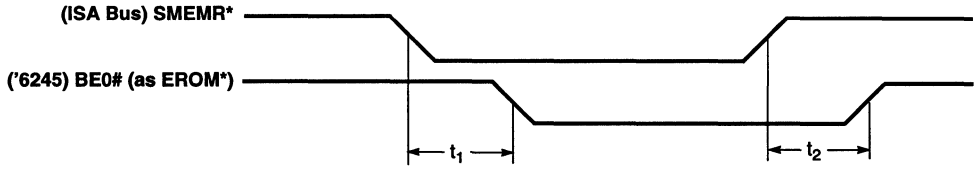
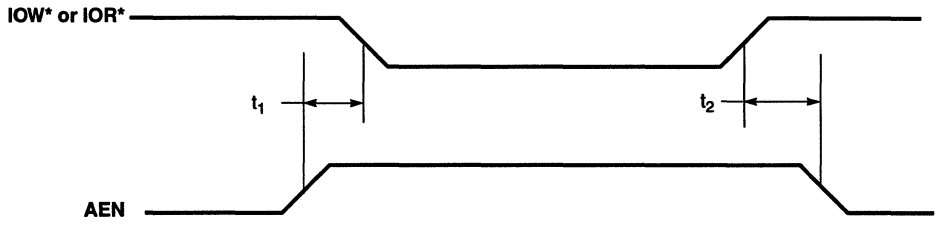


Figure 7-3. ROM Enable Timing (ISA Bus)

Table 7-4. AEN Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	AEN setup time to IOR* or IOW* low	5.0	–	ns
t_2	AEN hold time from IOR* or IOW* high	5.0	–	ns

NOTE: AEN high, as shown below, causes the CL-GD6245 to *disregard* the I/O cycle.

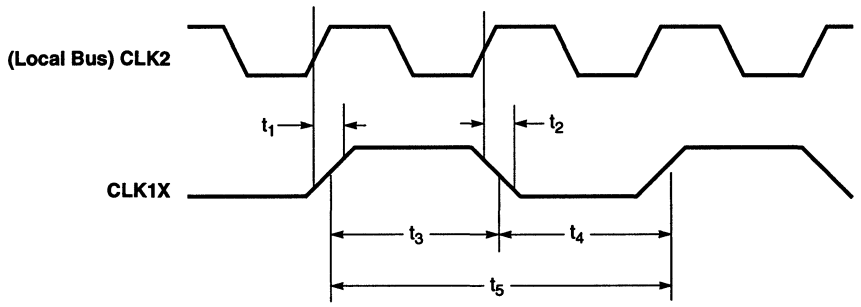


NOTE: All signals shown are from ISA bus.

Figure 7-4. AEN Timing (ISA Bus)

Table 7-5. CLK2 and CLK1X Timing (Local Bus)

Symbol	Parameter	CLK2		CLK1X		Units
		MIN	MAX	MIN	MAX	
t_1	Rise time	–	4.0	–	4.0	ns
t_2	Fall time	–	4.0	–	4.0	ns
t_3	Positive high pulse width	40	60	40	60	% t_5
t_4	Negative low pulse width	40	60	40	60	% t_5
t_5	Period	12.5	–	20	–	ns



NOTE: CLK1X is a divided-down signal from the system's central clock source.

Figure 7-5. CLK2 and CLK1X Timing (Local Bus)

Table 7-6. Reset Timing ('386 Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	CPU-RESET hold time from CLK2	4.0	–	ns
t_2	CPU-RESET setup time to CLK2	2.0	–	ns

NOTE: Applies to '386 only. For '486, CPU-RESET can be tied to RESET.

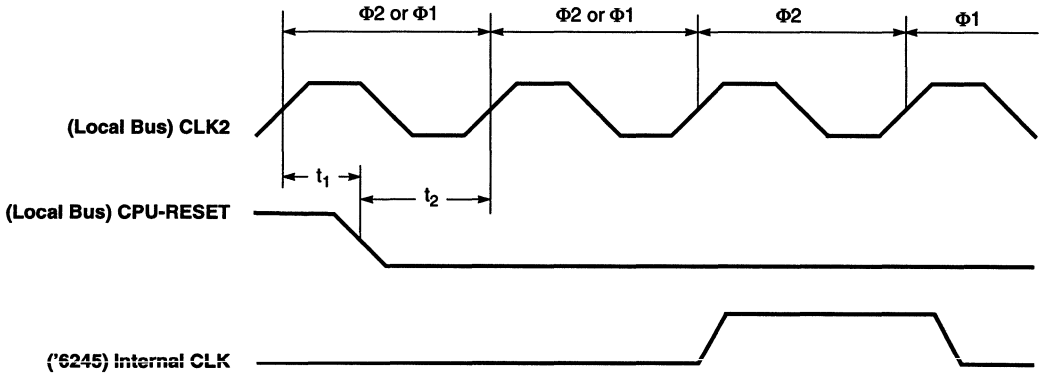
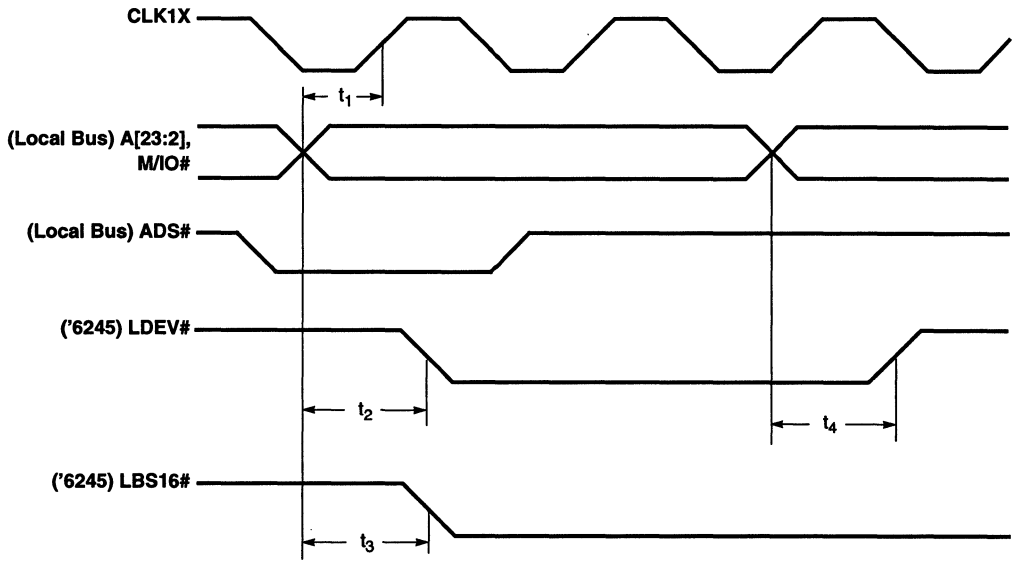


Figure 7-6. Reset Timing (Local Bus)

Table 7-7. ADS#, LDEV#, and LBS# Timing ('386DX and '486 Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, status, ADS# setup time to CLK1X	5.0	–	ns
t_2	LDEV# low delay from address, status (20-pF loading)	–	15	ns
t_3	LBS16# low delay from address, status	–	15	ns
t_4	LDEV# high delay from address, status	–	18	ns



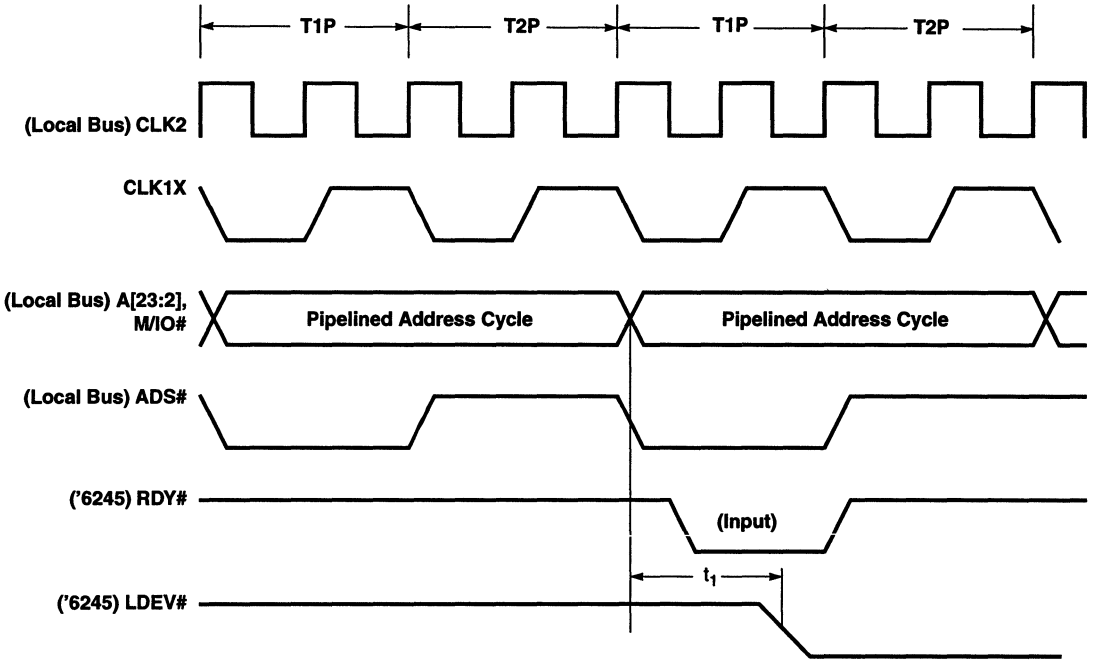
NOTE: CLK1X is a divided-down signal from the system's central clock source.

Figure 7-7. ADS#, LDEV#, and LBS# Timing ('386DX and '486 Local Bus)

Table 7-8. LDEV# Timing ('386SX Local Bus, Pipelining Shown)

Symbol	Parameter	MIN	MAX	Units
t_1	LDEV# delay from address	–	25	ns

NOTE: The *P* in *T1P* designates the pipeline mode.



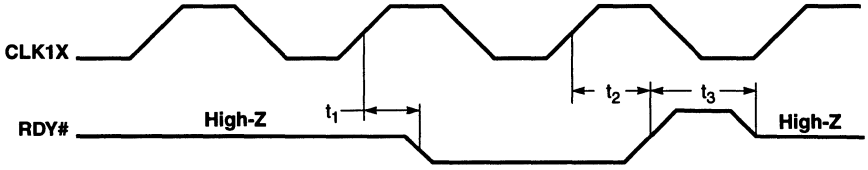
NOTE: CLK1X is a divided-down signal from the system's central clock source.

Figure 7-8. LDEV# Timing ('386SX Local Bus, Pipelining Shown)

Table 7-9. RDY# Delay (Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	RDY# active delay from CLK1X	–	12	ns
t_2	RDY# 'high' delay from CLK1X	–	12	ns
t_3	RDY# high before high-impedance	–	0.5	CLK1X[a]

[a] *CLK1X*, when used as a unit in this table, refers to a CLK1X period.

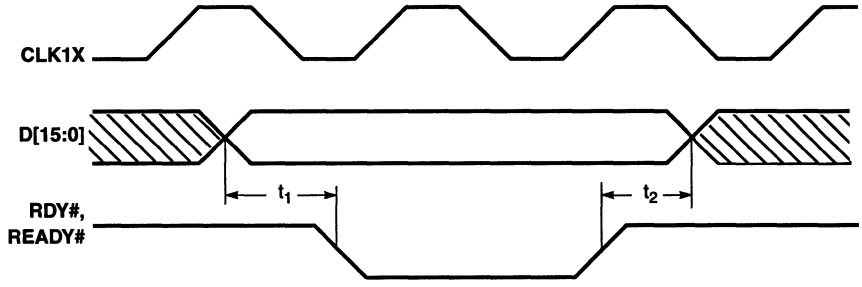


NOTE: CLK1X is a divided-down signal from the system's central clock source.

Figure 7-9. RDY# Delay (Local Bus)

Table 7-10. Read Data Timing (Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Read data setup time to RDY#, READY# low	15	–	ns
t_2	Read data hold time from RDY#, READY# high	12	–	ns



NOTE: CLK1X is a divided-down signal from the system's central clock source.

Figure 7-10. Read Data Timing (Local Bus)

Table 7-11. Self-Refresh DRAM Timing (Display Memory Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	CAS* low setup time to RAS* low setup time	100	300	ns

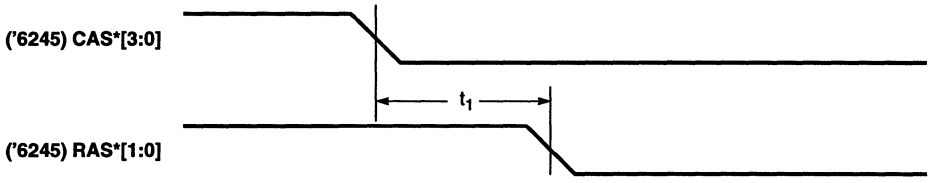


Figure 7-11. Self-Refresh DRAM Timing (Display Memory Bus)

Table 7-12. Read Timing (Display Memory Bus)

Symbol	Parameter	MIN[a]	MAX[a]	Units[b]
t_1	Row address setup time to RAS* low	5.0	–	ns
t_2	Column address setup time to CAS* low	5.0	–	ns
t_3	RAS* low to CAS* low delay	2.5	–	MCLK
t_4	Row address hold time from RAS* low	1.0	–	MCLK
t_5	Column address hold time from CAS* low	1.0	–	MCLK
t_6	Data valid delay from RAS* low	–	4.0	MCLK
t_7	Data valid delay from CAS* low	–	1.5	MCLK
t_8	Data valid delay from column address valid	–	2.0	MCLK
t_9	RAS* precharge (RAS* pulse width high)	3.0	–	MCLK
t_{10}	Read cycle time	7.0	–	MCLK
t_{11}	Read command hold time from CAS* high	0.5	–	MCLK
t_{12}	CAS* precharge (CAS* pulse width high)	0.5	–	MCLK
t_{13}	RAS* pulse width low RAS* pulse width low (Page mode)	4.0 –	– 32	MCLK µs
t_{14}	CAS* pulse width low	1.5	–	MCLK
t_{15}	Read data hold time from CAS* high	10	–	ns
t_{16}	Read command setup time	5.0	–	ns
t_{17}	Data valid delay from OE* low	–	1.5	MCLK
t_{18}	Read command hold time from RAS* high	1.0	–	MCLK
t_{19}	RAS* hold time from OE* low	1.5	–	MCLK
t_{20}	CAS* 'high' setup time to RAS* low (precharge time)	0.5	–	MCLK
t_{21}	RAS* low to CAS* high	4.0	–	MCLK
t_{22}	CAS* cycle time	2.0	–	MCLK
t_{23}	Read data hold time from OE* high	10	–	ns

[a] The memory interface specifications are valid from 0°C to 70°C at operating voltages of 3.3 ± 0.3 V and 5.0 ± 0.25 V.

[b] *MCLK*, when used as a unit in this table, refers to an MCLK period.

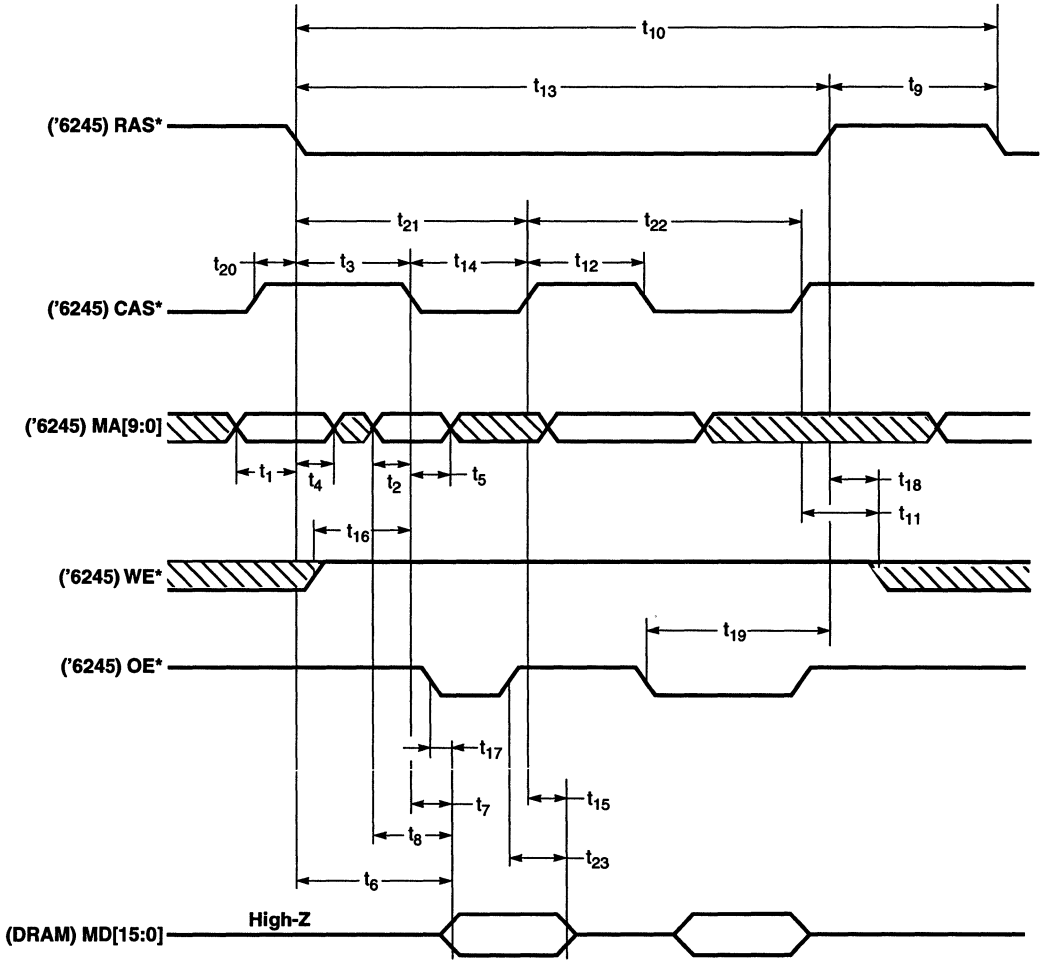


Figure 7-12. Read Timing (Display Memory Bus)

Table 7-13. Write Timing (Display Memory Bus)

Symbol	Parameter	MIN[a]	MAX[a]	Units[b]
t_1	Address setup time to RAS* low	5.0	–	ns
t_2	Address setup time to CAS* low	5.0	–	ns
t_3	RAS* low to CAS* low delay	2.5	–	MCLK
t_4	Row address hold time from RAS* low	1.0	–	MCLK
t_5	Column address hold time from CAS* low	1.0	–	MCLK
t_6	RAS* precharge (RAS* pulse width high)	3.0	–	MCLK
t_7	Write cycle time	7.0	–	MCLK
t_8	CAS* precharge (CAS* pulse width high)	0.5	–	MCLK
t_9	CAS* 'high' setup time to RAS* low (precharge time)	0.5	–	MCLK
t_{10}	RAS* low to CAS* high	4.0	–	MCLK
t_{11}	CAS* cycle time	2.0	–	MCLK
t_{12}	CAS* pulse width low	1.5	–	MCLK
t_{13}	RAS* pulse width low RAS* pulse width low (Page mode)	4.0 –	– 32	MCLK µs
t_{14}	WE* low setup time to CAS* low	0.5	–	MCLK
t_{15}	WE* low hold time to CAS* low	0.5	–	MCLK
t_{16}	WE* low pulse width	1.0	–	MCLK
t_{17}	Write data setup time to CAS* low	5.0	–	ns
t_{18}	Write data hold time from CAS* low	1.0	–	MCLK
t_{19}	WE* low to CAS* high delay time	1.0	–	MCLK

[a] The memory interface specifications are valid from 0°C to 70°C at operating voltages of 3.3 ± 0.3 V and 5 ± 0.25 V.

[b] *MCLK*, when used as a unit in this table, refers to an MCLK period.

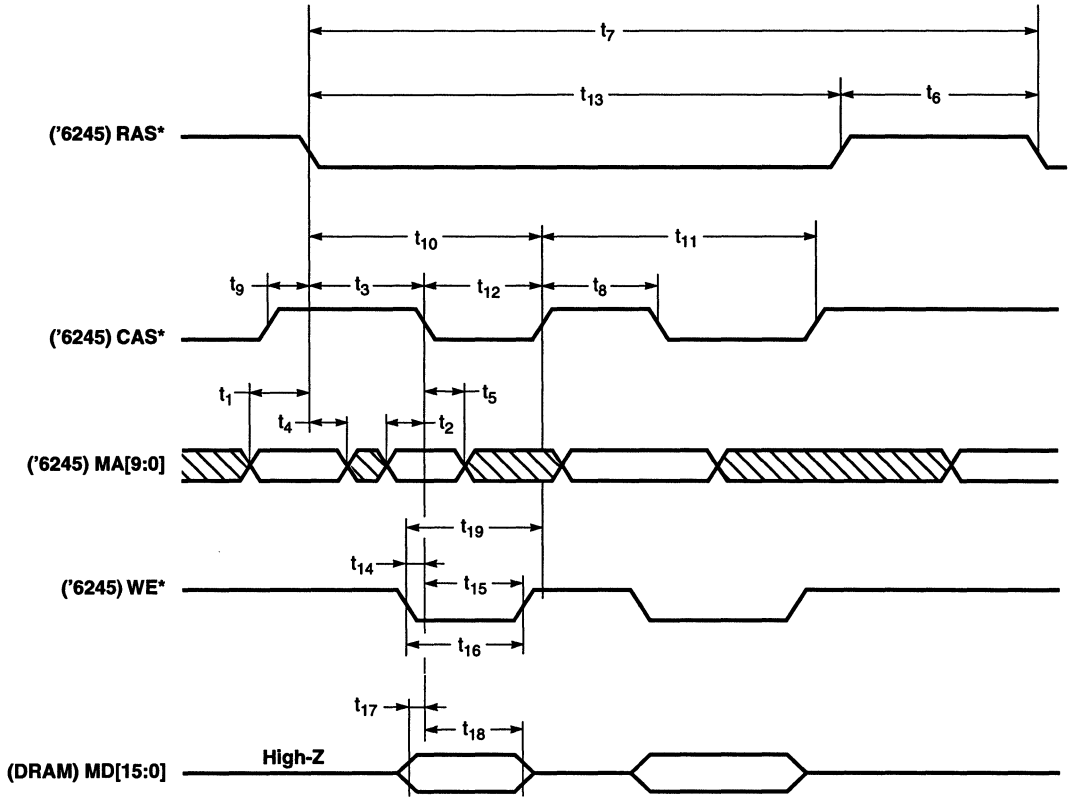


Figure 7-13. Write Timing (Display Memory Bus)

Table 7-14. CAS*-before-RAS* Refresh Timing (Display Memory Bus)

Symbol	Parameter	MIN	MAX	Units[a]
t_1	CAS* low setup time to RAS* low	1.0	–	MCLK
t_2	RAS* low pulse width	4.0	–	MCLK
t_3	RAS* high pulse width	3.0	–	MCLK
t_4	CAS* hold time for refresh	1.5	–	MCLK
t_5	Refresh cycle period	7.0	–	MCLK
t_6	CAS* pulse width high (pre-charge time)	2.0	–	MCLK
t_7	RAS* high to CAS* low (pre-charge time)	1.0	–	MCLK

[a] *MCLK*, when used as a unit in this table, refers to an MCLK period.

NOTE: There are either three or four RAS* pulses while CAS* remains low.

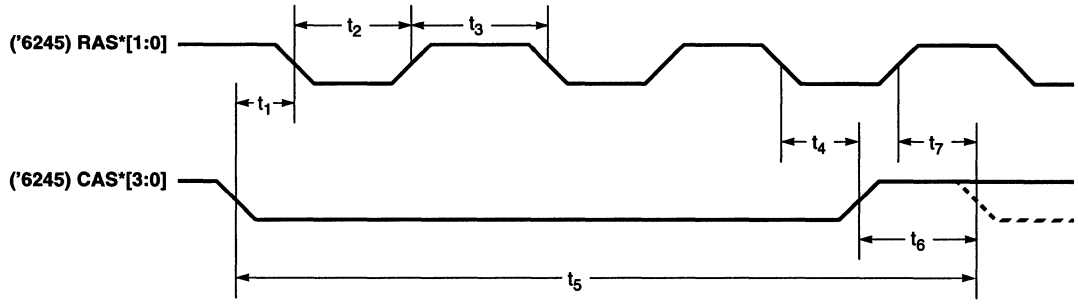


Figure 7-14. CAS*-before-RAS* Refresh Timing (Display Memory Bus)

Table 7-15. Reset Timing

Symbol	Parameter	MIN	MAX	Units
t_1	RESET pulse width high	12	–	MCLK[a]
t_2	MD[15:0] setup to RESET negative edge	2.0	–	ns
t_3	MD[15:0] hold from RESET negative edge	5.0	–	ns
t_4	RESET low to first IOW*	12	–	MCLK[a]

[a] *MCLK*, when used as a unit in this table, refers to an MCLK period.

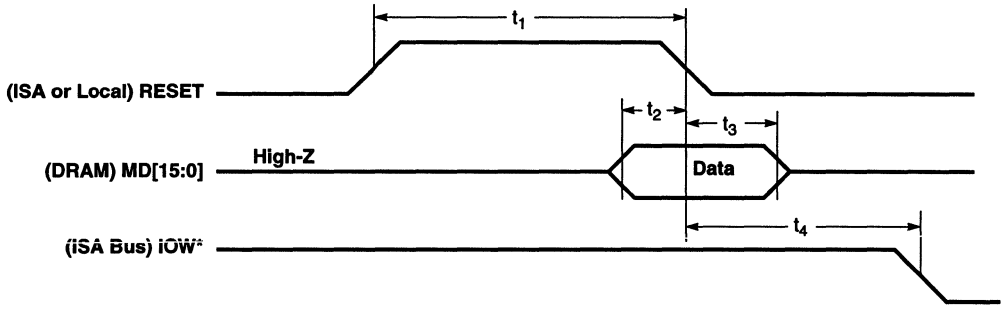


Figure 7-15. Reset Timing

Table 7-16. STN Monochrome and Color Passive LCD Interface Timing

Symbol	Parameter	M2DD-8 (Mono.)	M2SS-4 (Mono.)	C8DD-16 (Color)	C8DD-8 (Color)	C8SS-16 (Color)	C8SSI-d-8 (Color)	Units
t_1	FPVDCLK period	4T – 5	4T – 5	2.5T – 5	T – 5	5T – 5	5T – 5	ns
t_2	FPVDCLK high time	2T – 5	2T – 5	T – 5	0.5T – 5	2T – 5	T – 5	ns
t_3	FPVDCLK low time	2T – 5	2T – 5	T – 5	0.5T – 5	2T – 5	4T – 5	ns
t_4	FPVDCLK rise and fall time	5 MAX	5 MAX	5 MAX	5 MAX	5 MAX	5 MAX	ns
t_5	Data setup time	2T – 10	2T – 10	T – 5	0.5T – 5	2T – 10	T – 10	ns
t_6	Data hold time	2T – 10	2T – 10	T – 5	0.5T – 5	2T – 10	T – 10	ns
t_7	FPVDCLK low to LLCLK low	4T – 10	4T – 10	T – 5	2T – 10	4T – 10	2T – 10	ns
t_8	FPVDCLK low from LLCLK low	4T – 10	4T – 10	T – 5	2T – 10	4T – 10	2T – 10	ns
t_9	LLCLK high time	3T – 5	3T – 5	3T – 5	3T – 5	3T – 5	3T – 5	ns
t_{10}	LFS high setup to LLCLK low	2T typical	2T typical	2T typical	2T typical	2T typical	2T typical	ns
t_{11}	LFS high hold time to LLCLK low	2T typical	2T typical	2T typical	2T typical	2T typical	2T typical	ns
t_{12}	MOD delay from FPVDCLK high	300 MAX	300 MAX	300 MAX	300 MAX	300 MAX	300 MAX	ns

NOTES:

1) *T*, when used in this table, is the VCLK period (in units of ns).
2) Values are MIN unless specified otherwise.

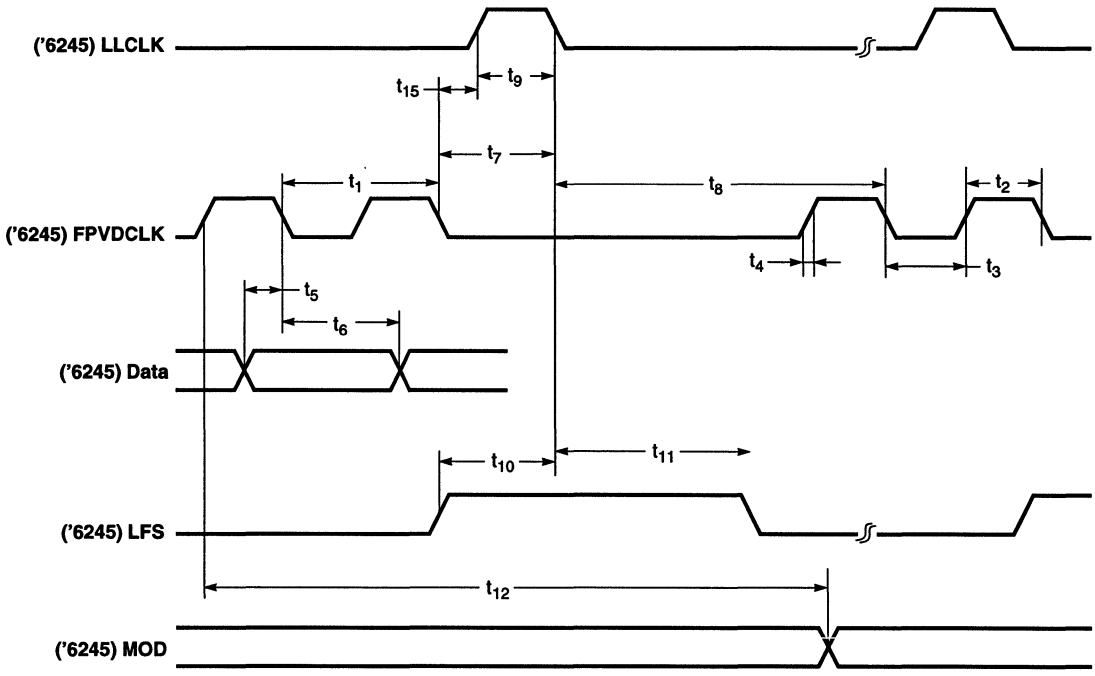


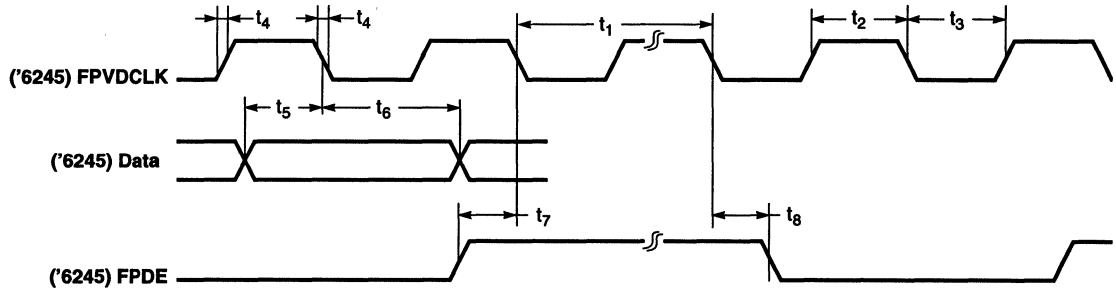
Figure 7-16. STN Monochrome and Color Passive LCD Interface Timing

Table 7-17. LCD Interface Timing

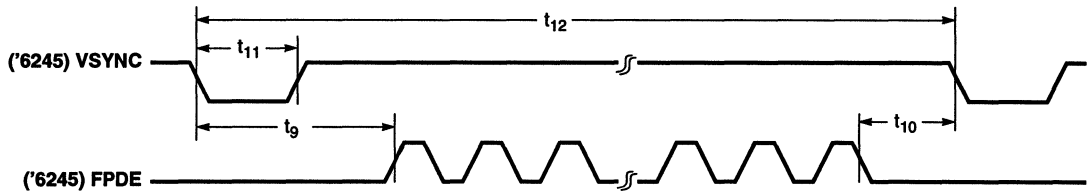
Symbol	Parameter	MIN[a]	MAX[a]	Units
t_1	FPVDCLK period	T – 5	–	ns
t_2	FPVDCLK high time	0.25T – 5	–	ns
t_3	FPVDCLK low time	0.25T – 5	–	ns
t_4	FPVDCLK rise and fall time	–	10	ns
t_5	Data setup time	0.25T – 5	–	ns
t_6	Data hold time	0.25T – 5	–	ns
t_7	FPDE setup to FPVDCLK	0.25T – 5	–	ns
t_8	FPDE hold to FPVDCLK	0.25T – 5	–	ns
t_9	Vertical front porch	0	30	lines
t_{10}	Vertical back porch	1	31	lines
t_{11}	VSYNC width [b]	1	2	lines
t_{12}	Vertical cycle time	–	60 Hz typical	

[a] *T*, when used in this table, is the VCLK period (in units of ns).

[b] VSYNC pulse width is programmable with a choice of one line period or two line periods. Refer to the explanation of ERF4.



Color TFT



Monochrome TFT

Figure 7-17. LCD Interface Timing

Table 7-18. Clock Frequency Synthesizer Input

Symbol	Parameter	V_{DD} = 3.3 ± 0.3 V		V_{DD} = 5.0 ± 0.25 V	
		MIN	MAX	MIN	MAX
t_1	Input clock rise time	1.0 ns	7.0 ns	1.0 ns	7.0 ns
t_2	Input clock fall time	1.0 ns	7.0 ns	1.0 ns	7.0 ns
t_3	Input clock low period of duty cycle	40% of t_{CLKP}	60% of t_{CLKP}	40% of t_{CLKP}	60% of t_{CLKP}
t_4	Input clock high period of duty cycle	40% of t_{CLKP}	60% of t_{CLKP}	40% of t_{CLKP}	60% of t_{CLKP}
t_5	Input clock OSC period (frequency)	69.84 ns – 0.1% (14.318 MHz)	69.84 ns + 0.1% (14.318 MHz)	69.84 ns – 0.1% (14.318 MHz)	69.84 ns + 0.1% (14.318 MHz)
V_{IH}	Input high voltage	2.0 V	V_{DD} voltage	2.0 V	V_{DD} voltage
V_{IL}	Input low voltage	Ground	0.5 V	Ground	0.8 V

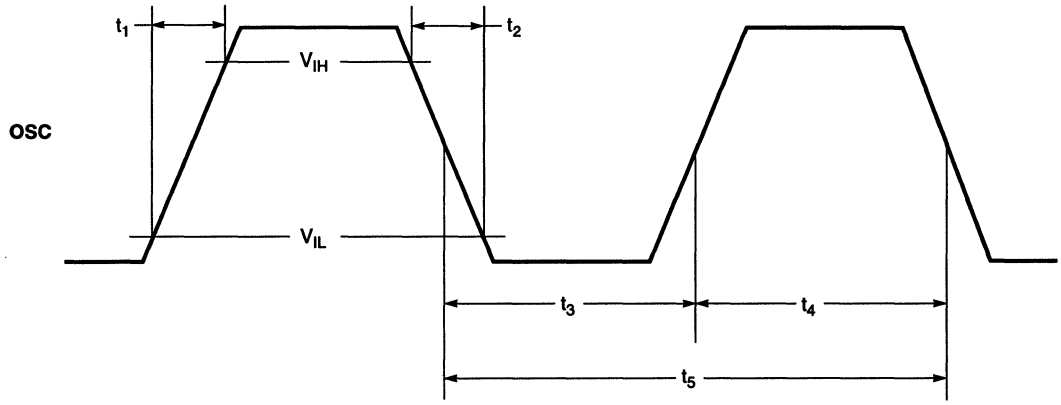


Figure 7-18. Clock Frequency Synthesizer Input

7.8 VCO, MCLK, and VCLK Values

Two programmable VCOs (voltage-controlled oscillators) determine the MCLK and VCLK frequencies. The MCLK frequency, which determines the memory timing and sequencing, is determined by VCO 1 and programmed by registers SRB, SRC, SRD, SRE, SR1B, SR1C, SR1D, and SR1E. The VCLK frequency, which determines the timing for driving the display, is determined by VCO 2 as shown in Figure 7-19 and programmed by registers SRF and SR1F. Table 7-19 lists the frequency ranges for the voltage values supplied to the VCO.

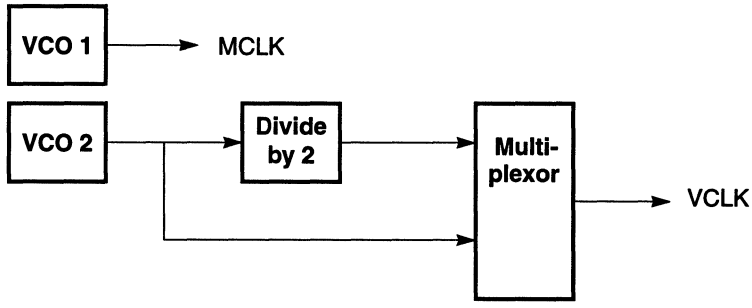
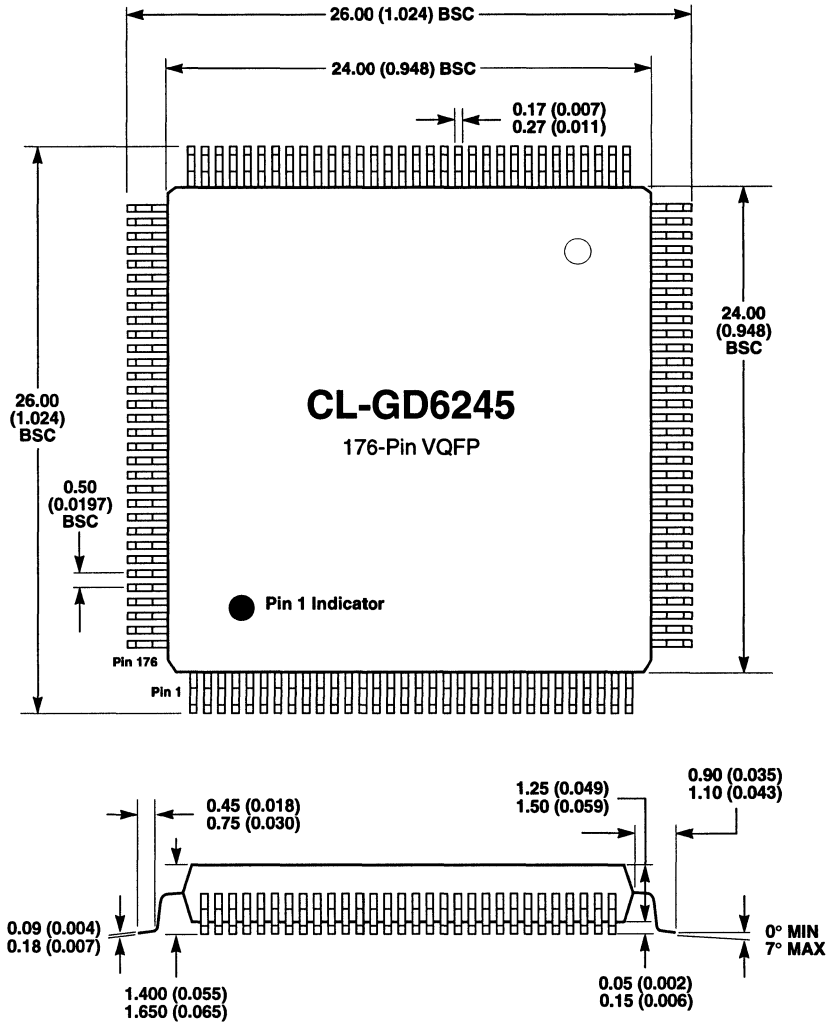


Figure 7-19. VCO, MCLK, and VCLK Design

Table 7-19. Minimum and Maximum Frequencies for VCO Circuits

Signal	Voltage Supply to VCO			
	3.3 V		5.0 V	
	MIN (MHz)	MAX (MHz)	MIN (MHz)	MAX (MHz)
Sequencer VCO	3	80	18	130
Video VCO	4	90	17	108
MCLK	25	50	25	50
VCLK	12	45	70	65

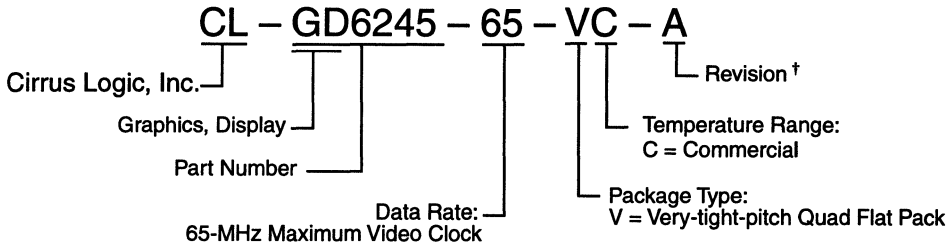
8. PACKAGE SPECIFICATIONS



NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

9. ORDERING INFORMATION EXAMPLE



† Contact Cirrus Logic for up-to-date information on revisions.

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