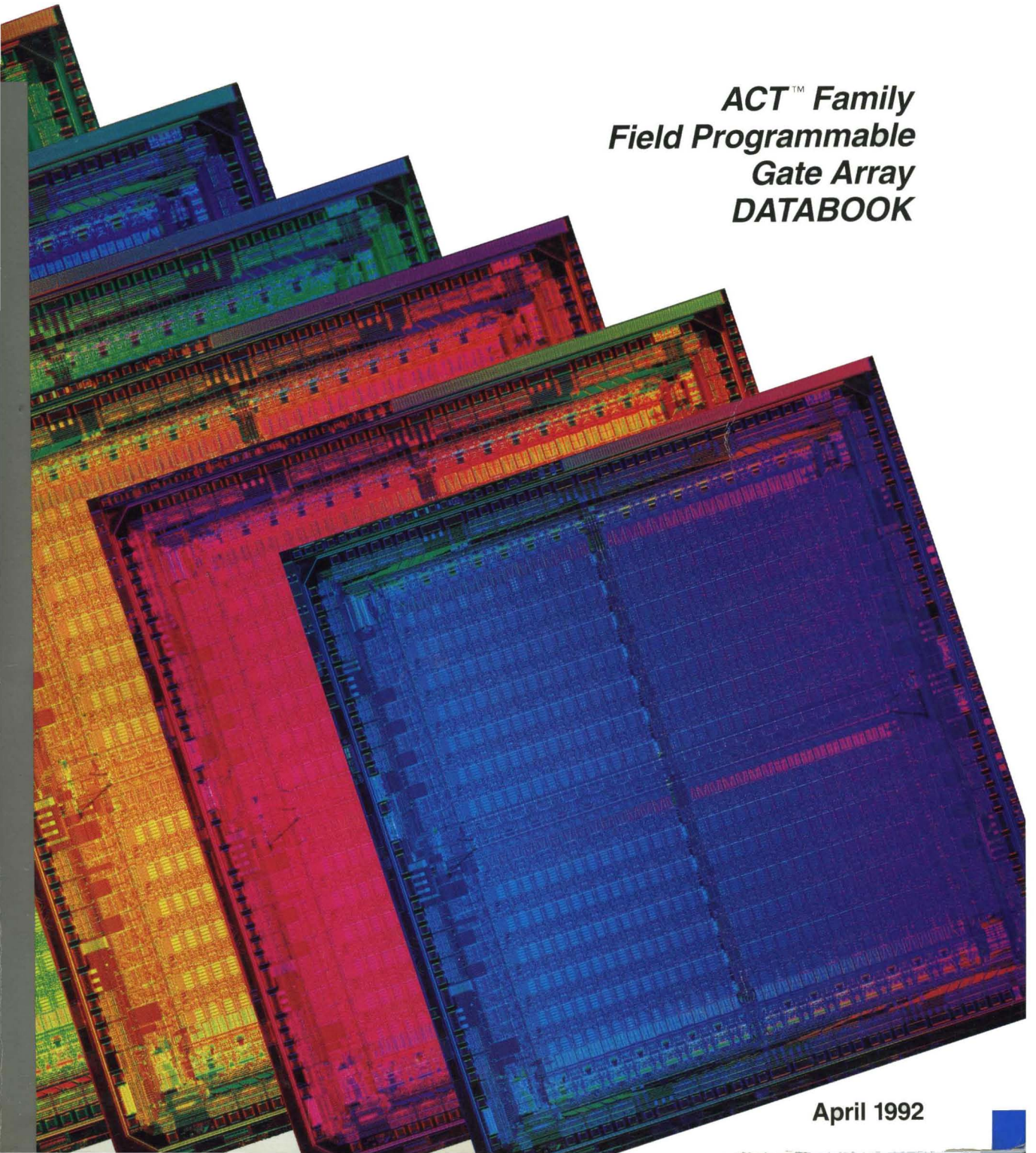
Actel



ACT™ Family Field Programmable Gate Array DATABOOK

April 1992

ACT™ Family
Field Programmable Gate Array
Databook

April 1992

ACT™ Family
Field Programmable Gate Arrays

This databook introduces you to Actel's Field Programmable Gate Arrays (FPGA) and the Action Logic System (ALS) design environment. In this book, you will find device specifications, reliability data, and ordering information for systems and devices.

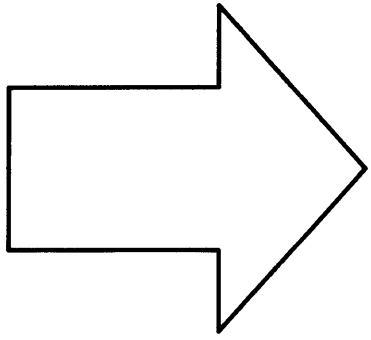
Refer to *The FPGA Design Guide* for practical design examples using Actel's FPGAs and for tools to help you estimate design requirements for your FPGA application.

For current availability and prices, contact your local Actel representative. A complete sales office listing is provided at the end of this book.

If you need to speak to a Technical Support engineer, call Actel's Technical Support Hotline: 800-262-1060.

ACT™ Family Field Programmable Gate Array Databook

Order of Contents



Product Selector Guide

Product Selector Table

Device	Pkg.[1]	# Pins	Speed Option[2]	Temp.[3]	User I/O	Gates		Flip-Flops (max)	Equiv. Pkgs.	
						Gate Array	PLD Equiv.		TTLs	20-Pin PALS
A1010A	PL	44	Std, -1, -2	C, I	34	1,200	3,000	147	34	12
	PL	68	Std, -1, -2	C, I	57	1,200	3,000	147	34	12
	PQ	100	Std, -1, -2	C, I	57	1,200	3,000	147	34	12
	PG	84	Std, -1	C, M, B	57	1,200	3,000	147	34	12
A1020A	PL	44	Std, -1, -2	C, I	34	2,000	6,000	273	53	17
	PL	68	Std, -1, -2	C, I	57	2,000	6,000	273	53	17
	PL	84	Std, -1, -2	C, I	69	2,000	6,000	273	53	17
	PQ	100	Std, -1, -2	C, I	69	2,000	6,000	273	53	17
	CQ	84	Std, -1	C, M, B	69	2,000	6,000	273	53	17
	JQ	44	Std, -1	C, M, B	34	2,000	6,000	273	53	17
	JQ	68	Std, -1	C, M, B	57	2,000	6,000	273	53	17
	JQ	84	Std, -1	C, M, B	69	2,000	6,000	273	53	17
	PG	84	Std, -1	C, M, B	69	2,000	6,000	273	53	17
A1225	PQ	100	Std, -1	C, I	83	2,500	6,250	382	70	23
	PG	100	Std, -1	C	83	2,500	6,250	382	70	23
A1240	PQ	144	Std, -1	C, I	104	4,000	10,000	514	105	34
	PG	132	Std, -1*	C, M, B	92	4,000	10,000	514	105	34
A1280	PQ	160	Std, -1	C, I	124	8,000	20,000	998	210	69
	CQ	172	Std	C, M, B	140	8,000	20,000	998	210	69
	PG	176	Std, -1*	C, M, B	140	8,000	20,000	998	210	69

* Only Commercial Temperature Devices offered in -1 Speed

Notes:

1. Package Types:
   - CQ – Ceramic Quad Flatpacks
   - JQ – J-Leaded Cerquad Chip Carriers
   - PG – Ceramic Pin Grid Arrays
   - PL – Plastic J-Leaded Chip Carriers
   - PQ – Plastic Quad Flat Packs
2. Speed Options:
   - Std – Standard Speed
   - -1 – Standard + 15% Speed
   - -2 – Standard + 25% Speed
3. Temperature Range:
   - C – Commercial Temperature (0 to +75°C)
   - I – Industrial (-40 to +85°C)
   - M – Military (-55 to +125°C)
   - B – MIL-STD-883C

ACT™ 1 Field Programmable Gate Arrays

Features

- Up to 2000 Gate Array Gates (6000 PLD/LCA™ equivalent gates)
- Replaces up to 53 TTL Packages
- Replaces up to 17 20-Pin PAL™ Packages
- Design Library with over 250 Functions
- Gate Array Architecture Allows Completely Automatic Place and Route
- Up to 547 Programmable Logic Modules
- Up to 273 Flip-Flops
- Flip-Flop Toggle Rates to 100 MHz
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Built-In High Speed Clock Distribution Network
- I/O Drive to 4 mA
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment

Product Family Profile

Device	A1010A	A1020A
Capacity		
Gate Array Equivalent Gates	1200	2000
PLD/LCA Equivalent Gates	3000	6000
TTL Equivalent Packages	34	53
20-Pin PAL Equivalent Packages	12	17
Logic Modules	295	547
Flip-Flops (maximum)	147	273
Routing Resources		
Horizontal Tracks/Channel	22	22
Vertical Tracks/Column	13	13
PLICE Antifuse Elements	112,000	186,000
User I/Os (maximum)	57	69
Packages	44 PLCC	44 PLCC
	68 PLCC	68 PLCC
		84 PLCC
	100 PQFP	100 PQFP
	44 JQCC	44 JQCC
	68 JQCC	68 JQCC
		84 JQCC
		84 CQFP
	84 CPGA	84 CPGA
Performance		
Flip-Flop Toggle Rate (maximum)	95 MHz	95 MHz
System Speed (maximum)	40 MHz	40 MHz
CMOS Process	1.2 µm	1.2 µm

Note:
1. See Product Plan on pages 1-6 for package availability.

Description

The ACT™ 1 family of field programmable gate arrays (FPGAs) offers a variety of package, speed, and application combinations. Devices are implemented in silicon gate, 1.2-micron or 2-micron two-level metal CMOS, and they employ Actel's PLICE™ antifuse technology. The unique architecture offers gate array flexibility, high performance, and instant turnaround through user programming. Device utilization is typically 95% of available logic modules.

ACT 1 devices also provide system designers with unique on-chip diagnostic probe capabilities, allowing convenient testing and debugging. Additional features include an on-chip clock driver with a hardwired distribution network. The network provides efficient clock distribution with minimum skew.

The user-definable I/Os are capable of driving at both TTL and CMOS drive levels. Available packages include plastic and ceramic J-leaded chip carriers, ceramic and plastic quad flatpacks, and ceramic pin grid array.

A security fuse may be programmed to disable all further programming and to protect the design from being copied or reverse engineered.

The Action Logic System

The ACT 1 device family is supported by Actel's Action Logic™ System (ALS), allowing logic design implementation with minimum effort. The ALS interfaces with the resident CAE system to provide a complete gate array design environment: schematic capture, simulation, fully automatic place and route, timing verification, and device programming. The Action Logic System is available for 386™ PC and for Apollo™ and Sun™ workstations and for running Viewlogic®, Mentor Graphics®, Valid™, and OrCAD™.

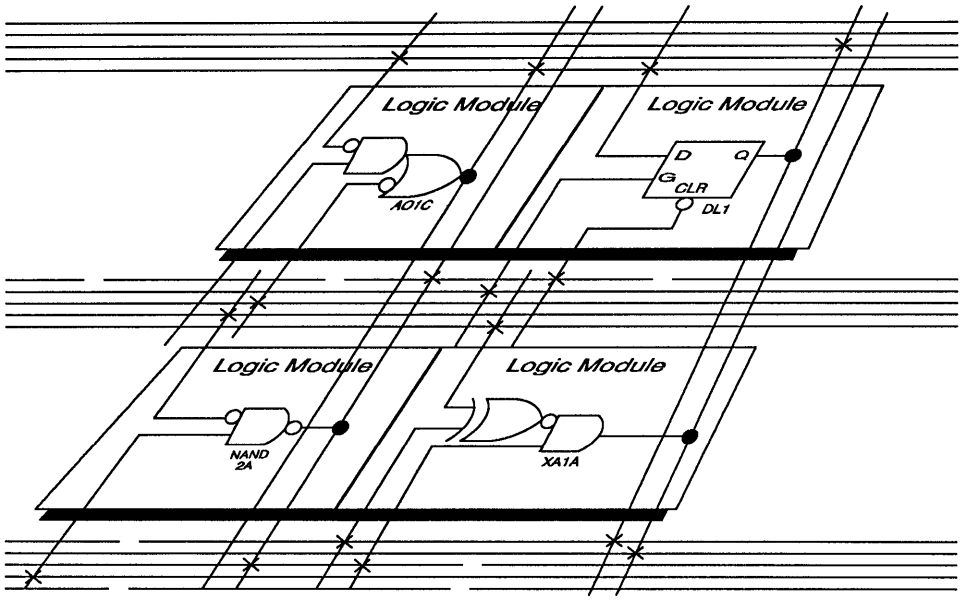


Figure 1. Partial View of an ACT 1 Device

ACT 1 Device Structure

A partial view of an ACT 1 device (Figure 1) depicts four logic modules and distributed horizontal and vertical interconnect tracks. PLICE antifuses, located at intersections of the horizontal and vertical tracks, connect logic module inputs and outputs. During programming, these antifuses are addressed and programmed to make the connections required by the circuit application.

The Actel Logic Module

The Actel logic module is an 8-input, one-output logic circuit chosen for the wide range of functions it implements and for its efficient use of interconnect routing resources (Figure 2).

The logic module can implement the four basic logic functions (NAND, AND, OR, and NOR) in gates of two, three, or four inputs. Each function may have many versions, with different combinations of active-low inputs. The logic module can also implement a variety of D-latches, exclusivity function, AND-ORs, and OR-ANDs. No dedicated hardwired latches or flip-flops are required in the array since latches and flip-flops may be constructed from logic modules wherever needed in the application.

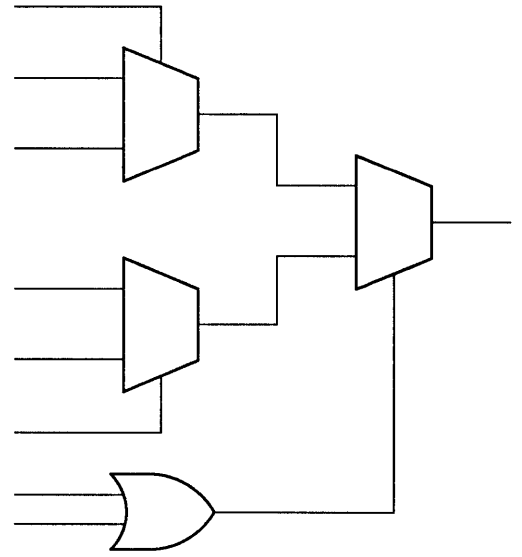


Figure 2. ACT 1 Logic Module

I/O Buffers

Each I/O pin is available as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Outputs sink or source 4 mA at TTL levels. See Electrical Specifications for additional I/O buffer specifications.

Device Organization

ACT 1 devices consist of a matrix of logic modules arranged in rows separated by wiring channels. This array is surrounded by a ring of peripheral circuits including I/O buffers, testability circuits, and diagnostic probe circuits providing real-time diagnostic capability. Between rows of logic modules are routing channels containing sets of segmented metal tracks with PLICE antifuses. Each channel has 22 signal tracks. Vertical routing is permitted via 13 vertical tracks per logic module column. The resulting network allows arbitrary and flexible interconnections between logic modules and I/O modules.

Probe Pin

ACT 1 devices have two independent diagnostic probe pins. These pins allow the user to observe any two internal signals by entering the appropriate net name in the diagnostic software. Signals may be viewed on a logic analyzer using Actel's Actionprobe™ diagnostic tools. The probe pins can also be used as user-defined I/Os when debugging is finished.

ACT 1 Array Performance

Temperature and Voltage Effects

Worst-case delays for ACT 1 arrays are calculated in the same manner as for masked array products. A typical delay parameter is multiplied by a derating factor to account for temperature, voltage, and processing effects. However, in an ACT 1 array, temperature and voltage effects are less dramatic than with masked devices. The electrical characteristics of module interconnections on ACT 1 devices remain constant over voltage and temperature fluctuations.

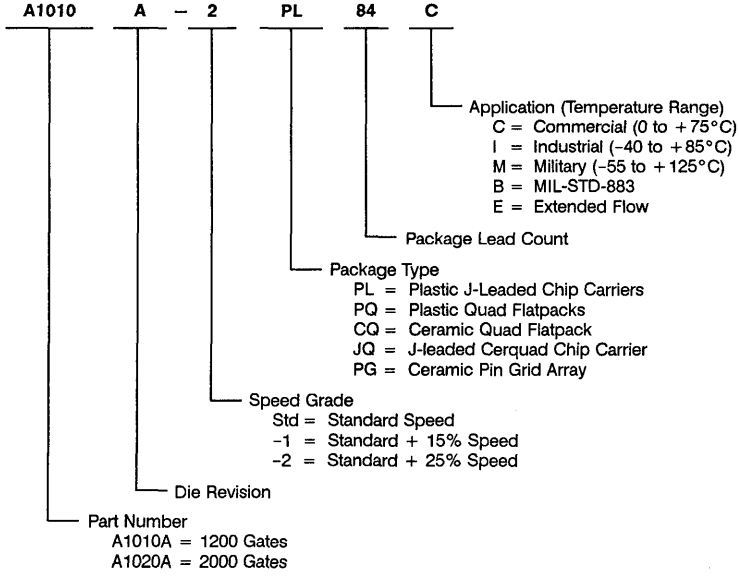
As a result, the total derating factor from typical to worst case for a standard speed ACT 1 array is only 1.19 to 1, compared to 2 to 1 for a masked gate array.

Logic Module Size

Logic module size also affects performance. A mask programmed gate array cell with four transistors usually implements only one logic level. In the more complex logic module (similar to the complexity of a gate array macro) of an ACT 1 array, implementation of multiple logic levels within a single module is possible. This eliminates interlevel wiring and associated RC delays. The effect is termed "net compression."

1

Ordering Information



Product Plan

	Speed Grade*			Application				
	Std	-1	-2	C	I	M	B	E
A1010A Device								
44-pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–	–
68-pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–	–
100-pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–	–
84-pin Ceramic Pin Grid Array (PG)	✓	✓	–	✓	–	✓	✓	–
A1020A Device								
44-pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–	–
68-pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–	–
84-pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–	–
100-pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–	–
84-pin Ceramic Pin Grid Array (PG)	✓	✓	–	✓	–	✓	✓	–
84-pin Ceramic Quad Flatpack (CQ)	✓	✓	–	✓	–	✓	✓	✓
44-pin J-leaded Cerquad Chip Carrier (JQ)	✓	✓	–	✓	–	✓	✓	–
68-pin J-leaded Cerquad Chip Carrier (JQ)	✓	✓	–	✓	–	✓	✓	–
84-pin J-leaded Cerquad Chip Carrier (JQ)	✓	✓	–	✓	–	✓	✓	–

Applications: C = Commercial, I = Industrial, M = Military, B = MIL-STD-883, E = Extended Flow

Availability: ✓ = Available, P = Planned, – = Not Planned

* Speed Grade: -1 = 15% faster than Standard, -2 = 25% faster than Standard

Device Resources

Device Series	Logic Modules	Gates	User I/Os			
			44-pin	68-pin	84-pin	100-pin
A1010A	295	1200	34	57	57	57
A1020A	547	2000	34	57	69	69

Pin Description

CLK Clock (Input)

TTL Clock input for global clock distribution network. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground (Input)

Input LOW supply voltage.

I/O Input/Output (Input, Output)

I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

MODE Mode (Input)

The MODE pin controls the use of multi-function pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/O.

NC No Connection

This pin is not connected to circuitry within the device.

$\overline{PRA}$ Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed designs confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

$\overline{PRB}$ Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} Supply Voltage (Input)

Input HIGH supply voltage.

V_{PP} Programming Voltage (Input)

Input supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

Absolute Maximum Ratings

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[1]	-0.5 to +7.0	Volts
V_I	Input Voltage	-0.5 to V_{CC} +0.5	Volts
V_O	Output Voltage	-0.5 to V_{CC} +0.5	Volts
I_{IK}	Input Clamp Current	±20	mA
I_{OK}	Output Clamp Current	±20	mA
I_{OK}	Continuous Output Current	±25	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.

Note:

1. $V_{PP} = V_{CC}$, except during device programming.

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to +70	-40 to +85	-55 to +125	°C
Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. Ambient temperature (T_A) used for commercial and industrial; case temperature (T_C) used for military.

Electrical Specifications

Parameter		Commercial		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = -4 mA)	3.84						V
	(I_{OH} = -3.2 mA)			3.7		3.7		V
V_{OL}[1]	(I_{OL} = 4 mA)		0.33		0.40		0.40	V
V_{IL}		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500		500	ns
C_{IO} I/O Capacitance[2, 3]			10		10		10	pF
Standby Current, I_{CC}[4]			10		20		25	mA
Leakage Current[5]		-10	10	-10	10	-10	10	µA
I_{OS} Output Short Circuit Current[6]	(V_O = V_{CC})	20	140	20	140	20	140	mA
	(V_O = GND)	-10	-100	-10	-100	-10	-100	mA

Notes:

1. Only one output tested at a time. V_{CC} = min.
2. Not tested, for information only.
3. Includes worst-case 84-pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.
4. Typical standby current = 3 mA. All outputs unloaded. All inputs = V_{CC} or GND.
5. V_O, V_{IN} = V_{CC} or GND.
6. Only one output tested at a time. Min. at V_{CC} = 4.5 V; Max. at V_{CC} = 5.5 V.

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the maximum power dissipation for an 84-pin plastic leaded chip carrier at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp. (°C)}}{\theta ja\ (°C/W)} = \frac{150°C - 70°C}{44°C/W} = 1.82\ W$$

Package Type	Pin Count	θjc	θja Still air	θja 300 ft/min.	Units
Plastic J-leaded Chip Carrier	44	15	52	40	°C/W
	68	13	45	35	°C/W
	84	12	44	33	°C/W
Plastic Quad Flatpack	100	13	55	47	°C/W
Ceramic Pin Grid Array	84	8	33	20	°C/W
Ceramic Quad Flatpack	84	5	40	30	°C/W
J-leaded Cerquad Chip Carrier	44	8	38	30	°C/W
	68	8	35	25	°C/W
	84	8	34	24	°C/W

Power Dissipation

The following formula is used to calculate total device dissipation.

Total Device Power (mW) = (0.20 x N x F1) + (0.085 x M x F2) + (0.80 x P x F3)

Where:

- F1 = Average logic module switching rate in MHz
- F2 = CLKBUF macro switching rate in MHz
- F3 = Average I/O module switching rate in MHz
- M = Number of logic modules connected to the CLKBUF macro
- N = Total number of logic modules used in the design (including M)
- P = Number of outputs loaded with 50 pF

Average switching rate of logic modules and of I/O modules is some fraction of the device operating frequency (usually CLKBUF). Logic modules and I/O modules switch states (from low-to-high or from high-to-low) only if the input data changes when the module is enabled. A conservative estimate for average logic module and I/O module switching rates (variables F1 and F3, respectively) is 10% of device clock driver frequency.

If the CLKBUF macro is not used in the design, eliminate the second term (including F2 and M variables) from the formula.

Sample A1020 Device Power Calculation

To illustrate the power calculation, consider a large design operating at high frequency. This sample design utilizes 85% of available logic modules on the A1020-series device (.85 x 547 = 465 logic modules used). The design contains 104 flip-flops (208 logic modules). Operating frequency of the design is 16 MHz. In this design, the CLKBUF macro drives the clock network. Logic modules and I/O modules are switching states at approximately 10% of the clock frequency rate (.10 x 16 MHz = 1.6 MHz). Sixteen outputs are loaded with 50 pF.

To summarize the design described above: N = 464; M = 208; F2 = 16; F1 = 4; F3 = 4; P = 16. Total device power can be calculated by substituting these values for variables in the device dissipation formula.

Total device power for this example =

(0.20 x 465 x 1.6) + (0.085 x 208 x 16) + (0.80 x 16 x 1.6) = 452 mW

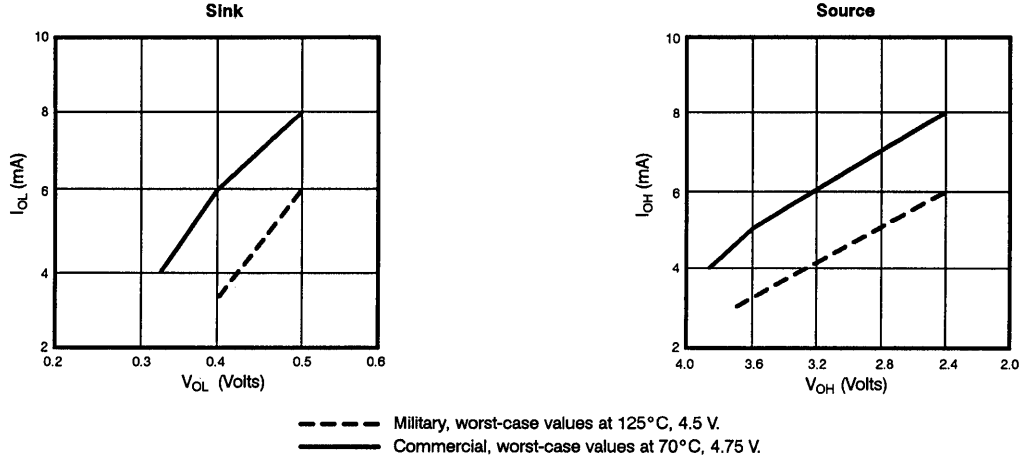
Functional Timing Tests

AC timing for logic module internal delays is determined after place and route. The ALS Timer utility displays actual timing parameters for circuit delays. ACT 1 devices are AC tested to a "binning" circuit specification.

The circuit consists of one input buffer + n logic modules + one output buffer (n=16 for A1010A; n=28 for A1020A). The logic modules are distributed along two sides of the device, as inverting or non-inverting buffers. The modules are connected through programmed antifuses with typical capacitive loading.

Propagation delay [$t_{PD} = (t_{PLH} + t_{PHL})/2$] is tested to the following AC test specifications.

Output Buffer Performance Derating



Note:
The above curves are based on characterizations of sample devices and are not completely tested on all devices.

Timing Derating

Operating temperature, operating voltage, and device processing conditions, along with device die size and speed grade, account for variations in array timing characteristics. These variations are summarized into a derating factor for ACT 1 array typical timing specifications. The derating factors shown in the table below are based on the recommended operating conditions for ACT 1 commercial, industrial, and military applications. The derating curves show worst-to-best case operating voltage range and best-to-worst case operating temperature range.

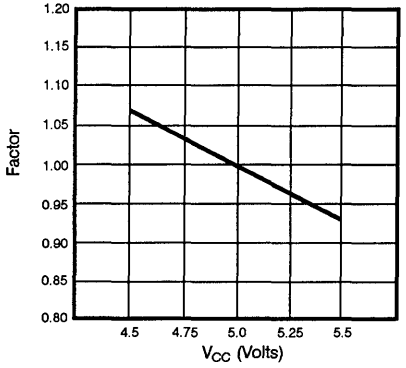
Timing Derating Factor (x typical)

	Commercial		Industrial		Military	
Device	**Best-Case**	**Worst-Case**	**Best-Case**	**Worst-Case**	**Best-Case**	**Worst-Case**
A1010A, A1020A						
Standard Speed	0.45	1.54	0.40	1.65	0.37	1.79
-1 Speed Grade	0.45	1.28	0.40	1.37	0.37	1.49
-2 Speed Grade	0.45	1.13	0.40	1.20	0.37	1.32

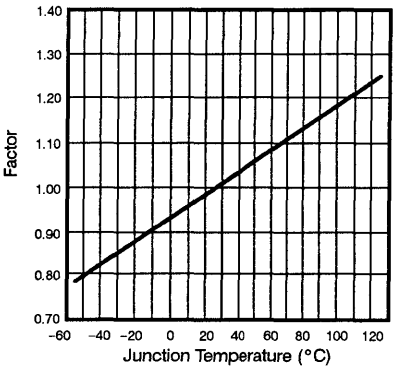
Note:

"Best-case" reflects maximum operating voltage, minimum operating temperature, and best-case processing. "Worst-case" reflects minimum operating voltage, maximum operating temperature, and worst-case processing. Best-case derating is based on sample data only and is not guaranteed.

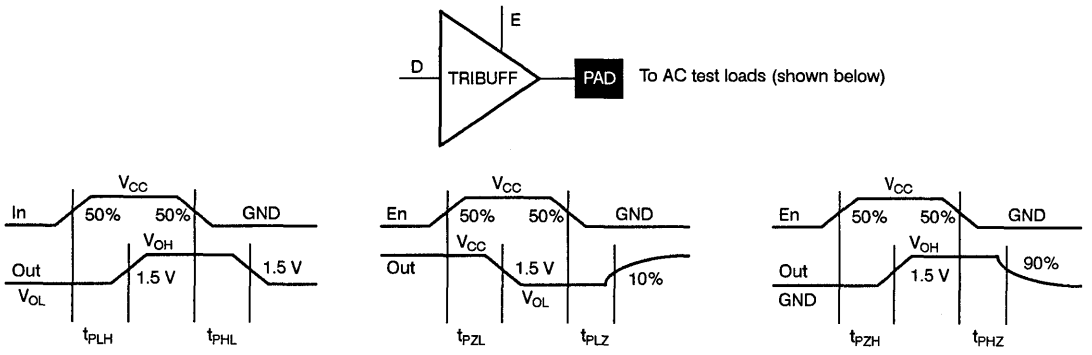
Voltage Derating Curve



Temperature Derating Curve

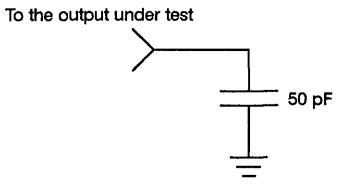


Output Buffer Delays

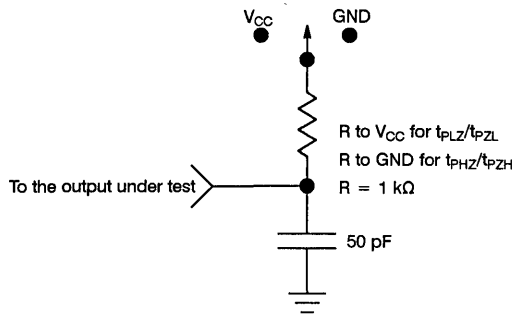


AC Test Loads

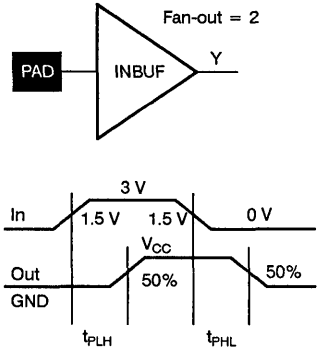
Load 1
(Used to measure propagation delay)



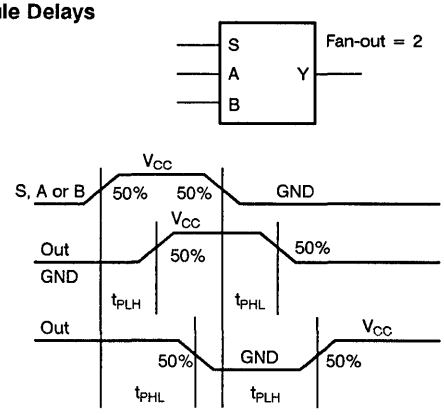
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

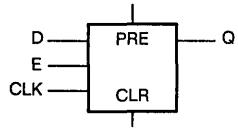


Module Delays

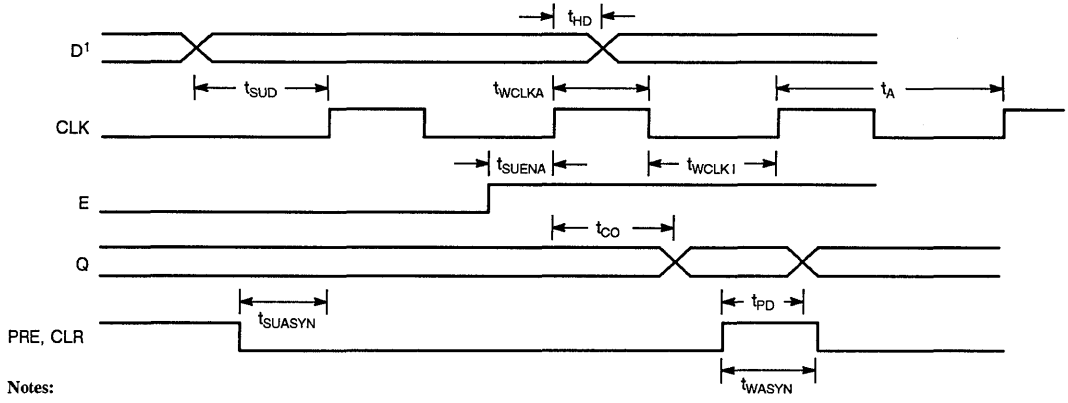


Sequential Timing Characteristics

Flip-Flops and Latches



(Positive edge triggered)



Notes:

1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

Timing Characteristics

Timing is design-dependent; actual delay values are determined after place and route of the design using the ALS Timer utility. The following delay values use statistical estimates for wiring delays based on 85% to 90% module utilization. Device utilization above 95% will result in performance degradation.

With ALS place and route programs, the user can assign criticality level to a net, based on timing requirements. Delays for both typical and critical (speed-sensitive) nets are given below. Most nets will fall into the "typical" category.

Less than 1% of all routing in a design requires the use of "long tracks." Long tracks, long vertical or horizontal routing paths, are used by the autorouter only as needed. Delays due to the use of long tracks range from 15 ns to 35 ns. Long tracks may be used to route the least critical nets in a given design.

Logic Module Timing

V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; t_{PD} = 3.0 ns @ FO = 0

Single Logic Module Macros
(e.g., most gates, latches, multiplexors)[1]

Parameter	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD}	Critical	5.4	5.8	6.2	8.5	Note 2	ns
t_{PD}	Typical	6.3	6.7	7.7	8.6	10.8	ns

Dual Logic Module Macros
(e.g., adders, wide input gates)[1]

Parameter	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD}	Critical	9.2	9.6	10.0	12.3	Note 2	ns
t_{PD}	Typical	10.2	10.6	11.6	12.5	14.6	ns

Sequential Element Timing Characteristics

Parameter		Fan-Out					Units
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{SU}	Set Up Time, Data Latches	3.5	3.9	4.2	4.5	4.8	ns
t_{SU}	Set Up Time, Flip-Flops	3.9	3.9	3.9	3.9	3.9	ns
t_H	Hold Time	0	0	0	0	0	ns
t_W	Pulse Width, Minimum[3]	7.7	8.5	9.2	10.0	14.0	ns
t_{CQ}	Delay, Critical Net	5.4	5.8	6.2	8.5	Note 2	ns
t_{CQ}	Delay, Typical Net	6.3	6.7	7.7	8.6	10.8	ns

Notes:
1. Most flip-flops exhibit single module delays.
2. Critical nets have a maximum fan-out of six.
3. Minimum pulse width, t_W, applies to CLK, PRE, and CLR inputs.

I/O Buffer Timing

V_{CC} = 5.0 V; T_J = 25°C; Process = Typical

INBUF Macros

Parameter	From - To	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PHL}	Pad to Y	6.9	7.6	8.9	10.7	14.3	ns
t_{PLH}	Pad to Y	5.9	6.5	7.7	8.4	12.4	ns

CLKBUF (High Fan-Out Clock Buffer) Macros

Parameter	FO = 40	FO = 160	FO = 320	Units
t_{PHL}	9.0	12.0	15.0	ns
t_{PLH}	9.0	12.0	15.0	ns

Notes:

1. A clock balancing feature is provided to minimize clock skew.
2. There is no limit to the number of loads that may be connected to the CLKBUF macro.

OUTBUF, TRIBUFF, and BIBUF Macros[1]

C_L = 50 pF

Parameter	From - To	CMOS	TTL	Units
t_{PHL}	D to Pad	3.9	4.9	ns
t_{PLH}	D to Pad	7.2	5.7	ns
t_{PHZ}	E to Pad	5.2	3.4	ns
t_{PZH}	E to Pad	6.5	4.9	ns
t_{PLZ}	E to Pad	6.9	5.2	ns
t_{PZL}	E to Pad	4.9	5.9	ns

Change in Propagation Delay with Load Capacitance[2]

Parameter	From - To	CMOS	TTL	Units
t_{PHL}	D to Pad	0.03	0.046	ns/pF
t_{PLH}	D to Pad	0.07	0.039	ns/pF
t_{PHZ}	E to Pad	0.08	0.046	ns/pF
t_{PZH}	E to Pad	0.07	0.039	ns/pF
t_{PLZ}	E to Pad	0.07	0.039	ns/pF
t_{PZL}	E to Pad	0.03	0.039	ns/pF

Notes:

1. The BIBUF macro input section exhibits the same delays as the INBUF macro.
2. Load capacitance delay delta can be extrapolated down to 15 pF minimum.

   Example:

   Delay for OUTBUF driving a 100-pF TTL load:

   t_{PHL} = 4.9 + (.046 x (100–50)) = 4.9 + 2.3 = 7.2 ns

   t_{PLH} = 5.7 + (.039 x (100–50)) = 5.7 + 2.0 = 7.7 ns

Soft Macro Library Overview

Macro Name	Modules Required	Description	Levels of Logic
Counters			
CNT4A	17	4-bit loadable binary counter with clear	4
CNT4B	15	4-bit loadable bin counter w/ clr, active low carry in & carry out	4
UDCNT4A	24	4-bit up/down cntr w/ sync active low load, carry in & carry out	6
Decoders			
DEC2X4	4	2 to 4 decoder	1
DEC2X4A	4	2 to 4 decoder with active low outputs	1
DEC3X8	8	3 to 8 decoder	1
DEC3X8A	8	3 to 8 decoder with active low outputs	1
DEC4X16A	20	4 to 16 decoder with active low outputs	2
DECE2X4	4	2 to 4 decoder with enable	1
DECE2X4A	4	2 to 4 decoder with enable and active low outputs	1
DECE3X8	11	3 to 8 decoder with enable	2
DECE3X8A	11	3 to 8 decoder with enable and active low outputs	2
Latches and Registers			
DLC8A	8	Octal latch with clear	1
DLE8	8	Octal latch with enable	1
DLM8	8	Octal latch with mulitplexed inputs	1
REGE8A	20	Octal register with preset and clear, active high enable	2
REGE8B	20	Octal register with active low clock, preset and clear, active high enable	2
Adders			
FA1	3	One bit full adder	3
FADD8	37	8-bit fast adder	4
FADD12	62	12-bit fast adder	5
FADD16	78	16-bit fast adder	5
FADD24	120	24-bit fast adder	6
FADD32	160	32-bit fast adder	7
Comparators			
ICMP4	5	4-bit identity comparator	2
ICMP8	9	8-bit identity comparator	3
MCMP16	93	16-bit magnitude comparator	5
MCMPC2	9	2-bit magnitude comparator with enables	3
MCMPC4	18	4-bit magnitude comparator with enables	4
MCMPC8	36	8-bit magnitude comparator with enables	6
Multiplexors			
MX8	3	8 to 1 multiplexor	2
MX8A	3	8 to 1 multiplexor with an active low output	2
MX16	5	16 to 1 multiplexor	2
Multipliers			
SMULT8	235	8 x 8 two's complement multiplier	Varies

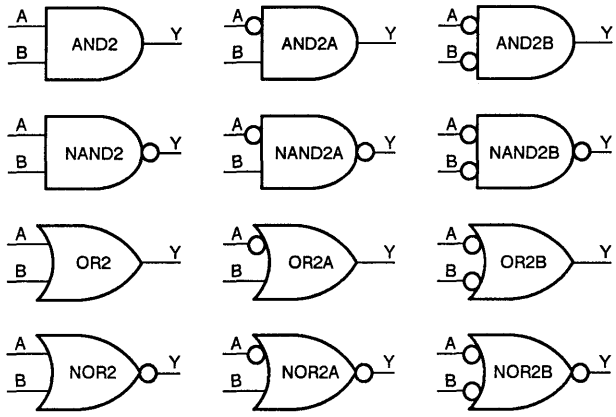
Soft Macro Library Overview (continued)

Macro Name	Modules Required	Description	Levels of Logic
Shift Registers			
SREG4A	8	4-bit shift register with clear	2
SREG8A	18	8-bit shift register with clear	2
TTL Replacements			
TA138	12	3 to 8 decoder with 3 enables and active low outputs	2
TA139	4	2 to 4 decoder with an enable and active low outputs	1
TA151	5	8 to 1 multiplexor with enable, true, and complementary outputs	3
TA153	2	4 to 1 multiplexor with active low enable	2
TA157	1	2 to 1 multiplexor with enable	1
TA161	22	4-bit sync counter w/ load, clear, count enables & ripple carry out	3
TA164	18	8-bit serial in, parallel out shift register	1
TA169	25	4-bit synchronous up / down counter	6
TA181	31	4-bit ALU	4
TA194	14	4-bit shift register	1
TA195	10	4-bit shift register	1
TA269	50	8-bit up/down cntr w/ clear, load, ripple carry output & enables	8
TA273	18	Octal register with clear	1
TA280	9	Parity generator and checker	4
TA377	16	Octal register with active low enable	1
Super Macros			
MC	102	DRAM Controller	Varies
DMA	225	Direct Memory Access Controller	Varies
SINT	180	SCSI Interface Controller	Varies

Hard Macro Library Overview

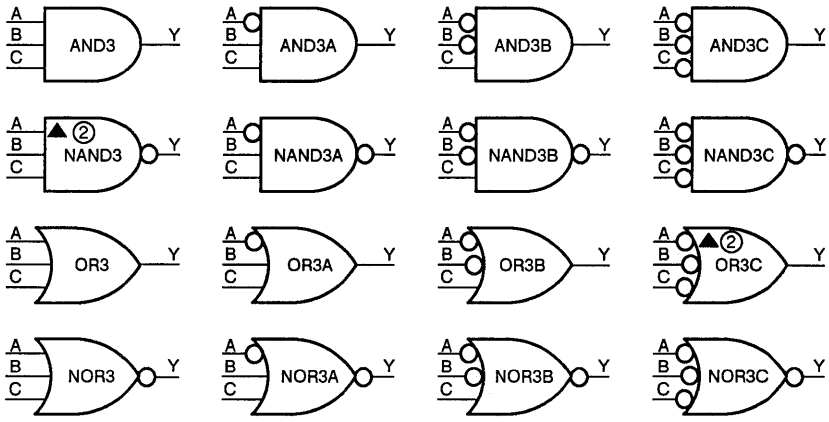
The following illustrations show all the available Hard Macros.

2-Input Gates (Module Count = 1)



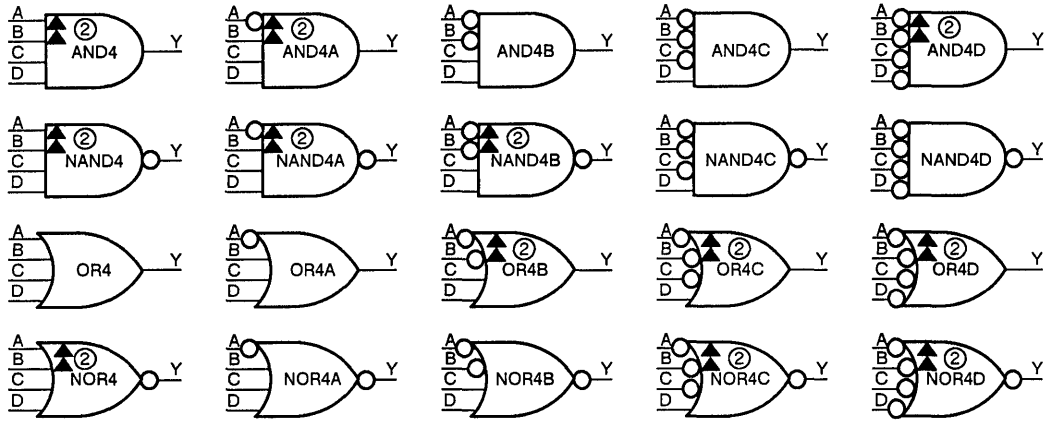
3-Input Gates (Module Count = 1, unless indicated otherwise)

② Indicates 2-module macro
▲ Indicates extra delay input

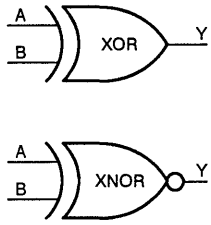


4-Input Gates (Module Count = 1, unless indicated otherwise)

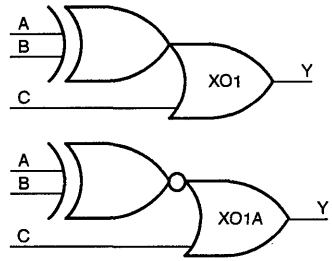
② Indicates 2-module macro
▲ Indicates extra delay input



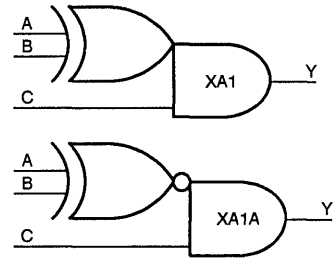
XOR Gates
(Module Count = 1)



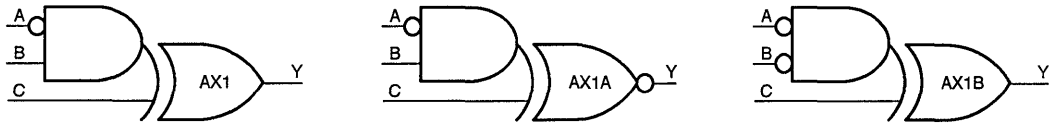
XOR-OR Gates
(Module Count = 1)



XOR-AND Gates
(Module Count = 1)

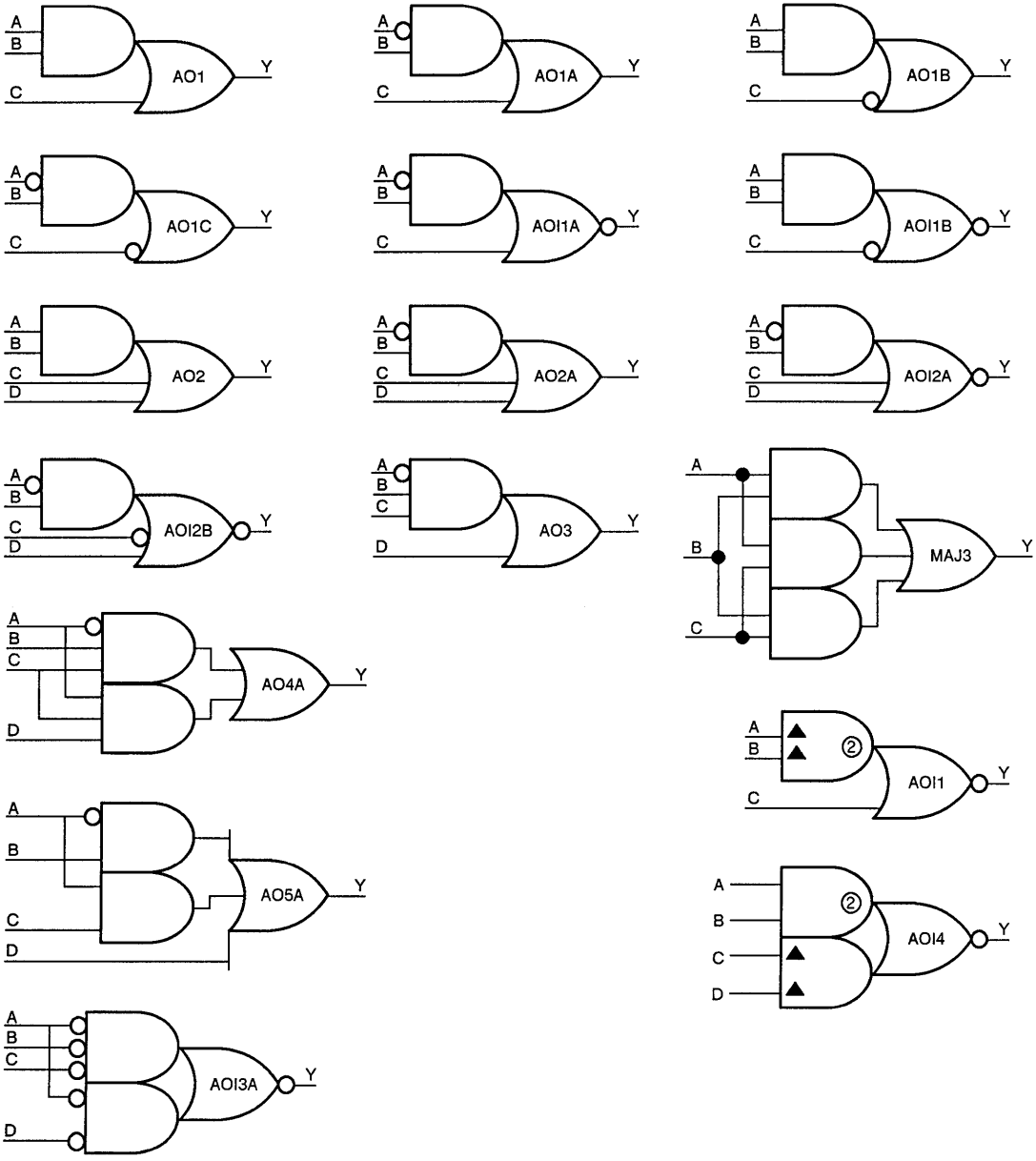


AND-XOR Gates
(Module Count = 1)



AND-OR Gates (Module Count = 1)

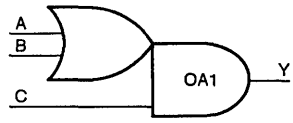
② Indicates 2-module macro
▲ Indicates extra delay input

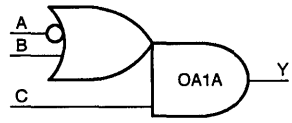


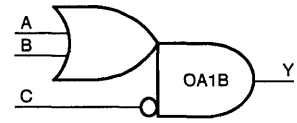
1

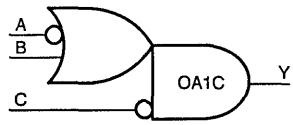
OR-AND Gates (Module Count = 1)

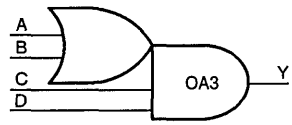
② Indicates 2-module macro
▲ Indicates extra delay input

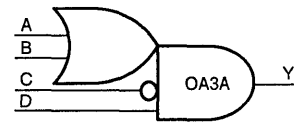


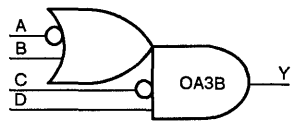


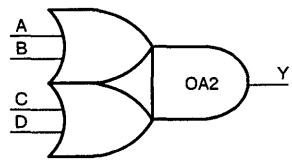


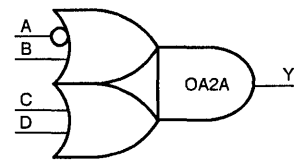


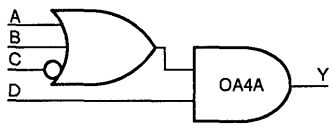


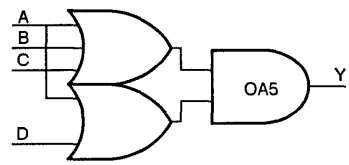


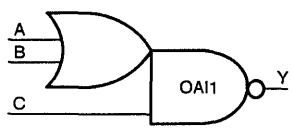


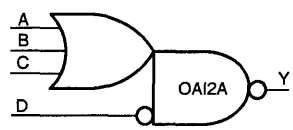


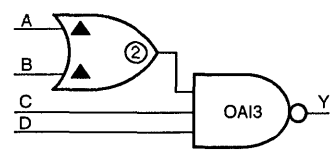




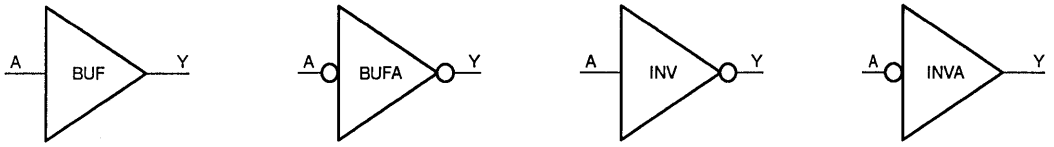




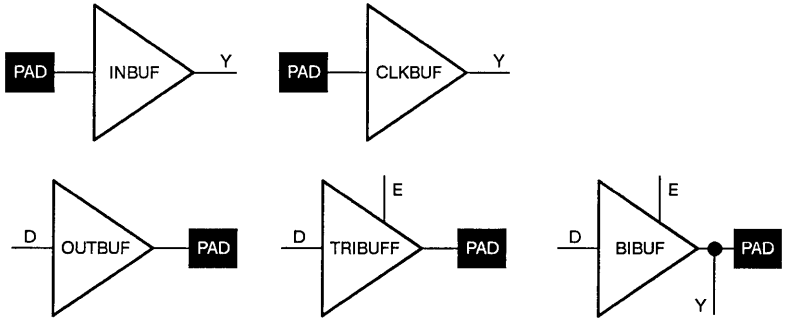




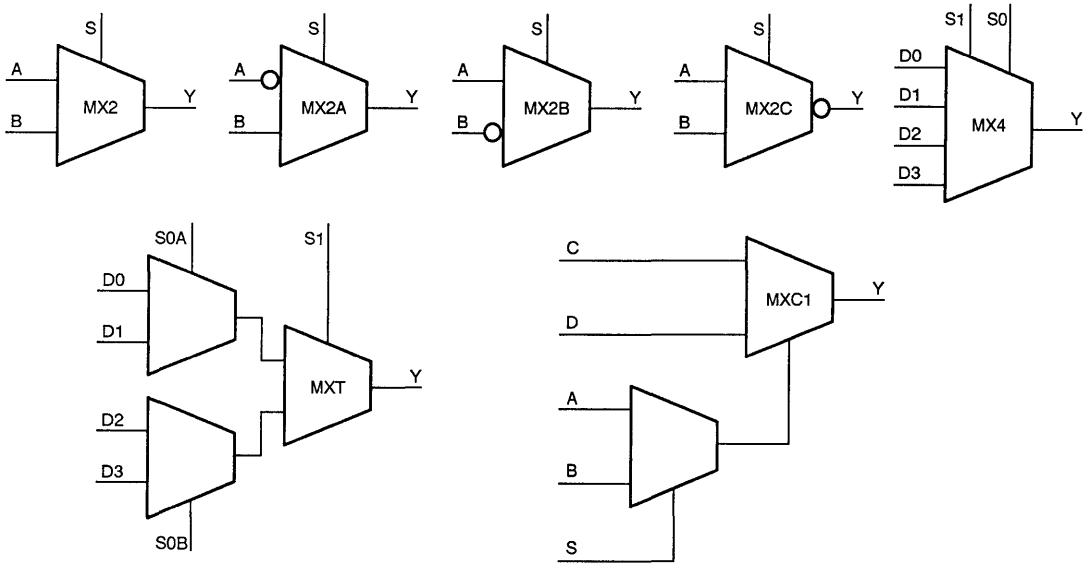
Buffers (Module Count = 1)



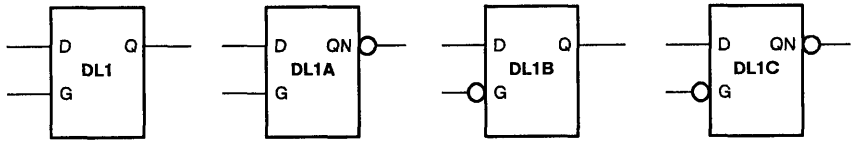
I/O Buffers (I/O Module Count = 1)



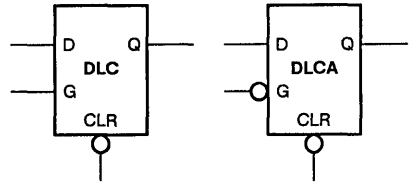
Multiplexors (Module Count = 1)



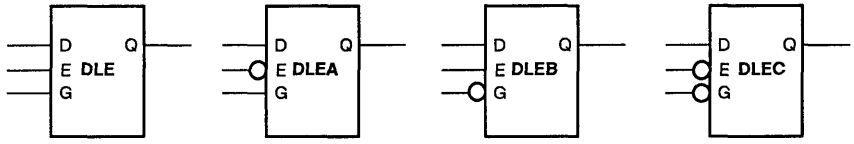
Latches (Module Count = 1)



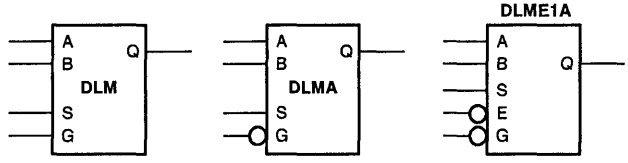
D-Latches with Clear (Module Count = 1)



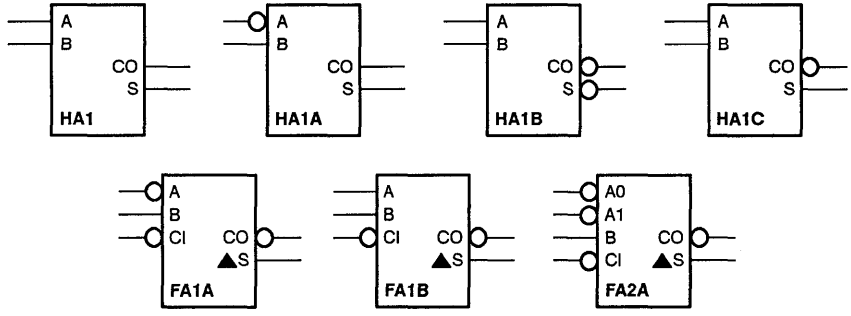
D-Latches with Enable (Module Count = 1)



Mux Latches (Module Count = 1)

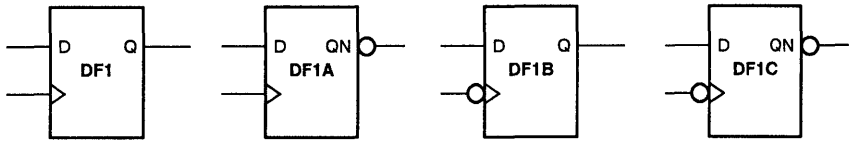


Adders (Module Count = 2)

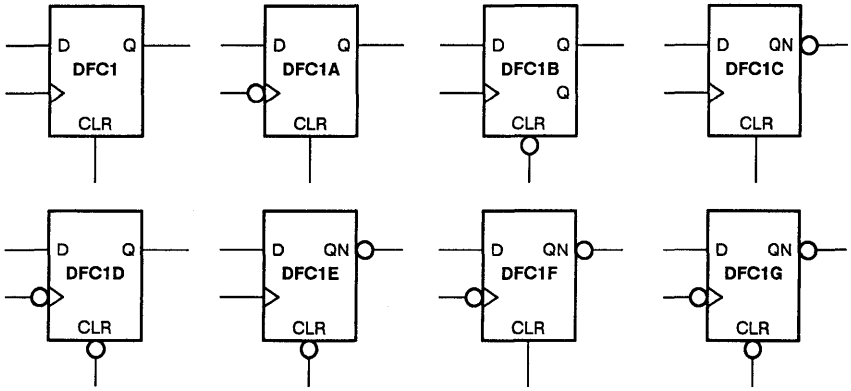


Macros FA1A, FA1B, and FA2A have two level delays from the inputs to the S outputs, as indicated by the▲

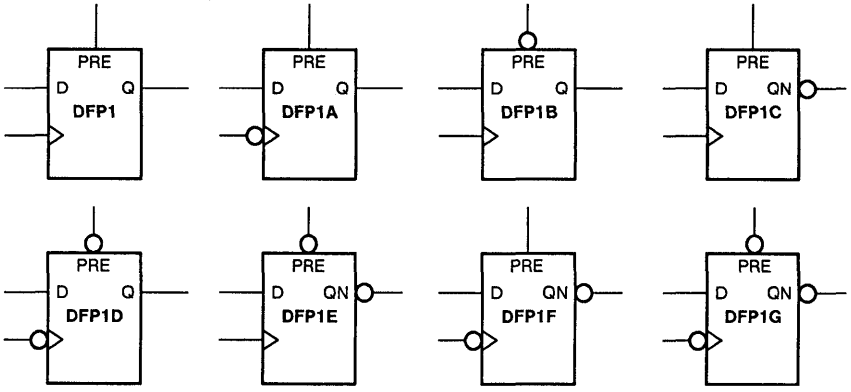
D-Type Flip-Flops (Module Count = 2)



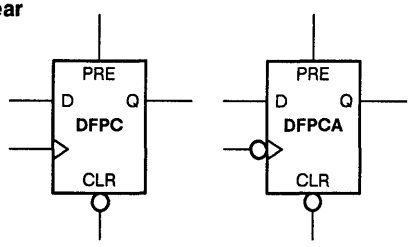
D-Type Flip-Flops with Clear



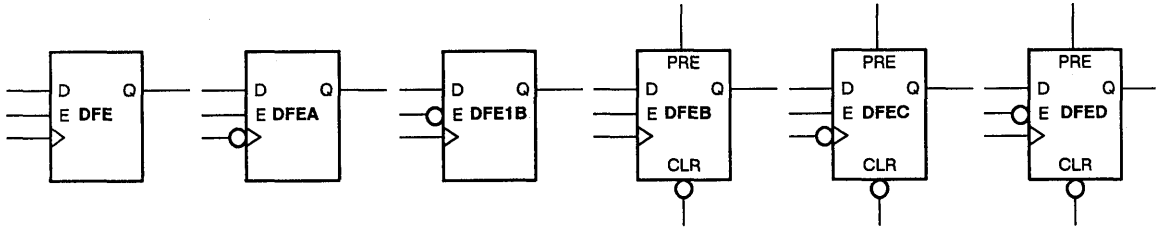
D-Type Flip-Flops with Preset



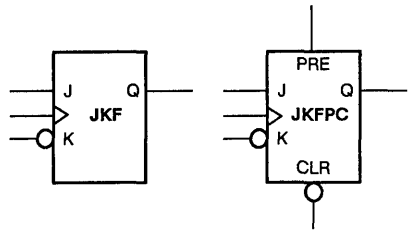
D-Type Flip-Flops with Preset and Clear



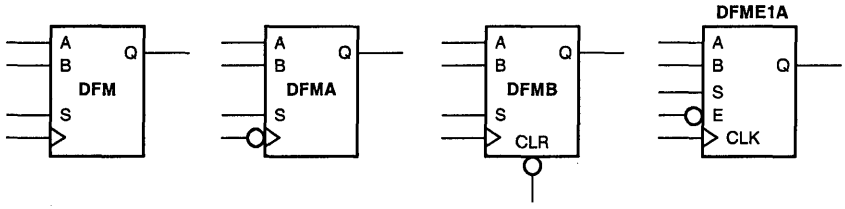
D-Type Flip-Flops with Enable (Module Count = 2)



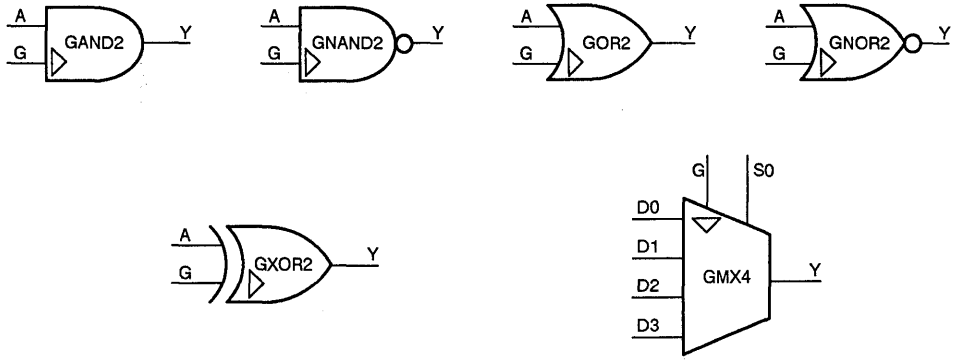
JK Flip-Flops (Module Count = 2)



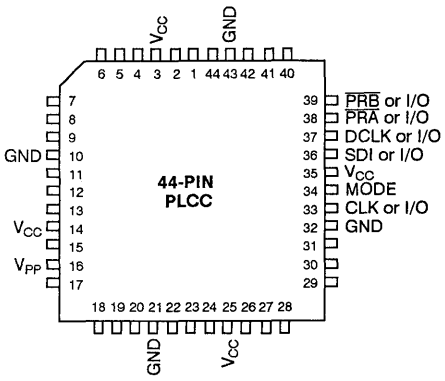
Mux Flip-Flops (Module Count = 2)

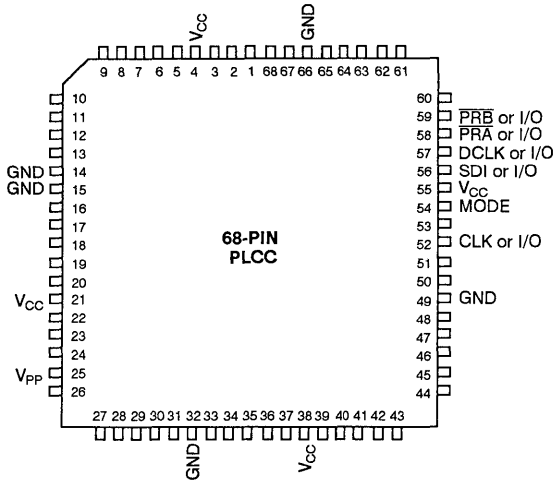


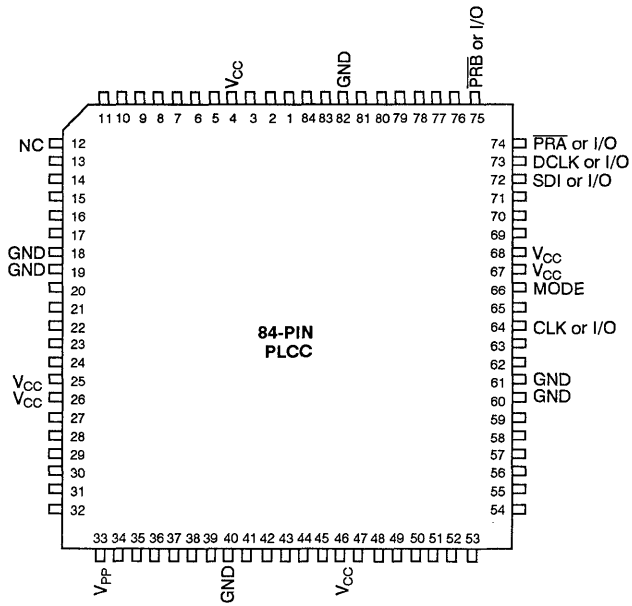
CLKBUF Interface Macros (Module Count = 1)



Package Pin Assignments
(Top View)



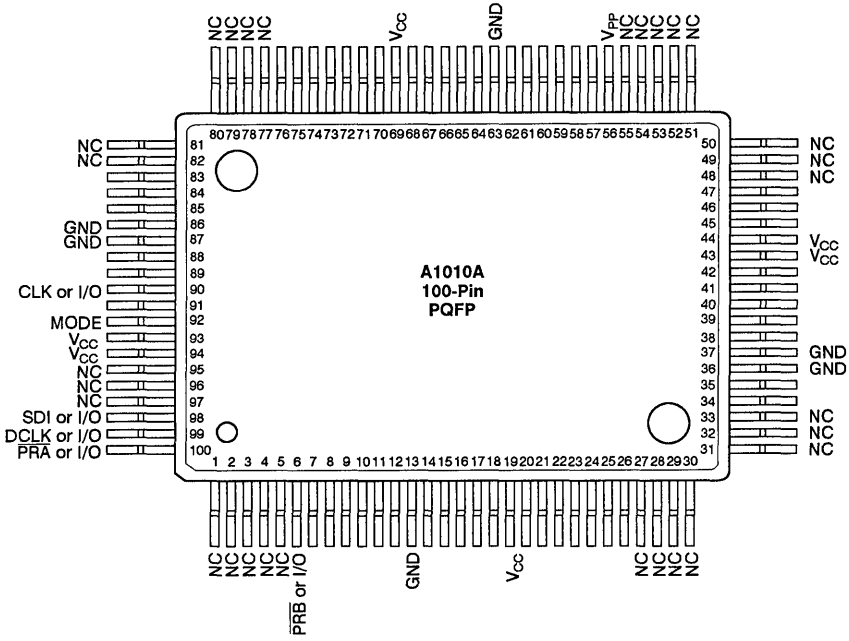


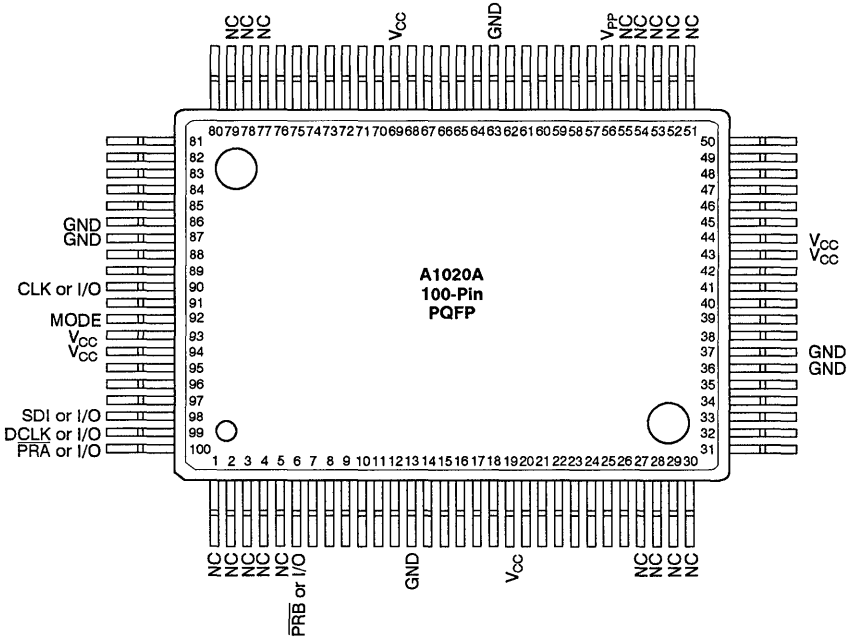


Notes:

1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

Package Pin Assignments (continued)
(Top View)





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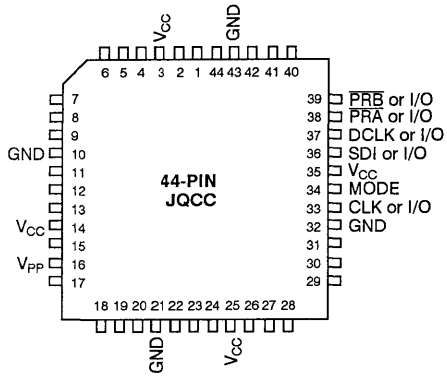
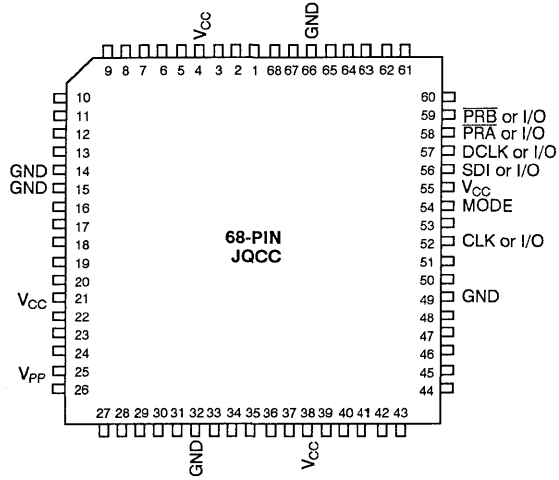
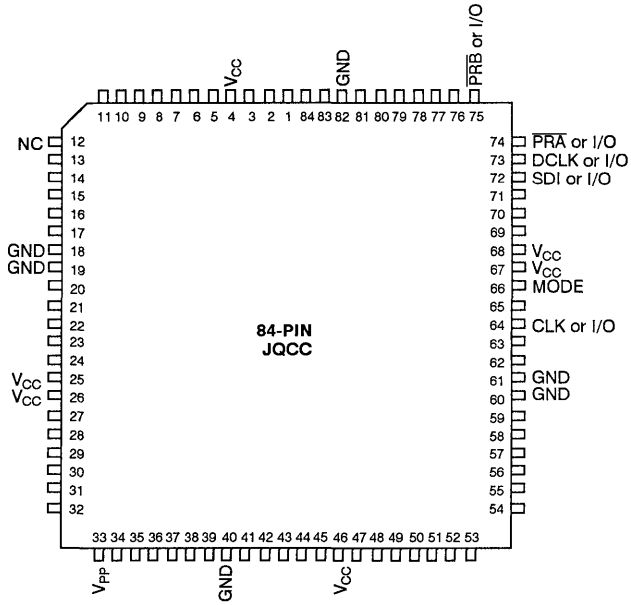
Package Pin Assignments (continued)







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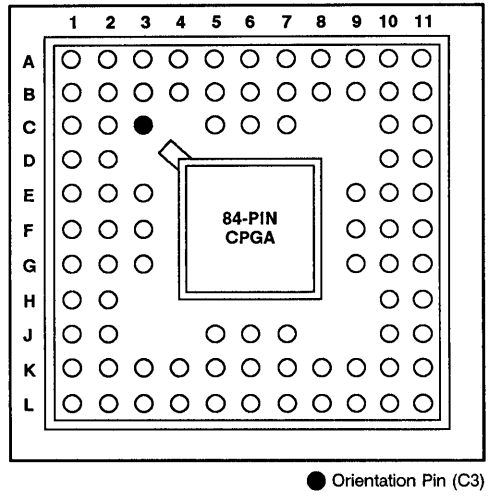
Package Pin Assignments (continued)



Signal	A1010-Series Devices	A1020-Series Devices
$\overline{PRA}$	A11	A11
$\overline{PRB}$	B10	B10
MODE	E11	E11
SDI	B11	B11
DCLK	C10	C10
V_{PP}	K2	K2
CLK or I/O	F9	F9
GND	B7, E2, E3, K5, F10, G10	B7, E2, E3, K5, F10, G10
V_{CC}	B5, F1, G2, K7, E9, E10	B5, F1, G2, K7, E9, E10
N/C (No Connection)	B1, B2, C1, C2, K1, J2, L1, J10, K10, K11, C11, D10, D11	B2

Notes:

1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
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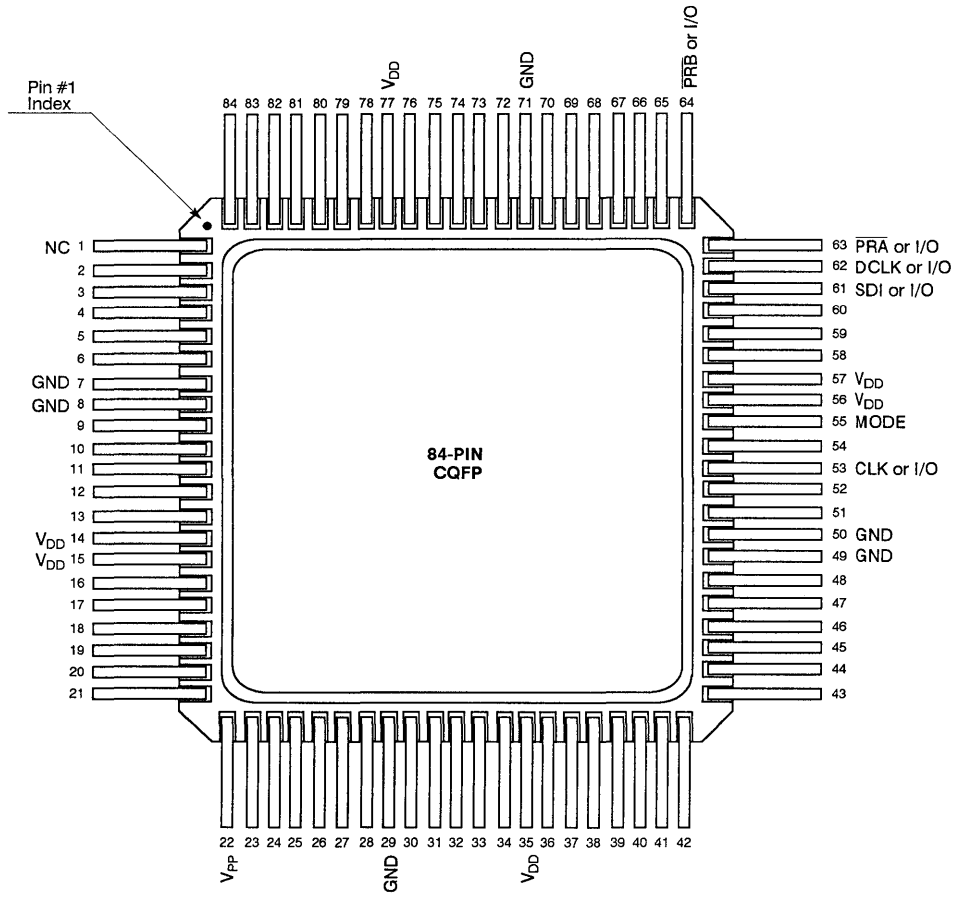
Package Pin Assignments (continued)



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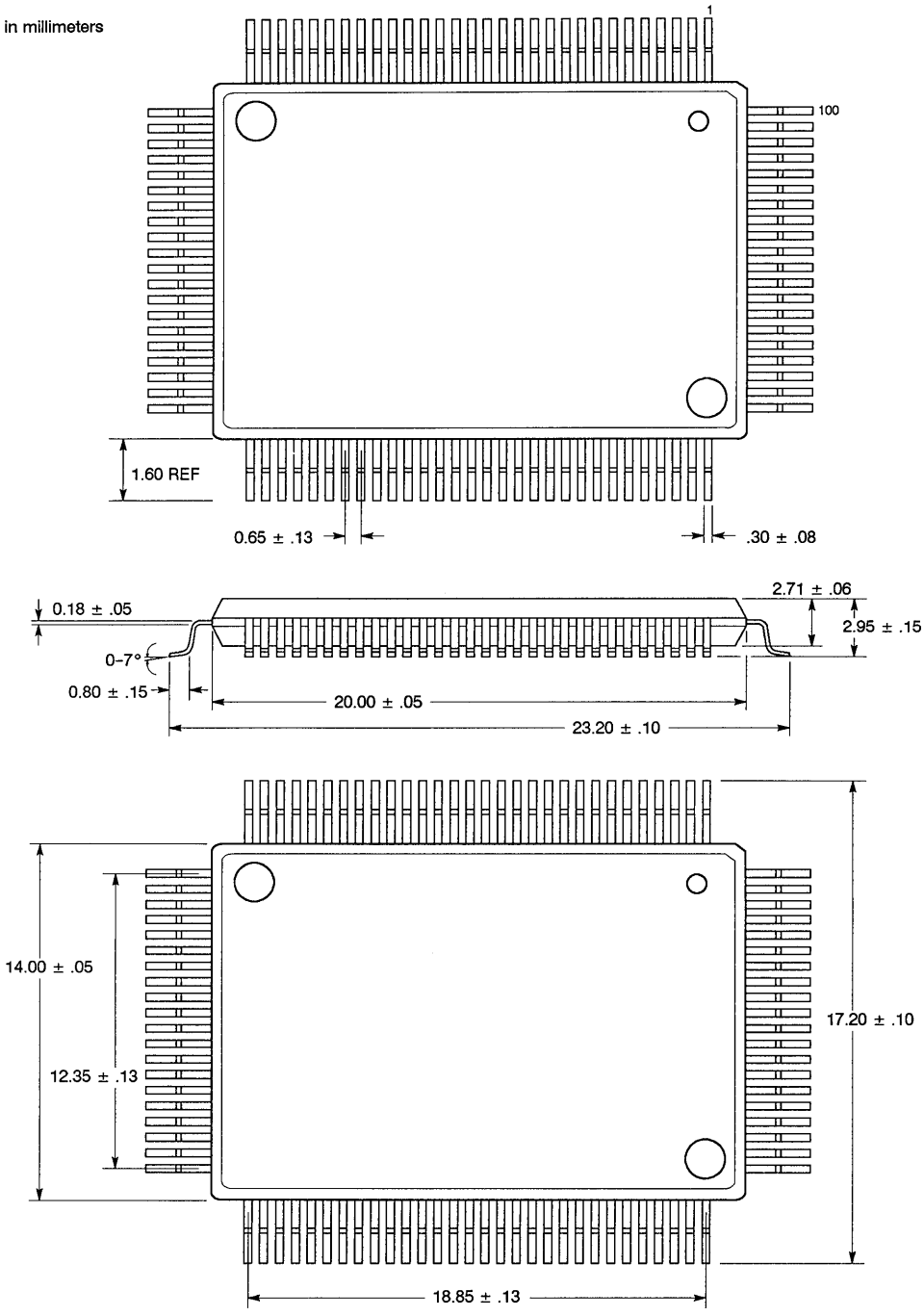
Package Mechanical Details (continued)

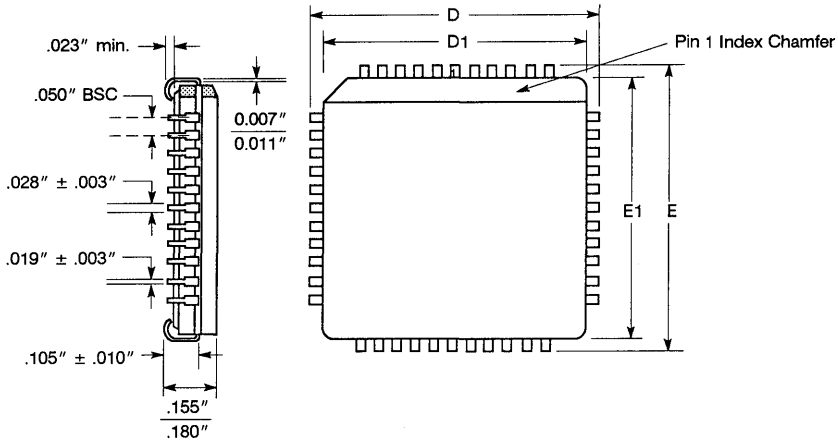
Plastic Quad Flatpack

Dimensions in millimeters



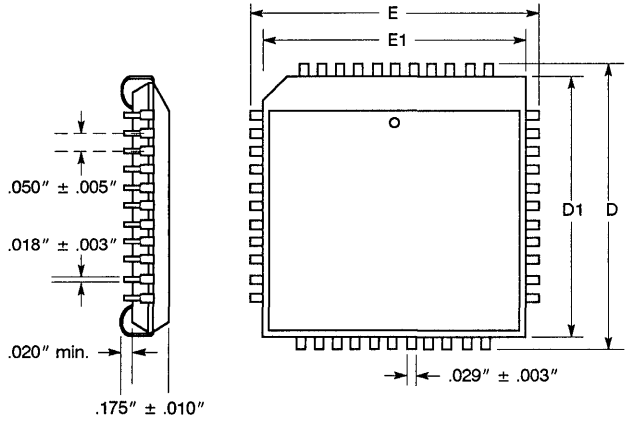
Package Mechanical Details

J-Leaded Cerquad Chip Carrier



Lead Count	D, E	D1, E1
44	.690″ ± .005″	.650″ ± .008″
68	.990″ ± .005″	.950″ ± .008″
84	1.190″ ± .005″	1.150″ ± .008″

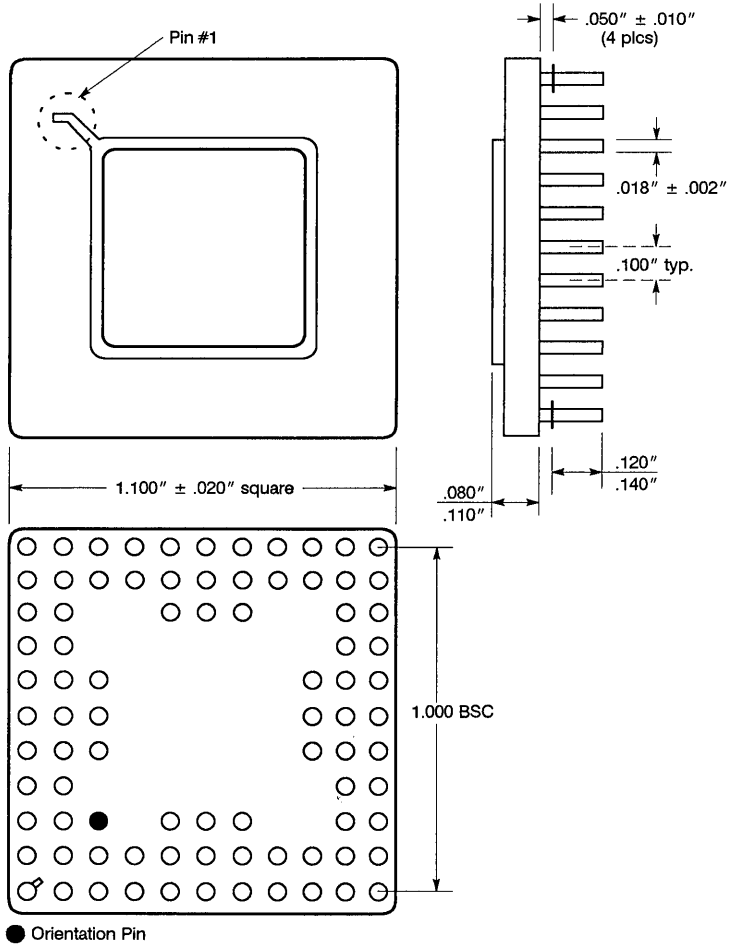
Plastic J-Leaded Chip Carrier



Lead Count	D, E	D1, E1
44	.690″ ± .005″	.655″ ± .005″
68	.990″ ± .005″	.955″ ± .005″
84	1.190″ ± .005″	1.155″ ± .005″

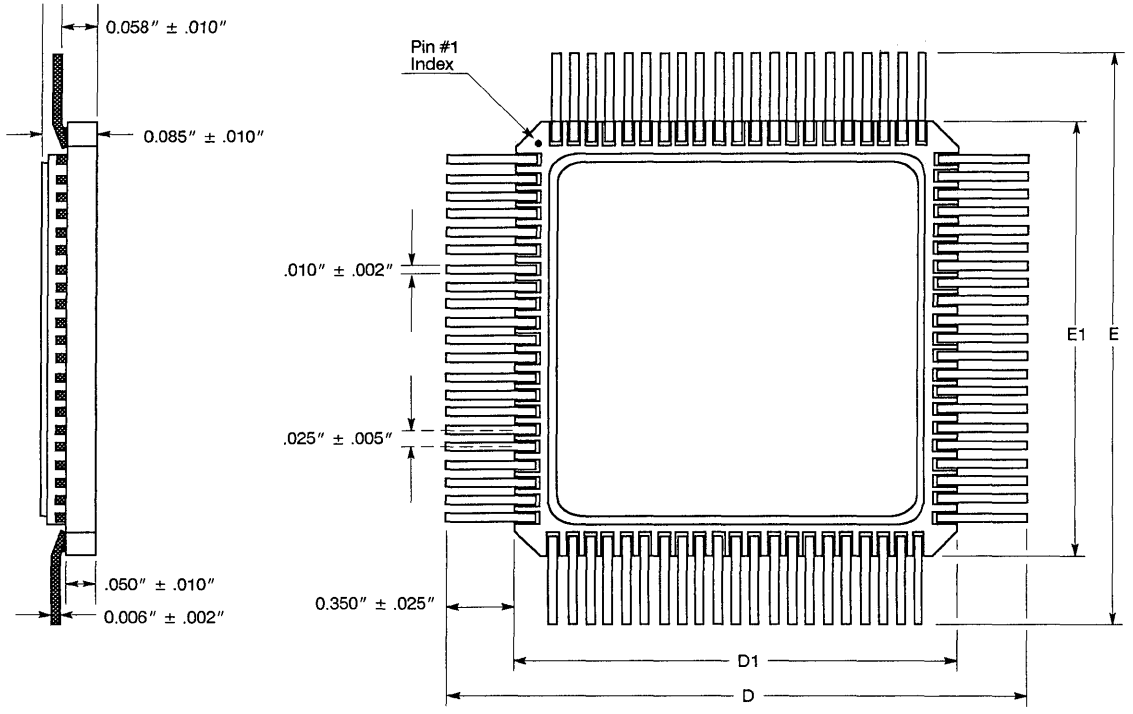
Package Mechanical Details (continued)

Ceramic Pin Grid Array



Package Mechanical Details (continued)

Ceramic Quad Flatpack



Lead Count	D, E	D1, E1
84	1.350″ ± .030″	0.650″ ± .010″

ACT™ 2 Field Programmable Gate Arrays

Features

- Up to 8000 Gate Array Gates (20,000 PLD/LCA™ equivalent gates)
- Replaces up to 210 TTL Packages
- Replaces up to 69 20-Pin PAL Packages
- Design Library with over 250 Macros
- Single-Module Sequential Functions
- Wide-Input Combinatorial Functions
- Up to 1232 Programmable Logic Modules
- Up to 998 Flip-Flops
- 16-Bit Counter Performance to 85 MHz
- 16-Bit Accumulator Performance to 33 MHz
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Two High-Speed, Low-Skew Clock Networks
- I/O Drive to 10 mA
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment

Product Family Profile

Device	A1280	A1240	A1225
Capacity			
Gate Array Equivalent Gates	8,000	4,000	2,500
PLD/LCA Equivalent Gates	20,000	10,000	6,250
TTL Equivalent Packages	210	105	70
20-Pin PAL Equivalent Packages	69	34	23
Logic Modules	1,232	684	451
S-Modules	624	348	231
C-Modules	608	336	220
Flip-Flops (maximum)	998	565	382
Routing Resources			
Horizontal Tracks/Channel	36	36	36
Vertical Tracks/Column	15	15	15
PLICE® Antifuse Elements	750,000	400,000	250,000
User I/Os (maximum)	140	104	83
Packages[1]	176 CPGA 160 PQFP 172 CQFP	132 CPGA 144 PQFP 84 PLCC	100 CPGA 100 PQFP 84 PLCC
Performance[2]			
16-Bit Counters	55 MHz	75 MHz	85 MHz
16-Bit Accumulators	30 MHz	33 MHz	33 MHz
CMOS Process	1.2 µm	1.2 µm	1.2 µm

Note:

1. See product plan for package availability.
2. Performance is based on a -1 speed graded device at commercial worst-case operating conditions.

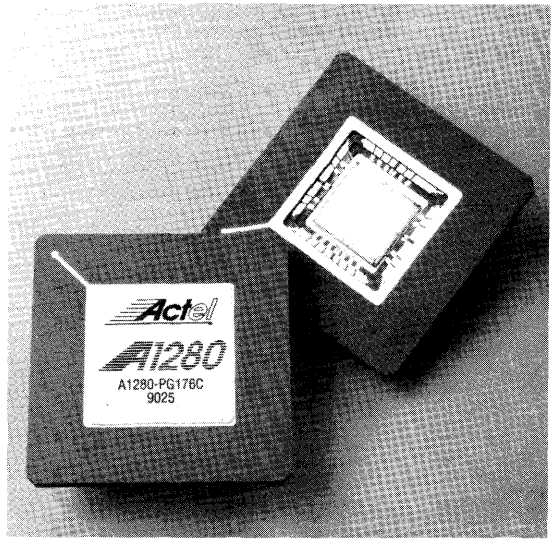


Figure 1. A1280 176-Pin CPGA

Description

The ACT™ 2 family represents Actel's second generation of field programmable gate arrays (FPGAs). The ACT 2 family presents a two-module architecture, consisting of C-Modules and S-Modules. These modules are optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining upward compatibility with the ACT 1 design environment. The devices are implemented in silicon gate, 1.2-µm, two-level metal CMOS, and employ Actel's PLICE antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance and fast time-to-production through user programming. The ACT 2 family is supported by the Action Logic™ System (ALS), which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and debug and diagnostic probe capabilities. The Action Logic System is supported on the following platforms: 386/486 PC and Sun®, HP® and Apollo® workstations. It provides CAE interfaces to the following design environments: Valid™, Viewlogic®, Mentor Graphics®, HP DCS and OrCAD™.

ACT 2 Architecture

This section of the datasheet is meant to familiarize the user with the architecture of ACT 2 family devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. Diagrams for the A1280, A1240, and A1225 are provided at the end of the datasheet. The additional circuitry required to program and test the devices will not be covered.

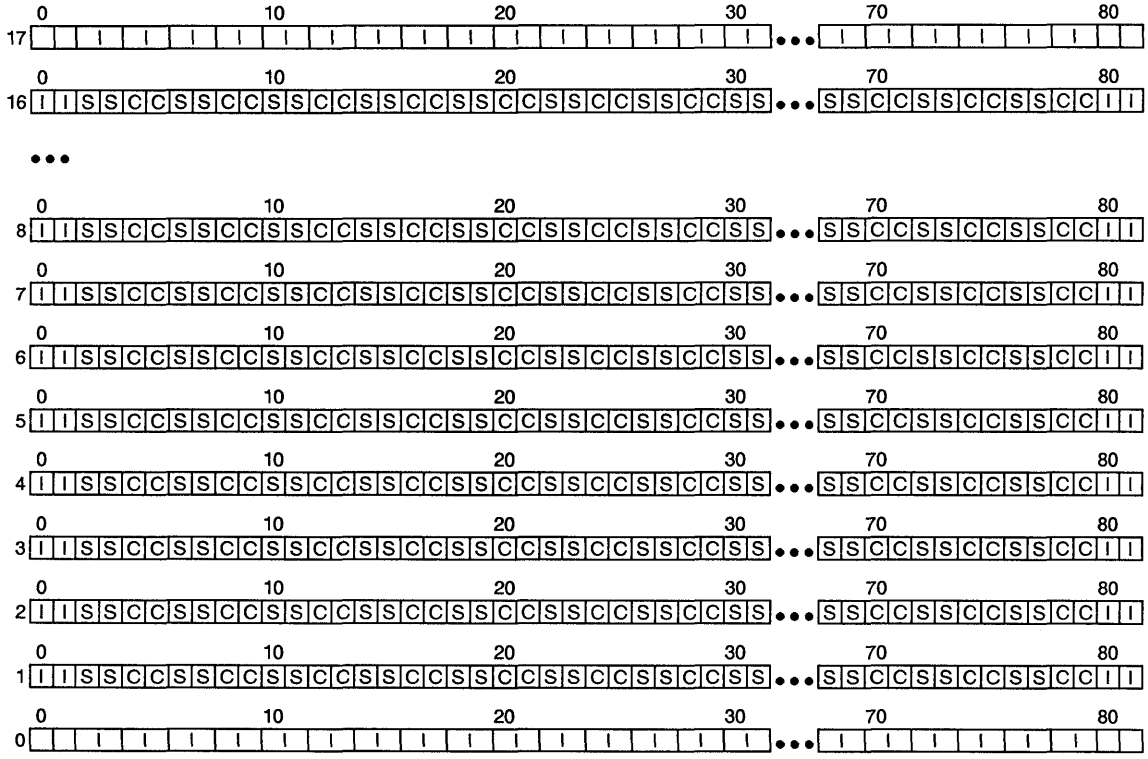
Array Topology

The ACT 2 family architecture is composed of five key elements or building blocks: Logic modules, I/O modules, Routing Tracks, Global Clock Networks, and Probe Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os.

Table 1. Array Sizes

Device	Rows	Columns	Logic	I/O
A1280	18	82	1232	140
A1240	14	62	684	104
A1225	13	46	451	83

The Logic and I/O modules are arranged in a two-dimensional array (Figure 2). There are three types of modules: Logic, I/O, and Bin. Logic and I/O modules are available as user resources. Bin modules are used during testing and are not available to users.



S = Sequential Module, C = Combinatorial Module, I = I/O Module

Figure 2. A1280 Simplified Floor Plan

Logic Modules

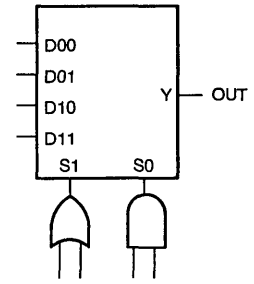
Logic modules are classified into two types: combinatorial C-modules and sequential S-modules (see Figures 3 and 4). The C-module is an enhanced version of the Act 1 family logic module optimized to implement high fan-in combinatorial macros, such as 5-input AND, 5-input OR, etc. The S-module is designed to implement high speed flip-flop functions within a single module. S-modules also include combinatorial logic, which allows an additional level of logic to be implemented without additional propagation delay. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating pairs (shown in Figure 2) and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). I/O-modules are arranged around the periphery of the array.

The combinatorial module (shown in Figure 2) implements the following function:

Z = !S1 * (D00 * !S0 + D01 * S0) + S1 * (D10 * !S0 + D11 * S0)

where:

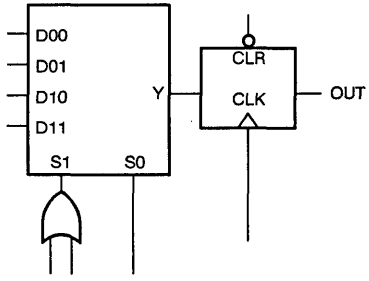
S0 = A0 * B0
S1 = A1 + B1



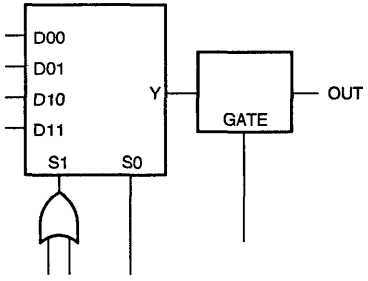
Up to 8-input function

Figure 3. C-Module Implementation

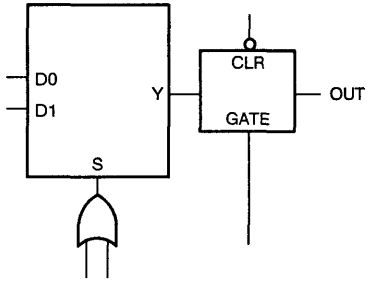
The sequential module implements this same function Z, followed by a sequential block. The sequential block can be configured to implement either a D-type flip-flop or transparent latch. It can also be fully transparent so that S-modules can be used to implement purely combinatorial functions. The function of the sequential module is determined by the macro selection from the design library of hard macros. Allowable S-module implementations are shown in Figure 4.



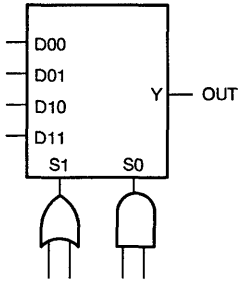
Up to 7-input function plus D-type flip-flop with clear



Up to 7-input function plus latch



Up to 4-input function plus latch with clear



Up to 8-input function (same as C-Module)

Figure 4. S-Module Implementations

I/Os

The I/O architecture consists of pad drivers located near the bonding pads and I/O modules located in the array. Top/bottom I/O modules are located in the top and bottom rows respectively. Side I/O modules occupy the leftmost two columns and the rightmost two columns of the array. The function of all I/O modules is identical, but the top/bottom I/O modules have a different routing interface to the array than the side I/O modules. I/Os implement a variety of user functions determined by library macro selection.

Special Purpose I/Os

Certain I/O pads are temporarily used for programming and testing the device. During normal user operation, these special I/O pads are identical to other I/O pads. The following special I/O pads and their functions, are shown in Table 2.

Table 2. Special I/O Pads

SDI	Serial Data In
SDIO	Serial Data Out
BININ	Binning Circuit In
BINOUT	Binning Circuit Out
DCLK	Serial Data Clock In
PRA	Probe A Output
PRB	Probe B Output

Two other pads, CLKA and CLKB, also differ from normal I/Os in that they can be used to drive the global clock networks. Power, Ground, and Programming pads are not considered I/O functions. Their function is summarized as follows:

VCCA, VCCQ, VCCI	Power
GNDA, GNDQ, GNDI	Circuit Ground
VSV, VKS	Programming Pads
MODE	Program/Debug Control

I/O Pads

I/O pads are located on the periphery of the die and consist of the bonding pad, the high-drive CMOS drivers, and the TTL level-shifter inputs. Each I/O pad is associated with a specific I/O module. Connections form the I/O pad to the I/O module are made using the signals DATAOUT, DATAIN and EN (shown in Figure 5).

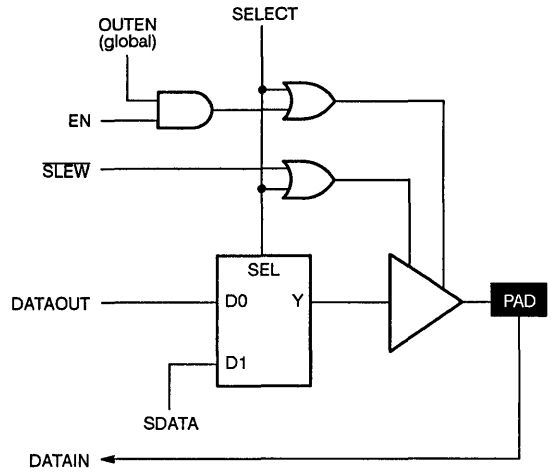


Figure 5. I/O Pad Signals

I/O Modules

There are two types of I/O modules: side and top/bottom. The I/O module schematic is shown in Figure 6. In the side I/O modules, there are two inputs supplying the data to be output from the chip: UO1 and UO2. (UO stands for user output). Two are used so that the router can choose to take the signal from either the routing channel above or the routing channel below the I/O module. The top/bottom I/O modules interact with only one channel and therefore have only one UO input.

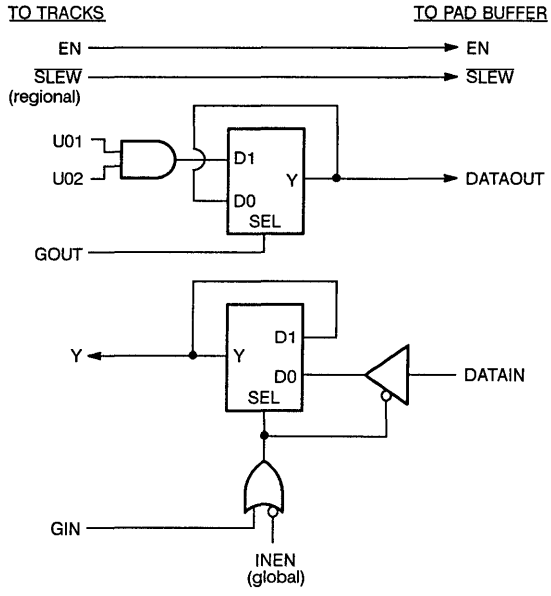


Figure 6. I/O Module

The EN input enables the tristate output buffer. The global signals INEN and OUTEN (Figure 5) are used to disable the inputs and outputs during certain test modes. Latches are provided in the input and output path. When GOUT is low, the output signal on UO1/UO2 is latched. When it is high, the latch is transparent. The latch can be used as the second stage of a rising-edge flip-flop as described in the Applications note accompanying this data sheet. GIN is the reverse of GOUT. When GIN is high, the input data is latched; when it is low, the input latch becomes transparent.

The output of the module, Y, is used for data being input to the chip. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below it (similar to logic modules). Side I/O modules may also connect to the array through nondedicated Long Vertical Tracks (LVTs). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom must be routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section). As a result, I/O signals connected to I/O modules on either the top or bottom of the array may incur a slight delay penalty (~1nS) over signals connected to I/O modules on the sides.

Hard Macros

Designing within the Actel design environment is accomplished using a building block approach. Over 250 logic function macros are provided in the ACT 2 design library. Hard macro logic functions range from simple SSI gates such as AND, NOR, and Exclusive OR to more complex functions such as flip-flops with 4:1 Multiplexed Data inputs. Hard macros are implemented in the ACT 2 architecture by using one or more C-modules or S-modules. Over 150 of the macros are implemented in a single module, while several two-module macros are also available. Two-module hard macros always utilize a module-pair, either SS, CC, CS, or SC. Because one- and two-module macros have small propagation delay variances, their performances can be predicted very accurately. Hard macro propagation delays are specified in the datasheet. Soft macros are comprised of multiple hard macros connected together to form complex functions. These functions range from MSI functions to 16-bit counters and accumulators. A large number of TTL equivalent hard and soft macros are also provided. Soft macro delays are not specified in the datasheet.

Routing Structure

The ACT 2 architecture uses Vertical and Horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into pieces called segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 7. Nondedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

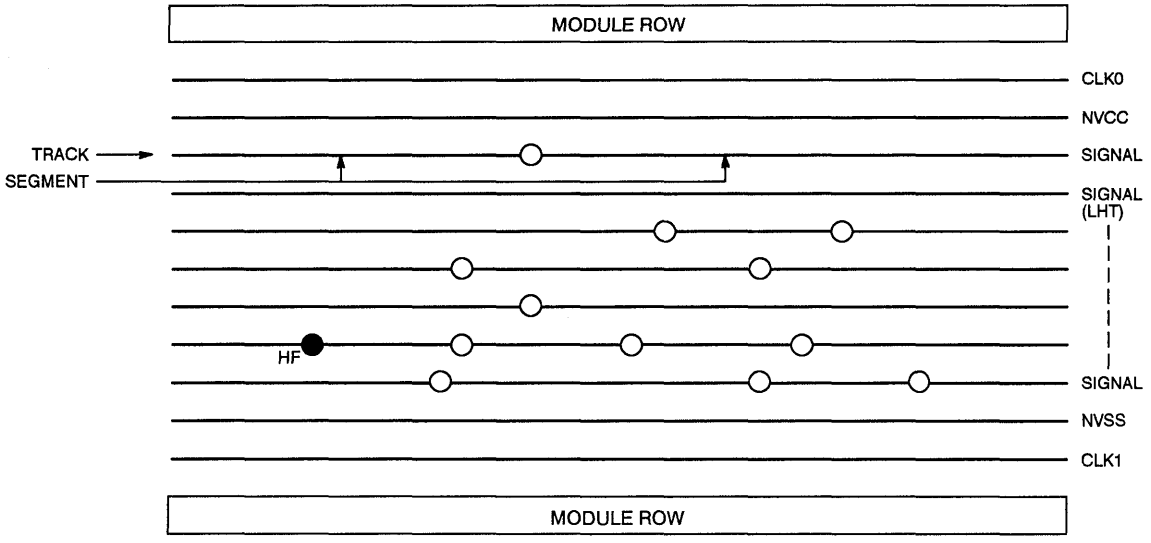


Figure 7. Horizontal Routing Tracks and Segments

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 8.

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PAL®s. The use of antifuses to implement a Programmable Logic Device results in highly testable structures as well as efficient programming algorithms. The structure is highly testable because there are no pre-existing connections, therefore temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Antifuse Structures

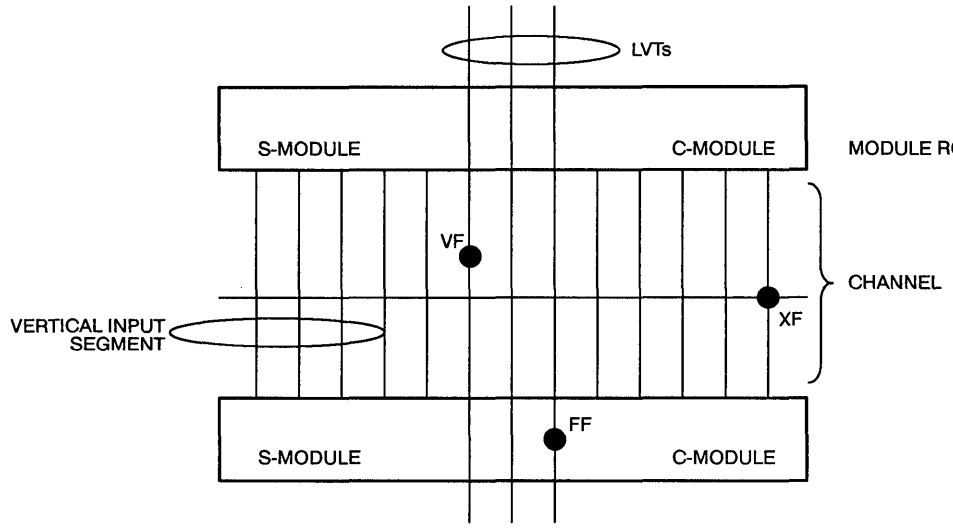


Figure 8. Vertical Routing Tracks and Segments

Antifuse Connections

Four types of antifuse connections are used in the routing structure of the Act 2 array. (The physical structure of the antifuse is identical in each case, only the usage differs.) The four types are:

XF	Cross connected antifuse	Most intersections of horizontal and vertical tracks have an XF that connects the perpendicular tracks.
HF	Horizontally connected antifuse	Adjacent segments in the same horizontal track are connected end-to-end by an HF.
VF	Vertically connected antifuse	Some long vertical tracks are divided into two segments. Adjacent long segments are connected end-to-end by a VF.
FF	"Fast-Fuse" antifuse	The FF connects a module output directly to a long vertical track.

Examples of all four antifuse connections are shown in Figures 7 and 8.

Antifuse Programming

The ACT 2 family uses the PLICE™ antifuse developed by Actel. The PLICE element is programmed by placing a high voltage (~20 V) across the element and supplying current (~5 mA) for a short duration (< 1ms). In the ACT 2 architecture, most antifuses are programmed to ~500 ohms resistance, except for the F-fuses which are programmed to ~250 ohms. The programming circuits are transparent to the user.

Clock Networks

Two low-skew, high fan-out clock distribution networks are provided in the ACT 2 architecture (Figure 9). These networks are referred to as CLK0 and CLK1. Each network has a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows:

1. externally from the CLKA pad
2. externally from the CLKB pad
3. internally from the CLKINA input
4. internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

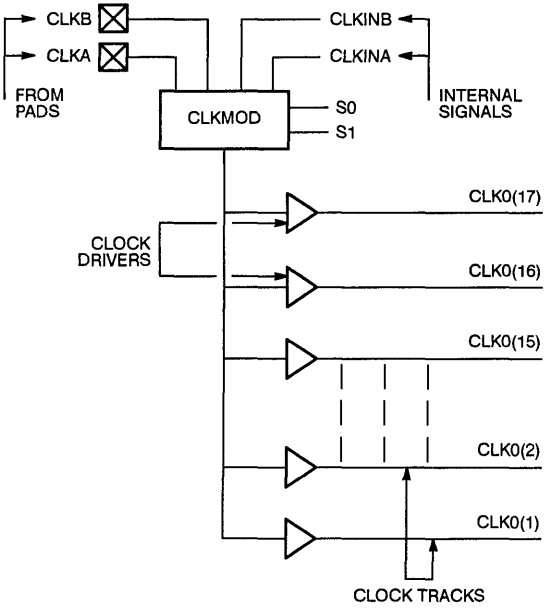


Figure 9. Clock Networks

The user configures the clock module by selecting one of two clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used.

The clock input pads may also be used as normal I/Os, by-passing the clock networks.

Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

Vertical tracks span the vertical height of the array. The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive (off), which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active (on) to verify the continuity of the metal tracks. Vertical input segments span only one channel. Inputs to the array modules come either from the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below (Figure 10).

Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 10, so that only four vertical tracks are required.

LVT Connections

Outputs may also connect to non-dedicated segments (LVTs). Each module pair in the array shares three LVTs that span the length of column as shown in Figure 9. Any module in the column pair can connect to one of the LVTs in the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, by-passing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

Antifuse Connections

In general every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

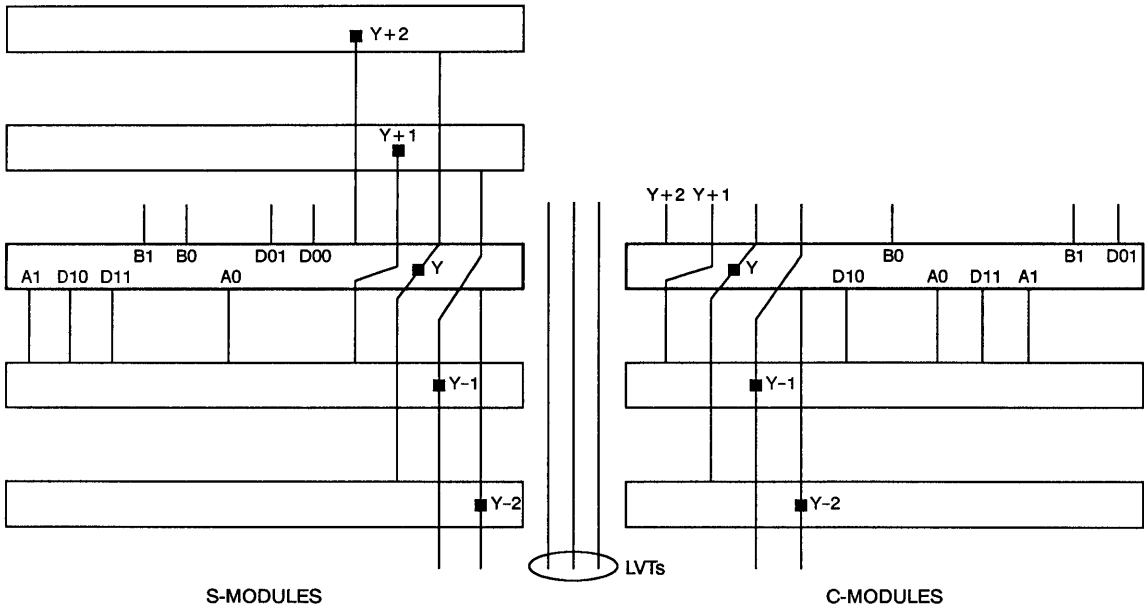


Figure 10. Logic Module Routing Interface

Clock Connections

To minimize loading on the clock networks, only a subset of inputs has fuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-Module. Both of these are illustrated in Figure 11.

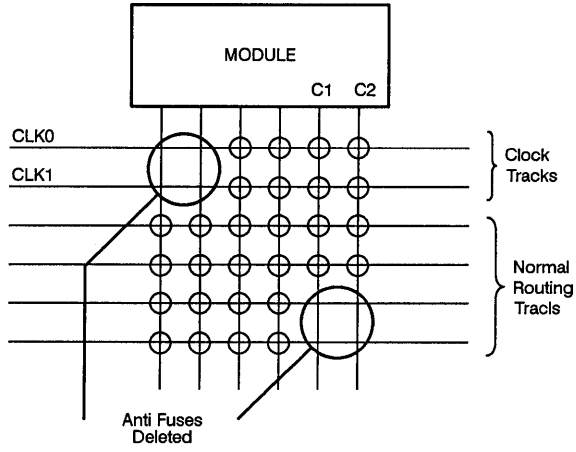


Figure 11. Fuse Deletion on Clock Networks

Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the external pins: MODE, SDI, DCLK. The function of these pins is summarized below. When MODE is low (GND), the device is in normal or user mode. When MODE is high (VCC), the device is placed into one of several programming or test states. The SDI pin (when MODE is high) is used to input serial data to the Mode register and various address registers surrounding the array. Data is clocked into these registers using the DCLK pin. The registers are connected as a long series of shift registers as shown in Figure 12. The Mode register determines the test or programming state of the device. Many of the test modes are used during wafer sort and final test at the factory. Other test modes are used during programming in the Activator® 2, and some of the modes are available only after programming. The Actionprobe® function is one such function available to users.

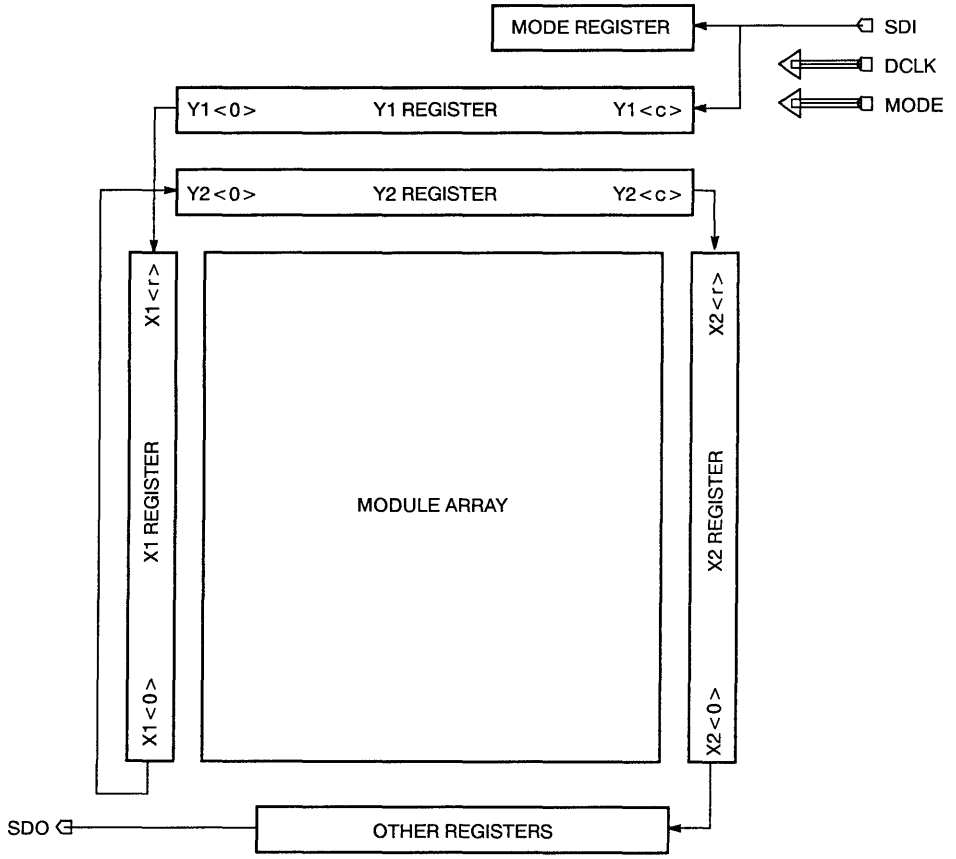


Figure 12. ACT 2 Shift Register

Actionprobe

If a device has been successfully programmed and the security fuse has not been programmed, any internal logic or I/O module output can be observed using the Actionprobe circuitry and the PRA and/or PRB pins. The Actionprobe Diagnostic system provides the software and hardware required to perform real-time debugging. The software automatically performs the following functions.

A pattern of "1s" and "0s" is shifted into the device from the SDI pin at each positive edge transition of DCLK. The complete sequence contains 10 bits of counter, 21 bits of Mode Register, n bits of zeros (filler of unused fields, where n depends on the particular device type), R bits of X2, C bits of Y2, R bits of X1, C bits of Y1, and a stop bit ("0" or "1"). After the stop bit has been shifted in, DCLK is left high (see definitions below). X1 and Y1 represent the (X,Y) location in the array for the Actionprobe output, PRA.

X2 and Y2 represent the (X,Y) location in the array for the Actionprobe output, PRB. R and C are the row and column size as defined in Table 1. The filler bits, counter pattern, and Mode register pattern are shown in Table 3. Addressing for rows and columns is active high, i.e. unselected rows and columns are "zeros" and the selected row and column is "high." The timing sequence is shown in Figure 13. The recommended frequency is 10 MHz with 10 nS setup and hold times allowing for SDI and DCLK transitions. The selected module output will be present at the PRA or PRB output approximately 20 nS after the stop-bit transition.

Table 3. Bit Stream Definitions for Actionprobe Diagnostics

Device	Probe_Mode	Filler (n)	Counter_Pattern	Mode_Register_Pattern	# of clocks
A1280	Probe A only	443	0011011111	00000011000111111000000	675
A1280	Probe B only	443	0011011111	00000010100111111000000	675
A1280	Probe A and B	443	0011011111	00000011100111111000000	675
A1240	Probe A only	361	1111000001	00000011000111111000000	541
A1240	Probe B only	361	1111000001	00000010100111111000000	541
A1240	Probe A and B	361	1111000001	00000011100111111000000	541
A1225	Probe A only	308	1101011010	00000011000111111000000	458
A1225	Probe B only	308	1101011010	00000010100111111000000	458
A1225	Probe A and B	308	1101011010	00000011100111111000000	458

For Example: Selecting PRA for A1280 results in the following bit stream:

0011011111_00000011000111111000000_
(443 zeros)_X2<0>...X2<17>_Y2<81>...Y2<0>_X1<0>...X1<0>...X1<17>_Y1<0>...Y1<81>_0,

where "_" is used for clarity only.

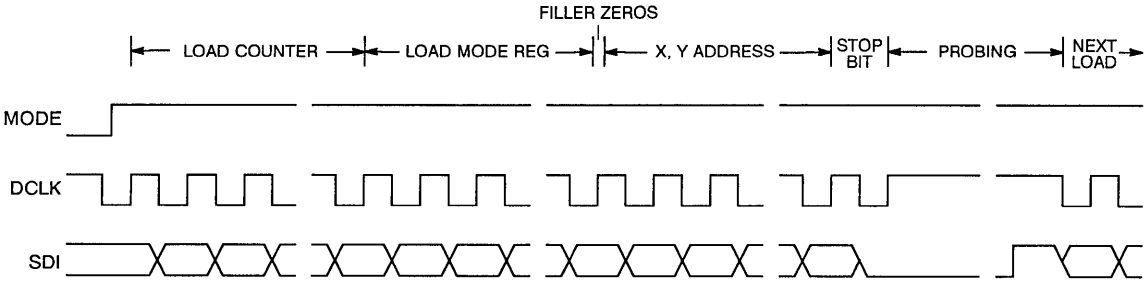
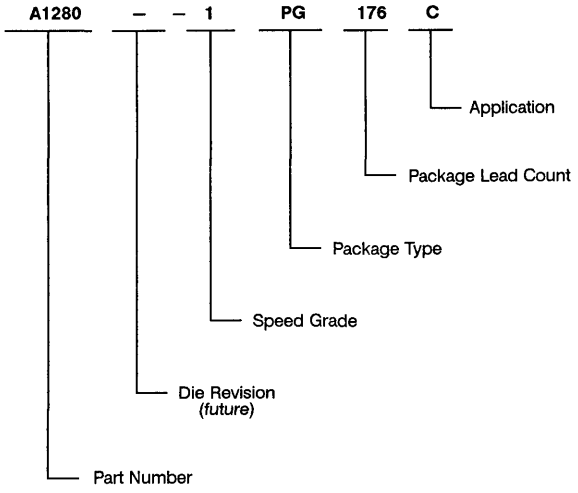


Figure 13. Timing Waveforms

Ordering Information



Product Plan

	Speed Grade		Application				
	Std	–1*	C	I	M	B	E
A1280 Device							
176-pin Ceramic Pin Grid Array (PG)	✓	✓	✓	–	✓	✓	–
160-pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	–	–	–
172-pin Ceramic Quad Flatpack (CQ)	✓	P	✓	–	✓	✓	✓
A1240 Device							
132-pin Ceramic Pin Grid Array (PG)	✓	✓	✓	–	✓	✓	–
144-pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	–	–	–
84-pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	–	–	–
A1225 Device							
100-pin Ceramic Pin Grid Array (PG)	✓	✓	✓	–	–	–	–
100-pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	–	–	–
84-pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	–	–	–

Applications: C = Commercial
I = Industrial
M = Military
B = 883B
E = Extended Flow

Availability: ✓ = Available
P = Planned
– = Not Planned

* Speed Grade: –1 = 15% faster than Standard

Device Resources

Device Series	Logic Modules	Gates	User I/Os							
			CPGA			PQFP			PLCC	CQFP
			176-pin	132-pin	100-pin	160-pin	144-pin	100-pin	84-pin	172-pin
A1280	1232	8000	140	–	–	125	–	–	–	140
A1240	684	4000	–	104	–	–	104	–	72	–
A1225	451	2500	–	–	83	–	–	–	72	–

Pin Description

CLKA Clock A (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground (Input)

Input LOW supply voltage.

I/O Input/Output (Input, Output)

I/O pins function as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

MODE Mode (Input)

The MODE pin controls the use of multi-function pins (DCLK, PRA, PRB, SDI, SDO). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os.

NC No Connection

This pin is not connected to circuitry within the device.

PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDO Serial Data Output (Output)

Serial data output for diagnostic probe. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} Supply Voltage (Input)

Input HIGH supply voltage.

V_{KS} Programming Voltage (Input)

Input supply voltage used for device programming. This pin must be connected to GND during normal operation.

V_{PP} Programming Voltage (Input)

Input supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

V_{SV} Programming Voltage (Input)

Input supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

Absolute Maximum Ratings

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[1,2,3]	-0.5 to +7.0	Volts
V_I	Input Voltage	-0.5 to V_{CC} +0.5	Volts
V_O	Output Voltage	-0.5 to V_{CC} +0.5	Volts
I_{IK}	Input Clamp Current	±20	mA
I_{OK}	Output Clamp Current	±20	mA
I_{OK}	Continuous Output Current	±25	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Stresses beyond those listed above may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.

Notes:

1. $V_{PP} = V_{CC}$, except during device programming.
2. $V_{SV} = V_{CC}$, except during device programming.
3. V_{KS} = GND, except during device programming.

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to +70	-40 to +85	-55 to +125	°C
Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. Ambient temperature (T_A) used for commercial and industrial. Case temperature (T_C) used for military.

Electrical Specifications

Parameter		Commercial		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = -10 mA)[2]	2.4						V
	(I_{OH} = -6 mA)	3.84						V
	(I_{OH} = -4 mA)			3.7		3.7		V
V_{OL}[1]	(I_{OL} = 10 mA)[2]		0.5					V
	(I_{OL} = 6 mA)		0.33		0.40		0.40	V
V_{IL}		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500		500	ns
C_{IO} I/O Capacitance[2, 3]			10		10		10	pF
Standby Current, I_{CC}[4]			10		20		25	mA
Leakage Current[5]		-10	10	-10	10	-10	10	µA

Notes:

1. Only one output tested at a time. V_{CC} = min.
2. Not tested, for information only.
3. Includes worst-case 176 CPGA package capacitance. V_{OUT} = 0 V, f = 1 MHz.
4. All outputs unloaded. All inputs = V_{CC} or GND, typical I_{CC} = 1 mA.
5. V_O, V_{IN} = V_{CC} or GND.

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the maximum power dissipation for a CPGA 176-pin package at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. military temp. (°C)}}{\theta ja\ (°C/W)} = \frac{150°C - 70°C}{20°C/W} = 4.0\ W$$

Package Type	Pin Count	θjc	θja Still air	θja 300 ft/min.	Units
CPGA	100	5	35	17	°C/W
	132	5	30	15	°C/W
	176	2	20	8	°C/W
PQFP[1]	100	13	55	47	°C/W
	144	15	35	26	°C/W
	160	15	33	24	°C/W
PLCC	84	12	44	33	°C/W

Note:
1. Maximum Power Dissipation for PQFP Package = 2.0 Watts

Power Dissipation

$P = [I_{CC} + I_{active}] \cdot V_{CC} + I_{OL} \cdot V_{OL} \cdot N + I_{OH} \cdot (V_{CC} - V_{OH}) \cdot M$

Where:

I_{CC} is the current flowing when no inputs or outputs are changing.

I_{active} is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power

Static power dissipation is typically a small component of the overall power. From the values provided in the Electrical Specifications, the maximum static power (commercial) dissipation is:

10 mA x 5.25 V = 52.5 mW

The static power dissipated by TTL loads depends on the number of outputs that drive high or low and the DC lead current flowing. Again, this number is typically small. For instance, a 32-bit bus driving TTL loads will generate 42 mW ATT with all outputs driving low or 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power

The active power component in CMOS devices is frequency dependent and depends on the user's logic and the external I/O. Active power dissipation results from charging internal chip capacitance such as that associated with the interconnect, unprogrammed antifuses, module inputs, and module outputs plus external capacitance due to PC board traces and load device inputs. An additional component of active power dissipation is due to totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1.

$$\text{Power } (\mu W) = C_{EQ} \cdot V_{CC}^2 \cdot f \qquad (1)$$

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CC} is power supply in volts.

f is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{active} at a specified frequency and voltage for each circuit component of interest. The results for ACT 2 devices are:

	C_{EQ} (pF)
Modules	7.7
Input Buffers	18.0
Output Buffers	25.0
Clock Buffer Loads	2.5

To calculate the active power that is dissipated from the complete design, you must solve Equation 1 for each component. In order to do this, you must know the switching frequency of each part of the logic. The exact equation is a piece-wise linear summation over all components, as shown in Equation 2.

$$\text{Power} = [(m \cdot 7.7 \cdot f_1) + (n \cdot 18.0 \cdot f_2) + (p \cdot (25.0 + C_L) \cdot f_3) + (q \cdot 2.5 \cdot f)] \cdot V_{CC}^2 \qquad (2)$$

Where:

n = Number of logic modules switching at frequency f_1

m = Number of input buffers switching at frequency f_2

p = Number of output buffers switching at frequency f_3

q = Number of clock loads on the global clock network

f = Frequency of global clock

f_1 = Average logic module switching rate in MHz

f_2 = Average input buffer switching rate in MHz

f_3 = Average output buffer switching rate in MHz

C_L = Output load capacitance

Determining Average Switching Frequency

In order to determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following rules will help you to determine average switching frequency in logic circuits. These rules are meant to represent worst-case scenarios so that they can be generally used for predicting the upper limits of power dissipation. These rules are as follows:

Module Utilization = 80% of combinatorial modules

Average Module Frequency = F/10

Inputs = 1/3 of I/O

Average Input Frequency = F/5

Outputs = 2/3 of I/Os

Average Output Frequency = F/10

Clock Net 1 Loading = 40% of sequential modules

Clock Net 1 Frequency = F

Clock Net 2 Loading = 40% of sequential modules

Clock Net 2 Frequency = F/2

Estimated Power

The results of estimating active power are displayed in Figure 14. The graphs provide a simple guideline for estimating power. The tables may be interpolated when your application has different resource utilizations or frequencies.

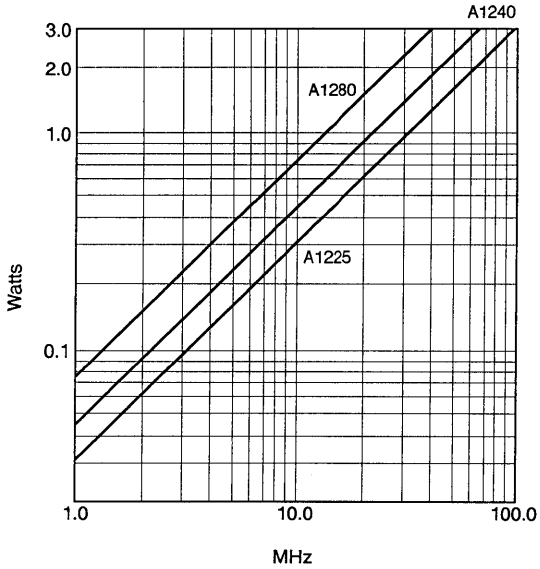
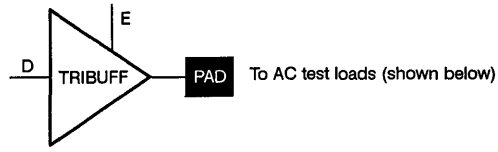
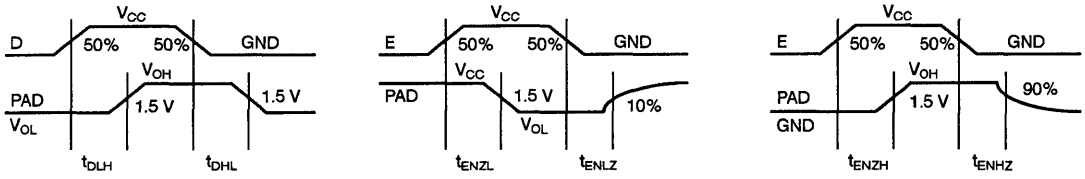


Figure 14. ACT 2 Power Estimates

Parameter Measurement

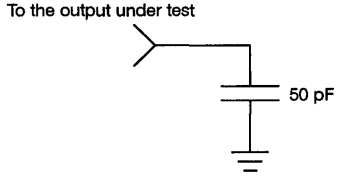
Output Buffer Delays



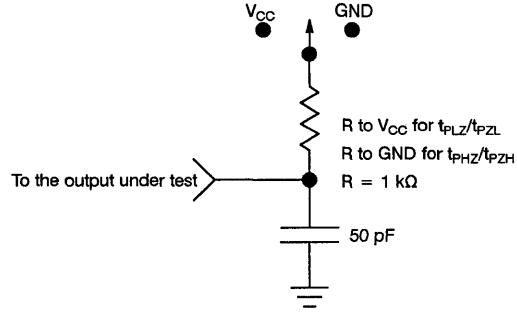


AC Test Loads

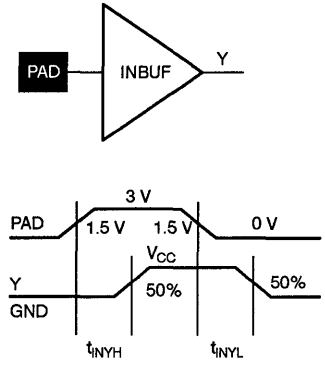
Load 1
(Used to measure propagation delay)



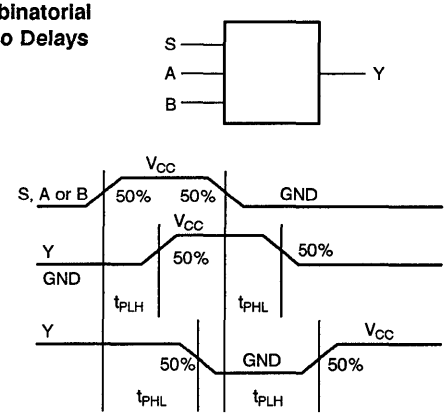
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

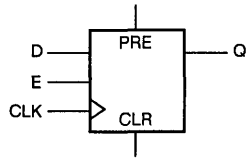


Combinatorial Macro Delays

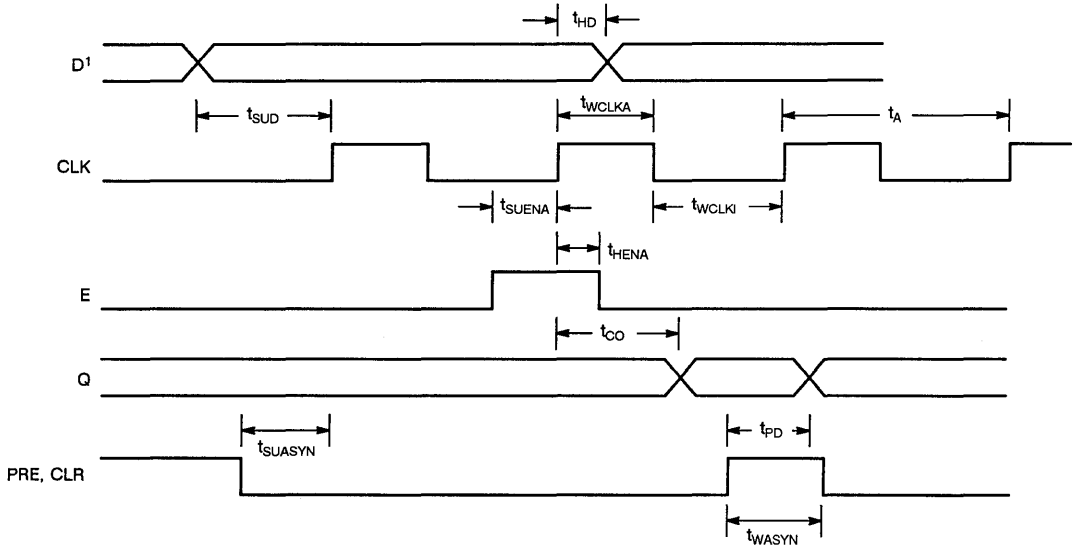


Sequential Timing Characteristics

Flip-Flops and Latches



(Positive edge triggered)

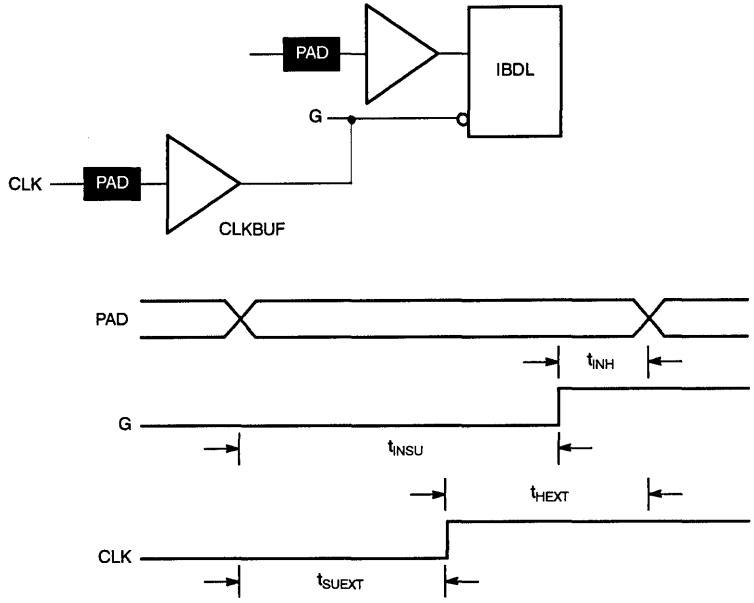


Notes:

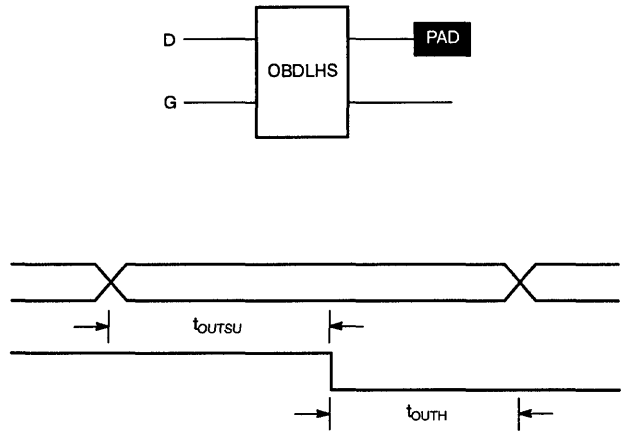
1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

Sequential Timing Characteristics (continued)

Input Buffer Latches



Output Buffer Latches



Timing Characteristics

Timing characteristics for ACT arrays fall into three categories: family dependent, device dependent, and design dependent. The output buffer characteristics are common to all ACT 2 family members. Internal module delays are device dependent. Internal wiring delays between modules are design dependent. Design dependency means actual delays are not determined until after placement and routing of the users design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

The macro propagation delays shown in the Timing Characteristics tables include the module delay plus estimates derived from statistical analysis for wiring delay. This statistical estimate is based on fully utilized devices (90% module utilization).

Critical Nets and Typical Nets

Propagation delays are expressed for two types of nets: critical and typical. Critical nets are determined by net property assignment before placement and routing. Up to 6% of the nets in a design may be designated as *critical*, while 90% of the nets in a design are *typical*.

Fan-Out Dependency

Propagation delays depend on the fan-out (number of loads) driven by a macro. Delay time increases when fan-out increases due to the capacitive loading of the macro's inputs, as well as the interconnect's resistance and capacitance.

Long Tracks

Some nets in the design use *long tracks*. Long tracks are special routing resources that span multiple rows or columns or modules, and are used frequently in large fan-out (> 10) situations. Long tracks employ three and sometimes four antifuse connections. This increased capacitance and resistance results in longer net delays for macros connected to long tracks. Typically up to 6% of the nets in a fully utilized device require long tracks. Long tracks contribute an additional 10 ns to 15 ns delay.

Timing Derating

Operating temperature, operating voltage, and device processing conditions, along with device die size and speed grade, account for variations in array timing characteristics. These variations are summarized into a derating factor for ACT 2 array typical timing specifications. The derating factors shown in the table below are based on the recommended operating conditions for ACT 2 applications. The derating curves in Figure 15 show worst-to-best case operating voltage range and best-to-worst case operating temperature range. The temperature derating curve is based on device junction temperature. Actual junction temperature is determined from Ambient Temperature, Power Dissipation, and Package Thermal characteristics.

1

Timing Derating Factor (x typical)

Commercial		Industrial		Military	
Best-Case	**Worst-Case**	**Best-Case**	**Worst-Case**	**Best-Case**	**Worst-Case**
0.40	1.40	0.37	1.50	0.35	1.6

Note:
"Best-case" reflects maximum operating voltage, minimum operating temperature, and best-case processing. "Worst-case" reflects minimum operating voltage, maximum operating temperature, and worst-case processing. Best-case derating is based on sample data only and is not guaranteed.

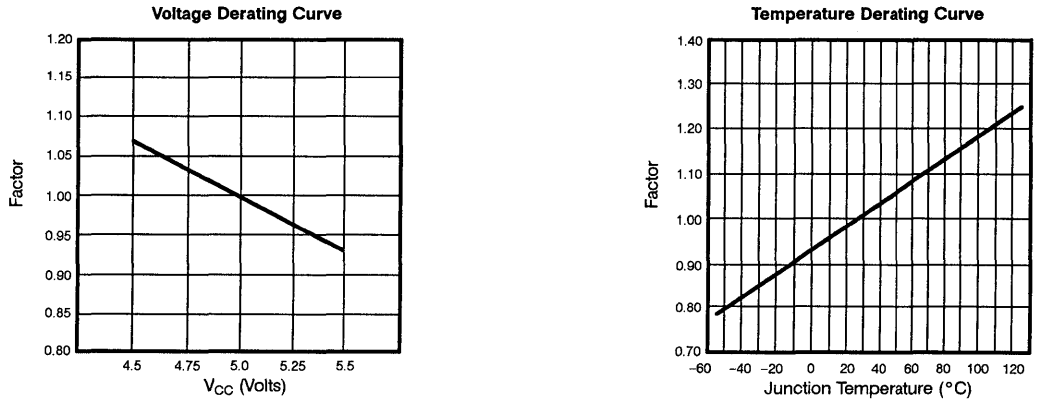


Figure 15. Operating Curves

A1280 Timing Characteristics

Propagation Delays (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD1}	Single Module	Critical	4.5	5.0	5.5	6.0	–	ns
t_{PD1}	Single Module	Typical	5.7	6.2	6.7	8.2	11.7	ns
t_{PD2}	Dual Module	Critical	7.5	8.0	8.5	9.0	–	ns
t_{PD2}	Dual Module	Typical	8.7	9.2	9.7	11.2	14.7	ns
t_{CO}	Sequential Clk to Q	Critical	4.5	5.0	5.5	6.0	–	ns
t_{CO}	Sequential Clk to Q	Typical	5.7	6.2	6.7	8.2	11.7	ns
t_{GO}	Latch G to Q	Critical	4.5	5.0	5.5	6.0	–	ns
t_{GO}	Latch G to Q	Typical	5.7	6.2	6.7	8.2	11.7	ns
t_{PD}	Asynchronous to Q	Critical	4.5	5.0	5.5	6.0	–	ns
t_{PD}	Asynchronous to Q	Typical	5.7	6.2	6.7	8.2	11.7	ns

Sequential Timing Characteristics (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

		Commercial		Industrial		Military		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.5		1.0		ns
t_{SUASYN}	Flip-Flop (Latch) Asynchronous Input Setup	1.0		1.5		2.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.0		1.5		2.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0	ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.0		4.5		5.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.0		4.5		5.0		ns
t_A	Flip-Flop Clock Input Period	18.0		20.0		22.0		ns
t_{INH}	Input Buffer Latch Hold		2.0		2.5		2.5	ns
t_{INSU}	Input Buffer Latch Setup	-2.5		-3.0		-3.5		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0	ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.5		1.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		48.0		43.0		39.0	MHz

Notes:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1280 Timing Characteristics (continued)

I/O Buffer Timing (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{INYH}	Pad to Y High	6.7	7.2	7.7	8.2	11.7	ns
t_{INYL}	Pad to Y Low	6.6	7.1	7.6	8.1	11.5	ns
t_{INGH}	G to Y High	6.6	7.2	7.7	8.2	11.7	ns
t_{INGL}	G to Y Low	6.4	6.9	7.5	8.0	11.4	ns

Global Clock Network (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 32	FO = 128	FO =384	Units
t_{CKH}	Input Low to High	9.1	10.1	12.3	ns
t_{CKL}	Input High to Low	9.1	10.2	12.5	ns
t_{PWH}	Minimum Pulse Width High	4.0	4.5	5.0	ns
t_{PWL}	Minimum Pulse Width Low	4.0	4.5	5.0	ns
t_{CKSW}	Maximum Skew	0.5	1.0	2.5	ns
t_{SUEXT}	Input Latch External Setup[1]	0.0	0.0	0.0	ns
t_{HEXT}	Input Latch External Hold[1]	7.0	8.0	11.2	ns
t_P	Minimum Period	13.3	14.3	15.3	ns
f_{MAX}	Maximum Frequency	75.0	70.0	65.0	MHz

Note:
1. Derating does not apply to this parameter.

Output Buffer Timing (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	TTL	CMOS	Units
t_{DLH}	Data to Pad High	4.6	6.7	ns
t_{DHL}	Data to Pad Low	6.5	4.9	ns
t_{ENZH}	Enable Pad Z to High	8.3	8.3	ns
t_{ENZL}	Enable Pad Z to Low	5.5	5.5	ns
t_{ENHZ}	Enable Pad High to Z	4.5	4.5	ns
t_{ENLZ}	Enable Pad Low to Z	6.0	6.0	ns
t_{GLH}	G to Pad High	4.6	4.6	ns
t_{GHL}	G to Pad Low	6.5	6.5	ns
d_{TLH}	Delta Low to High	0.06	0.11	ns/pF
d_{THL}	Delta High to Low	0.11	0.08	ns/pF

A1280-1 Timing Characteristics

Propagation Delays (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD1}	Single Module	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{PD1}	Single Module	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{PD2}	Dual Module	Critical Net	7.5	8.0	8.5	9.0	–	ns
t_{PD2}	Dual Module	Typical Net	7.9	8.3	8.7	10.0	13.0	ns
t_{CO}	Sequential Clk to Q	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{CO}	Sequential Clk to Q	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{GO}	Latch G to Q	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{GO}	Latch G to Q	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{PD}	Asynchronous to Q	Critical	3.9	4.3	4.8	5.3	–	ns
t_{PD}	Asynchronous to Q	Typical	4.9	5.3	5.7	7.0	10.0	ns

Sequential Timing Characteristics (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

		Commercial		Industrial		Military		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.5		1.0		ns
t_{SUASYN}	Flip-Flop (Latch) Asynchronous Input Setup	1.0		1.5		2.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.0		1.5		2.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0	ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.0		4.5		5.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.0		4.5		5.0		ns
t_A	Flip-Flop Clock Input Period	15.0		18.0		20.0		ns
t_{INH}	Input Buffer Latch Hold		2.0		2.5		2.5	ns
t_{INSU}	Input Buffer Latch Setup	-2.5		-3.0		-3.5		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0	ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.5		1.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		65.0		60.0		50.0	MHz

Notes:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1280-1 Timing Characteristics (continued)

I/O Buffer Timing (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{INYH}	Pad to Y High	6.1	6.5	5.9	7.4	10.5	ns
t_{INYL}	Pad to Y Low	5.9	6.4	6.8	7.3	10.4	ns
t_{INGH}	G to Y High	6.1	6.5	5.9	7.4	10.5	ns
t_{INGL}	G to Y Low	5.9	6.4	6.8	7.3	10.4	ns

Global Clock Network (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 32	FO = 128	FO = 384	Units
t_{CKH}	Input Low to High	7.8	8.7	10.4	ns
t_{CKL}	Input High to Low	7.8	8.8	10.6	ns
t_{PWH}	Minimum Pulse Width High	4.0	4.5	5.0	ns
t_{PWL}	Minimum Pulse Width Low	4.0	4.5	5.0	ns
t_{CKSW}	Maximum Skew	0.5	1.0	2.5	ns
t_{SUEXT}	Input Latch External Setup[1]	0.0	0.0	0.0	ns
t_{HEXT}	Input Latch External Hold[1]	7.0	8.0	11.2	ns
t_P	Minimum Period	11.4	12.0	13.0	ns
f_{MAX}	Maximum Frequency	89.0	83.0	77.0	MHz

Note:
1. Derating does not apply to this parameter.

Output Buffer Timing (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	TTL	CMOS	Units
t_{DLH}	Data to Pad High	4.6	6.7	ns
t_{DHL}	Data to Pad Low	6.5	4.9	ns
t_{ENZH}	Enable Pad Z to High	8.3	8.3	ns
t_{ENZL}	Enable Pad Z to Low	5.5	5.5	ns
t_{ENHZ}	Enable Pad High to Z	4.5	4.5	ns
t_{ENLZ}	Enable Pad Low to Z	6.0	6.0	ns
t_{GLH}	G to Pad High	4.6	4.6	ns
t_{GHL}	G to Pad Low	6.5	6.5	ns
d_{TLH}	Delta Low to High	0.06	0.11	ns/pF
d_{THL}	Delta High to Low	0.11	0.08	ns/pF

A1240 Timing Characteristics

PRELIMINARY DATA

Propagation Delays (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD1}	Single Module	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{PD1}	Single Module	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{PD2}	Dual Module	Critical Net	7.5	8.0	8.5	9.0	–	ns
t_{PD2}	Dual Module	Typical Net	7.9	8.3	8.7	10.0	13.0	ns
t_{CO}	Sequential Clk to Q	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{CO}	Sequential Clk to Q	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{GO}	Latch G to Q	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{GO}	Latch G to Q	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{PD}	Asynchronous to Q	Critical	3.9	4.3	4.8	5.3	–	ns
t_{PD}	Asynchronous to Q	Typical	4.9	5.3	5.7	7.0	10.0	ns

Sequential Timing Characteristics (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

		Commercial		Industrial		Military		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.5		1.0		ns
t_{SUASYN}	Flip-Flop (Latch) Asynchronous Input Setup	1.0		1.5		2.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.0		1.5		2.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0	ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.0		4.5		5.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.0		4.5		5.0		ns
t_A	Flip-Flop Clock Input Period	15.0		18.0		20.0		ns
t_{INH}	Input Buffer Latch Hold		2.0		2.5		2.5	ns
t_{INSU}	Input Buffer Latch Setup	-2.5		-3.0		-3.5		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0	ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.5		1.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		66.0		55.0		50.0	MHz

Notes:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1240 Timing Characteristics (continued)

PRELIMINARY DATA

I/O Buffer Timing (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{INYH}	Pad to Y High	6.1	6.5	5.9	7.4	10.5	ns
t_{INYL}	Pad to Y Low	5.9	6.4	6.8	7.3	10.4	ns
t_{INGH}	G to Y High	6.1	6.5	5.9	7.4	10.5	ns
t_{INGL}	G to Y Low	5.9	6.4	6.8	7.3	10.4	ns

Global Clock Network (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 32	FO = 128	FO =256	Units
t_{CKH}	Input Low to High	9.1	10.1	11.2	ns
t_{CKL}	Input High to Low	9.1	10.2	11.3	ns
t_{PWH}	Minimum Pulse Width High	4.0	4.5	5.0	ns
t_{PWL}	Minimum Pulse Width Low	4.0	4.5	5.0	ns
t_{CKSW}	Maximum Skew	0.5	1.0	2.5	ns
t_{SUEXT}	Input Latch External Setup[1]	0.0	0.0	0.0	ns
t_{HEXT}	Input Latch External Hold[1]	7.0	8.0	11.2	ns
t_P	Minimum Period	11.1	11.5	11.8	ns
f_{MAX}	Maximum Frequency	90.0	87.0	85.0	MHz

Note:
1. Derating does not apply to this parameter.

Output Buffer Timing (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	TTL	CMOS	Units
t_{DLH}	Data to Pad High	4.6	6.7	ns
t_{DHL}	Data to Pad Low	6.5	4.9	ns
t_{ENZH}	Enable Pad Z to High	8.3	8.3	ns
t_{ENZL}	Enable Pad Z to Low	5.5	5.5	ns
t_{ENHZ}	Enable Pad High to Z	4.5	4.5	ns
t_{ENLZ}	Enable Pad Low to Z	6.0	6.0	ns
t_{GLH}	G to Pad High	4.6	4.6	ns
t_{GHL}	G to Pad Low	6.5	6.5	ns
d_{TLH}	Delta Low to High	0.06	0.11	ns/pF
d_{THL}	Delta High to Low	0.11	0.08	ns/pF

A1240-1 Timing Characteristics

PRELIMINARY DATA

Propagation Delays (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD1}	Single Module	Critical Net	3.5	3.9	4.3	4.8	–	ns
t_{PD1}	Single Module	Typical Net	4.4	4.8	5.1	6.3	9.0	ns
t_{PD2}	Dual Module	Critical Net	7.5	8.0	8.5	9.0	–	ns
t_{PD2}	Dual Module	Typical Net	7.4	7.8	8.1	9.3	12.0	ns
t_{CO}	Sequential Clk to Q	Critical Net	3.5	3.9	4.3	4.8	–	ns
t_{CO}	Sequential Clk to Q	Typical Net	4.4	4.8	5.1	6.3	9.0	ns
t_{GO}	Latch G to Q	Critical Net	3.5	3.9	4.3	4.8	–	ns
t_{GO}	Latch G to Q	Typical Net	4.4	4.8	5.1	6.3	9.0	ns
t_{PD}	Asynchronous to Q	Critical	3.5	3.9	4.3	4.8	–	ns
t_{PD}	Asynchronous to Q	Typical	4.4	4.8	5.1	6.3	9.0	ns

Sequential Timing Characteristics (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

		Commercial		Industrial		Military		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.5		1.0		ns
t_{SUASYN}	Flip-Flop (Latch) Asynchronous Input Setup	1.0		1.5		2.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.0		1.5		2.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0	ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.0		4.5		5.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.0		4.5		5.0		ns
t_A	Flip-Flop Clock Input Period	13.0		15.0		18.0		ns
t_{INH}	Input Buffer Latch Hold		2.0		2.5		2.5	ns
t_{INSU}	Input Buffer Latch Setup	-2.5		-3.0		-3.5		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0	ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.5		1.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		75.0		66.0		55.0	MHz

Notes:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1240-1 Timing Characteristics (continued)

PRELIMINARY DATA

I/O Buffer Timing (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{INYH}	Pad to Y High	5.5	5.9	5.3	6.7	9.5	ns
t_{INYL}	Pad to Y Low	5.3	5.8	6.1	6.6	9.4	ns
t_{INGH}	G to Y High	5.5	5.9	5.3	6.7	9.5	ns
t_{INGL}	G to Y Low	5.3	5.8	6.1	6.6	9.4	ns

Global Clock Network (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 32	FO = 128	FO =256	Units
t_{CKH}	Input Low to High	7.8	8.7	9.3	ns
t_{CKL}	Input High to Low	7.8	8.8	9.4	ns
t_{PWH}	Minimum Pulse Width High	4.0	4.5	5.0	ns
t_{PWL}	Minimum Pulse Width Low	4.0	4.5	5.0	ns
t_{CKSW}	Maximum Skew	0.5	1.0	2.5	ns
t_{SUEXT}	Input Latch External Setup[1]	0.0	0.0	0.0	ns
t_{HEXT}	Input Latch External Hold[1]	7.0	8.0	11.2	ns
t_P	Minimum Period	9.1	19.5	10.0	ns
f_{MAX}	Maximum Frequency	110.0	105.0	100.0	MHz

Note:
1. Derating does not apply to this parameter.

Output Buffer Timing (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	TTL	CMOS	Units
t_{DLH}	Data to Pad High	4.6	6.7	ns
t_{DHL}	Data to Pad Low	6.5	4.9	ns
t_{ENZH}	Enable Pad Z to High	8.3	8.3	ns
t_{ENZL}	Enable Pad Z to Low	5.5	5.5	ns
t_{ENHZ}	Enable Pad High to Z	4.5	4.5	ns
t_{ENLZ}	Enable Pad Low to Z	6.0	6.0	ns
t_{GLH}	G to Pad High	4.6	4.6	ns
t_{GHL}	G to Pad Low	6.5	6.5	ns
d_{TLH}	Delta Low to High	0.06	0.11	ns/pF
d_{THL}	Delta High to Low	0.11	0.08	ns/pF

A1225 Timing Characteristics

PRELIMINARY DATA

Propagation Delays (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD1}	Single Module	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{PD1}	Single Module	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{PD2}	Dual Module	Critical Net	7.5	8.0	8.5	9.0	–	ns
t_{PD2}	Dual Module	Typical Net	7.9	8.3	8.7	10.0	13.0	ns
t_{CO}	Sequential Clk to Q	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{CO}	Sequential Clk to Q	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{GO}	Latch G to Q	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{GO}	Latch G to Q	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{PD}	Asynchronous to Q	Critical	3.9	4.3	4.8	5.3	–	ns
t_{PD}	Asynchronous to Q	Typical	4.9	5.3	5.7	7.0	10.0	ns

Sequential Timing Characteristics (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

		Commercial		Industrial		
Parameter	Description	Min.	Max.	Min.	Max.	Units
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.5		ns
t_{SUASYN}	Flip-Flop (Latch) Asynchronous Input Setup	1.0		1.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.0		1.5		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0	ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.0		4.5		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.0		4.5		ns
t_A	Flip-Flop Clock Input Period	13.0		15.0		ns
t_{INH}	Input Buffer Latch Hold		2.0		2.5	ns
t_{INSU}	Input Buffer Latch Setup	-2.5		-3.0		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0	ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		75.0		66.0	MHz

Notes:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1225 Timing Characteristics (continued)

PRELIMINARY DATA

I/O Buffer Timing (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{INYH}	Pad to Y High	6.1	6.5	5.9	7.4	10.5	ns
t_{INYL}	Pad to Y Low	5.9	6.4	6.8	7.3	10.4	ns
t_{INGH}	G to Y High	6.1	6.5	5.9	7.4	10.5	ns
t_{INGL}	G to Y Low	5.9	6.4	6.8	7.3	10.4	ns

Global Clock Network (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 32	FO = 128	FO =256	Units
t_{CKH}	Input Low to High	7.8	8.7	9.3	ns
t_{CKL}	Input High to Low	7.8	8.8	9.4	ns
t_{PWH}	Minimum Pulse Width High	4.5	5.1	5.5	ns
t_{PWL}	Minimum Pulse Width Low	4.5	5.1	5.5	ns
t_{CKSW}	Maximum Skew	0.5	1.0	2.5	ns
t_{SUEXT}	Input Latch External Setup[1]	0.0	0.0	0.0	ns
t_{HEXT}	Input Latch External Hold[1]	7.0	8.0	11.2	ns
t_P	Minimum Period	9.1	9.5	10.0	ns
f_{MAX}	Maximum Frequency	110.0	105.0	100.0	MHz

Note:
1. Derating does not apply to this parameter.

Output Buffer Timing (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	TTL	CMOS	Units
t_{DLH}	Data to Pad High	4.6	6.7	ns
t_{DHL}	Data to Pad Low	6.5	4.9	ns
t_{ENZH}	Enable Pad Z to High	8.3	8.3	ns
t_{ENZL}	Enable Pad Z to Low	5.5	5.5	ns
t_{ENHZ}	Enable Pad High to Z	4.5	4.5	ns
t_{ENLZ}	Enable Pad Low to Z	6.0	6.0	ns
t_{GLH}	G to Pad High	4.6	4.6	ns
t_{GHL}	G to Pad Low	6.5	6.5	ns
d_{TLH}	Delta Low to High	0.06	0.11	ns/pF
d_{THL}	Delta High to Low	0.11	0.08	ns/pF

A1225-1 Timing Characteristics

PRELIMINARY DATA

Propagation Delays (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD1}	Single Module	Critical Net	3.5	3.9	4.3	4.8	–	ns
t_{PD1}	Single Module	Typical Net	4.4	4.8	5.1	6.3	9.0	ns
t_{PD2}	Dual Module	Critical Net	7.5	8.0	8.5	9.0	–	ns
t_{PD2}	Dual Module	Typical Net	7.4	7.8	8.1	9.3	12.0	ns
t_{CO}	Sequential Clk to Q	Critical Net	3.5	3.9	4.3	4.8	–	ns
t_{CO}	Sequential Clk to Q	Typical Net	4.4	4.8	5.1	6.3	9.0	ns
t_{GO}	Latch G to Q	Critical Net	3.5	3.9	4.3	4.8	–	ns
t_{GO}	Latch G to Q	Typical Net	4.4	4.8	5.1	6.3	9.0	ns
t_{PD}	Asynchronous to Q	Critical	3.5	3.9	4.3	4.8	–	ns
t_{PD}	Asynchronous to Q	Typical	4.4	4.8	5.1	6.3	9.0	ns

Sequential Timing Characteristics (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

		Commercial		Industrial		
Parameter	Description	Min.	Max.	Min.	Max.	Units
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.5		ns
t_{SUASYN}	Flip-Flop (Latch) Asynchronous Input Setup	1.0		1.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.0		1.5		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0	ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.0		4.5		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.0		4.5		ns
t_A	Flip-Flop Clock Input Period	11.7		13.3		ns
t_{INH}	Input Buffer Latch Hold		2.0		2.5	ns
t_{INSU}	Input Buffer Latch Setup	-2.5		-3.0		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0	ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		85.0		75.0	MHz

Notes:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1225-1 Timing Characteristics (continued)

PRELIMINARY DATA

I/O Buffer Timing (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{INYH}	Pad to Y High	5.5	5.9	5.3	6.7	9.5	ns
t_{INYL}	Pad to Y Low	5.3	5.8	6.1	6.6	9.4	ns
t_{INGH}	G to Y High	5.5	5.9	5.3	6.7	9.5	ns
t_{INGL}	G to Y Low	5.3	5.8	6.1	6.6	9.4	ns

Global Clock Network (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 32	FO = 128	FO =256	Units
t_{CKH}	Input Low to High	7.0	7.8	8.6	ns
t_{CKL}	Input High to Low	7.0	7.8	8.6	ns
t_{PWH}	Minimum Pulse Width High	4.2	4.5	5.0	ns
t_{PWL}	Minimum Pulse Width Low	4.2	4.5	5.0	ns
t_{CKSW}	Maximum Skew	0.5	1.0	2.5	ns
t_{SUEXT}	Input Latch External Setup[1]	0.0	0.0	0.0	ns
t_{HEXT}	Input Latch External Hold[1]	7.0	8.0	11.2	ns
t_P	Minimum Period	8.3	8.7	9.1	ns
f_{MAX}	Maximum Frequency	120.0	115.0	110.0	MHz

Note:
1. Derating does not apply to this parameter.

1

Output Buffer Timing (V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; Derating Required)

Parameter	Description	TTL	CMOS	Units
t_{DLH}	Data to Pad High	4.6	6.7	ns
t_{DHL}	Data to Pad Low	6.5	4.9	ns
t_{ENZH}	Enable Pad Z to High	8.3	8.3	ns
t_{ENZL}	Enable Pad Z to Low	5.5	5.5	ns
t_{ENHZ}	Enable Pad High to Z	4.5	4.5	ns
t_{ENLZ}	Enable Pad Low to Z	6.0	6.0	ns
t_{GLH}	G to Pad High	4.6	4.6	ns
t_{GHL}	G to Pad Low	6.5	6.5	ns
d_{TLH}	Delta Low to High	0.06	0.11	ns/pF
d_{THL}	Delta High to Low	0.11	0.08	ns/pF

Macro Library

Overview

The following tables describe ACT 2 macros, which are building blocks for designing FPGAs with the ALS and your CAE interface.

The macros are divided into four categories: I/O Macros, Hard Macros (Combinable and Non-Combinable), Soft Macros, and TTL Macros.

Equation Statement Elements

Combinatorial Elements

All equations for combinatorial logic elements use the following operators:

Operator	Symbol
AND	See Note 1
NOT	!
OR	+
XOR	^

Notes:

1. A space between the 'A' and 'B' in the equation Y = A B means **A AND B.**
2. Order of operators in decreasing precedence is: NOT, AND, XOR, and OR.
3. Signals expressed in bold have a dual module delay.

Sequential Elements

All equations for sequential logic elements use the following formula:

Q = <!> (<!> CLK or G, <data equation>, <!> CLR, <!> PRE)

<!>	Optional Inversion
CLK	Flip-Flop Clock Pin
G	Latch Gate Pin
CLR	Asynchronous Clear Pin
PRE	Asynchronous Preset Pin

ACT 2 Macro Selections

I/O Macros

Macro Name	No. of Modules		Description
	I/O	Clock	
INBUF	1		Input
IBDL	1		Input with Input Latch
BBDLHS	1		Bidirectional with Input Latch and Output Latch
BBHS	1		Bidirectional
BIBUF	1		Bidirectional
CLKBIBUF	1	1	Bidirectional with Input Dedicated to Clock Network
CLKBUF	1	1	Input for Dedicated Clock Network
OBDLHS	1		Output with Output Latch
OBHS	1		Output
OUTBUF	1		Output
TBDLHS	1		Three State Output with Latch
TBHS	1		Three State Output
TRIBUFF	1		Three State Output

Note:

The following are functionally identical:
OBHS and OUTBUF; TRIBUFF and TBHS; BBHS and BIBUF.

TTL Macros

Macro Name	Description	Logic Levels	No. of Modules	
			Seq.	Comb.
TA00	2-input NAND	1		1
TA02	2-input NOR	1		1
TA04	Inverter	1		1
TA07	Buffer	1		1
TA08	2-input AND	1		1
TA10	3-input NAND	1		1
TA11	3-input AND	1		1
TA20	4-input NAND	1		2
TA21	4-input AND	1		1
TA27	3-input NOR	1		1
TA32	2-input OR	1		1
TA40	4-input NAND	1		2
TA42	4 to 10 decoder	1		10
TA51	AND-OR-Invert	1		2
TA54	4-wide AND-OR-Invert	2		5
TA55	2-wide 4-input AND-OR-Invert	2		3
TA86	2-input exclusive OR	1		1
TA138	3 to 8 decoder with enable and active low outputs	2		12
TA139	2 to 4 decoder with enable and active low outputs	1		4
TA150	16 to 1 multiplexor	3		6
TA151	8 to 1 multiplexor with enable and active low outputs	3		5
TA153	4 to 1 multiplexor	2		2
TA154	4 to 16 decoder	2		22
TA157	2 to 1 multiplexor	1		1
TA160	4-bit decode counter with clear	4	4	12
TA161	4-bit binary counter with clear	3	4	10
TA164	8-bit serial in, parallel out shift register	1	8	
TA169	4-bit up/down counter	6	4	14
TA174	Hex D-type flip-flop with clear	1	6	
TA175	Quadruple D-type flip-flop with clear	1	4	
TA190	4-bit up/down decode counter with up/down mode	7	4	31
TA191	4-bit up/down binary counter with up/down mode	7	4	30
TA194	4-bit shift register	1	4	4
TA195	4-bit shift register	1	4	1
TA269	8-bit up/down binary counter	8	8	28
TA273	Octal register with clear	1	8	
TA280	Parity generator and checker	4		9
TA377	Octel register with active low enable	1	8	
TA688	8-bit identity comparator	3		9

Soft Macros

Function	Description	Macro Name	Logic Levels	No. of Modules	
				Seq.	Comb.
Counters	4-bit binary counter with load, clear	CNT4A	4	4	8
	4-bit binary counter with load, clear, carry in, carry out	CNT4B	4	4	7
	4-bit up/down counter with load, carry in, and carry out	UDCNT4A	5	4	13
	very fast 16-bit down counter	VCNT16C	1	34	31
	2-bit down counter, prescaler	VCNT2CP	1	5	2
	2-bit down counter, most significant bit	VCNT2CU	1	2	3
	4-bit down counter, middle bits	VCNT4C	1	4	8
	4-bit down counter, low order bits	VCNT4CL	1	4	7
Decoders	2 to 4 decoder	DEC2X4	1		4
	2 to 4 decoder with active low outputs	DEC2X4A	1		4
	3 to 8 decoder	DEC3X8	1		8
	3 to 8 decoder with active low outputs	DEC3X8A	1		8
	4 to 16 decoder with active low outputs	DEC4X16A	2		20
	2 to 4 decoder with enable	DECE2X4	1		4
	2 to 4 decoder with enable and active low outputs	DECE2X4A	1		4
	3 to 8 decoder with enable	DECE3X8	2		11
	3 to 8 decoder with enable and active low outputs	DECE3X8A	2		11
Registers	octal latch with clear	DLC8A	1	8	
	octal latch with enable	DLE8	1	8	
	octal latch with multiplexed data	DLM8	1	8	
	4-bit shift register with clear	SREG4A	1	4	
	8-bit shift register with clear	SREG8A	1	8	
Adders	8-bit adder	FADD8	3		44
	9-bit adder	FADD9	3		49
	10-bit adder	FADD10	3		56
	12-bit adder	FADD12	4		69
	16-bit adder	FADD16	5		97
	2-bit sum generator	SUMX1A	2		5
	very fast 16-bit adder	VADD16C	3		97
Comparators	4-bit identity comparator	ICMP4	2		5
	8-bit identity comparator	ICMP8	3		5
	2-bit magnitude comparator with enable	MCMPC2	3		9
	4-bit magnitude comparator with enable	MCMPC4	4		18
	8-bit magnitude comparator with enable	MCMPC8	6		36
Multiplexors	8 to 1 multiplexor	MX8	2		3
	8 to 1 multiplexor with active low outputs	MX8A	2		3
	16 to 1 multiplexor	MX16	2		5

Combinable Hard Macros 1 (for DF1, DF1B, DFC1B, DFC1D, DL1, DL1B, DLC, and DLCA)

Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
AND	2-input	AND2	Y = A B		1
		AND2A	Y = !A B		1
		AND2B	Y = !A !B		1
		AND3B	Y = !A !B C		1
AND-OR		AO1A	Y = ((!A) B) + C		1
		AO1D	Y = (!A !B) + C		1
AND-OR Invert		AOI1D	Y = !((!A !B) + !C)		1
Buffers and Inverters		BUF	Y = A		1
		BUFA	Y = !(!A)		1
		INV	Y = !A		1
		INVA	Y = !A		1
Clock Net Interface		GAND2	Y = A G		1
		GNOR2	Y = !(A + G)		1
		GOR2	Y = A + G		1
Multiplexor	2:1	MX2	Y = (A !S) + (B S)		1
NAND	2-input	NAND2A	Y = !(!A B)		1
		NAND2B	Y = !(!A !B)		1
	3-input	NAND3C	Y = !(!A !B !C)		1
NOR	2-input	NOR2	Y = !(A + B)		1
		NOR2A	Y = !(!A + B)		1
		NOR2B	Y = !(!A + !B)		1
	3-input	NOR3A	Y = !(!A + B + C)		1
OR-AND		OA1	Y = (A + B) C		1
OR	2-input	OR2	Y = A + B		1
		OR2A	Y = !A + B		1
	3-input	OR3	Y = A + B + C		1

Combinable Hard Macros 2 (for DF1, DF1B, DFC1B, DFC1D, DL1, and DL1B)

Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
AND	3-input	AND3	Y = A B C		1
		AND3A	Y = !A B C		1
		AND3C	Y = !A !B !C		1
	4-input	AND4B	Y = !A !B C D		1
		AND4C	Y = !A !B !C D		1
AND-OR		AO1	Y = (A B) + C		1
		AO1B	Y = (A B) + (!C)		1
		AO1C	Y = ((!A) B) + (!C)		1
		AO1E	Y = (!A !B) + !C		1
		AO11	Y = A B + ((A + B) C)		1
		AO2	Y = ((A B) + C + D)		1
		AO2A	Y = ((!A B) + C + D)		1
		AO2B	Y = (!A !B) + C + D		1
		AO2C	Y = (!A B) + !C + D		1
		AO2D	Y = (!A !B) + !C + D		1
		AO3	Y = (!A B C) + D		1
		AO3B	Y = (!A !B C) + D		1
		AO3C	Y = (!A !B !C) + D		1
		A04A	Y = (!A B C) + (A C D)		1
		AO5A	Y = (!A B) + (A C) + D		1
AND-OR Invert		AOI1A	Y = !((!A B) + C)		1
		AOI1B	Y = !((A B) + !C)		1
		AOI1C	Y = !((!A !B) + C)		1
		AOI2A	Y = !((!A B) + C + D)		1
		AOI3A	Y = !((!A !B !C) + (!A !D)		1
Exclusive OR	XNOR, AND-XOR	AX1B	Y = (!A !B) ^ C		1
Boolean		CS2	Y = !((A + S) B) C + ((A + S) B) D		1
		CY2B	Y = A1 B1 + (A0 + B0) A1 + (A0 + B0) B1		1
Clock Net Interface		GMX4	Y = (D0 !S0 !G) + (D1 !G S0) + (D2 G !S0) + (D3 S0 G)		1
		GNAND2	Y = !(A G)		1
		GXOR2	Y = A ^ G		1
AND-OR		MAJ3	Y = (A B) + (B C) + (A C)		1
Multiplexor		MX2A	Y = (!A !S) + (B S)		1
		MX2C	Y = (!A !S) + (!B S)		1
	4:1	MX4	Y = (D0 !S0 !S1) + (D1 S0 !S1) + (D2 !S0 S1) + (D3 S0 S1)		1
NAND	2-input	NAND2	Y = !(A B)		1
	3-input	NAND3A	Y = !(!A B C)		1
		NAND3B	Y = !(!A !B C)		1
	4-input	NAND4C	Y = !(!A !B !C D)		1
		NAND4D	Y = !(!A !B !C !D)		1
NOR	3-input	NOR3	Y = !(A + B + C)		1
		NOR3B	Y = !(!A + !B + C)		1
		NOR3C	Y = !(!A + !B + !C)		1
	4-input	NOR4A	Y = !(!A + B + C + D)		1
		NOR4B	Y = !(!A + !B + C + D)		1

Combinable Hard Macros 2 (continued) (for DF1, DF1B, DFC1B, DFC1D, DL1, and DL1B)

Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
OR-AND		OA1A	Y = (!A + B) C		1
		OA1B	Y = (A + B) (!C)		1
		OA1C	Y = (!A + B) (!C)		1
		OA2	Y = (A + B) (C + D)		1
		OA2A	Y = (!A + B) (C+ D)		1
		OA3	Y = ((A + B) C D)		1
		OA3A	Y = ((A + B) !C D)		1
		OA4	Y = (A + B + C) D		1
		OA4A	Y = ((A + B + !C) D)		1
		OA5	Y = (A+B+C)(A+D)		1
OR-AND Invert		OAI1	Y = !((A + B) C)		1
		OAI2A	Y = !((A + B + C) !D)		1
		OAI3A	Y = !((A + B) !C !D)		1
OR	3-input	OR3A	Y = !A + B + C		1
		OR3B	Y = !A + !B + C		1
	4-input	OR4	Y = A + B + C + D		1
		OR4A	Y = !A + B + C + D		1
Exclusive OR	XOR	XOR	Y = A ^ B		1
		XO1	Y = (A ^ B) + C		1
		XO1A	Y = !(A ^ B) + C		1
	XNOR, AND-XOR	XNOR	Y = !(A ^ B)		1
		XA1	Y = (A ^ B) C		1
		XA1A	Y = !(A ^ B) C		1

Non-Combinable Hard Macros

Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
AND	4-input	AND4	Y = A B C D		1
		AND4A	Y = (!A B C D)		1
		AND4D	Y = !A !B !C !D		2
	5-input	AND5B	Y = !A !B C D E		1
OR	2-input	OR2B	Y = !A + !B		1
	3-input	OR3C	Y = !A + !B + !C		1
	4-input	OR4B	Y = !A + !B + C + D		1
		OR4C	Y = !A + !B + !C + D		1
		OR4D	Y = !A + !B + !C + !D		2
	5-input	OR5B	Y = !A + !B + C + D + E		1
NAND	3-input	NAND3	Y = !(A B C)		1
	4-input	NAND4	Y = !(A B C D)		2
		NAND4A	Y = !(!A B C D)		1
		NAND4B	Y = !(!A !B C D)		1
	5-input	NAND5C	Y = !(!A !B !C D E)		1
NOR	4-input	NOR4	X = !(A + B + C + D)		2
		NOR4C	Y = !(!A + !B + !C + D)		1
		NOR4D	Y = !(!A + !B + !C + !D)		1
	5-input	NOR5C	Y = !(!A + !B + !C + D +E)		1
Exclusive OR	XNOR, AND-XOR	AX1	Y = (!A B) ^ C		1
		AX1A	Y = !(!A B) ^ C		2
		AX1C	Y = (A B) ^ C		1
AND-OR		A02E	Y = (!A !B) + !C + !D		1
		AO3A	Y = (A B C) + D		1
		AO6	Y = A B + C D		1
		AO6A	Y = A B + C !D		1
		AO7	Y = A B C + D + E		1
		AO8	Y = (A B) + (!C !D) + E		1
		AO9	Y = (A B) + C + D + E		1
		AO10	Y = (A B + C) (D + E)		1
AND-OR Invert		AOI1	Y = !(A B + C)		1
		AOI2B	Y = !((!A B) + !C + D)		1
		AOI4	Y=!((A B) + (C D))		2
		AOI4A	Y = !(A B + !C D)		1
OR-AND		OA3B	Y = ((!A + B) !C D)		1
OR-AND Invert		OAI3	Y = !((A + B) C D)		1
Multiplexor	2:1	MX2B	Y = (A !S) + (!B S)		1

Non-Combinable Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
Adders	half	HA1	CO = A B S = A ^ B		2
		HA1A	CO = !A B S = !(A ^ B)		2
		HA1B	CO = !(A B) S = !(A ^ B)		2
		HA1C	CO = !(A B) S = (A ^ B)		2
	full	FA1A	CO = (Cl !B !A) + (A !B) + (B Cl A) S = (B !A !Cl) + (CO !A Cl) + (CO A !Cl) + (B A Cl)		2
		FA1B	CO = !A(!B + B Cl) + A(!B Cl) S = !A(!Cl CO + Cl B) + A(!Cl B + Cl CO)		2
		FA2A	CO = (Cl !B !(A0+A1)) + (!B (A0+A1)) + (B Cl (A0+A1)) S = (B !(A0+A1) !Cl) + (CO !(A0+A1) Cl) + (CO(A0+A1) !Cl) + (B(A0+A1)Cl)		2
Boolean		CS1	Y = !(A + S B) C + D (A + S B)		1
		CY2A	Y = A1 B1 + A0 B0 A1 + A0 BO B1		1
		MXT	Y = (!S1 (!S0A D0) + (S0A D1)) + (S1 (!S0B D2 + S0B D3))		2
		MXC1	Y = !(!S A + S B) C + (!S A + S B) D		2
D-type Flip-Flops		DF1	Q = (CLK, D, –, –)	1	
		DF1A	QN = !(CLK, D, –, –)	1	
		DF1B	Q = (!CLK, D, –, –)	1	
		DF1C	QN = !(!CLK, D,– ,–)	1	
	with clear	DFC1	Q = (CLK, D, CLR, –)	1	1
		DFC1A	Q = (!CLK, D, CLR, –)	1	1
		DFC1B	Q = (CLK, D, !CLR, –)	1	
		DFC1D	Q = (!CLK, D, !CLR, –)	1	
		DFC1E	QN = !(CLK, D, !CLR, –)	1	1
		DFC1G	QN = !(!CLK, D, !CLR, –)	1	1
	with enable	DFE	Q = (CLK, !E Q + E D, –, –)	1	
		DFE1B	Q = (CLK, !E D + E Q, –, –)	1	
		DFE1C	Q = (!CLK, D !E + Q E, –, –)	1	
		DFE3A	Q = (CLK, D E + Q !E, !CLR, –)	1	
		DFE3B	Q = (!CLK, D E + Q !E, !CLR, –)	1	
		DFE3C	Q = (CLK, D !E + Q E, !CLR, –)	1	
		DFE3D	Q = (!CLK, D !E + Q E, !CLR, –)	1	
		DFEA	Q = (!CLK, !E Q + E D, –, –)	1	1

Non-Combinable Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
D-type Flip-Flops (continued)	with multiplexed data	DFM	Q = (CLK, A !S + B S, –, –)	1	
		DFM1B	QN = !(CLK, A !S + B S, –, –)	1	
		DFM1C	QN = !(!CLK, A !S + B S, –, –)	1	
		DFM3	Q = (CLK, A !S + B S, CLR, –)	1	1
		DFM3B	Q = (!CLK, A !S + B S, !CLR, –)	1	
		DFM3E	Q = (!CLK, A !S + B S, CLR, –)	1	1
		DFM4C	QN = !(CLK, !A !S + !B S, –, !PRE)	1	
		DFM4D	QN = !(!CLK, A !S + B S, –, !PRE)	1	
		DFM6A	Q = (CLK, (D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1), !CLR, –)	1	
		DFM6B	Q = (!CLK, (D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1), !CLR, –)	1	
		DFM7A	Q = (CLK, !CLR, (D0 !S0 + D1 S0) !(S10 + S11) + (D2 !S0 + D3 S0) (S10 + S11))	1	
		DFM7B	Q = (!CLK, !CLR, (D0 !S0 + D1 S0) !(S10 + S11) + (D2 !S0 + D3 S0) (S10 + S11))	1	
		DFMA	Q = (!CLK, A !S + B S, –, –)	1	
		DFMB	Q = (CLK, A !S + B S, !CLR, –)	1	
		DFME1A	Q = (CLK, !E A !S + !E B S + E Q, –, –)	1	
	with preset	DFP1	Q = (CLK, D, –, PRE)		2
		DFP1A	Q = (!CLK, D, –, PRE)		2
		DFP1B	Q = (CLK, D, –, !PRE)		2
		DFP1C	QN = !(CLK, D, –, PRE)	1	1
		DFP1D	Q = (!CLK, D, –, !PRE)	2	
		DFP1E	QN = !(CLK, D, –, !PRE)	1	
		DFP1F	Q = (!CLK, D, –, PRE)	1	1
		DFP1G	QN = !(!CLK, D, –, !PRE)		1
	with clear and preset	DFPC	Q = (CLK, D, CLR, PRE)		2
		DFPCA	Q = (!CLK, D, !CLR, PRE)		2
JK Flip-Flops		JKF	Q = (CLK, !Q J + Q K, –, –)	1	
		JKF1B	Q = (!CLK, !Q J + Q K, –, –)	1	
		JKF2A	Q = (CLK, !Q J + Q K, !CLR, –)	1	
		JKF2B	Q = (!CLK, !Q J + Q K, !CLR, –)	1	
		JKF2C	Q = (CLK, !Q J + Q K, CLR, –)	1	1
		JKF2D	Q = (!CLK, !Q J + Q K, CLR, –)	1	1
T-type Flip-Flops		TF1A	Q = (CLK, T !Q + !T Q, !CLR, –)	1	
		TF1B	Q = (!CLK, T !Q + !T Q, !CLR, –)	1	
Data Latch		DL1	Q = (G, D, –, –)	1	
		DL1A	QN = !(G, D, –, –)	1	
		DL1B	Q = (!G, D, –, –)	1	
		DL1C	QN = !(!G, D, –, –)	1	
		DL2A	Q = (G, D, !CLR, PRE)		2
		DL2B	QN = !(!G, D, CLR, PRE)		2
		DL2C	Q = (!G, D, !CLR, PRE)		2
		DL2D	QN = !(G, D, CLR, !PRE)		2

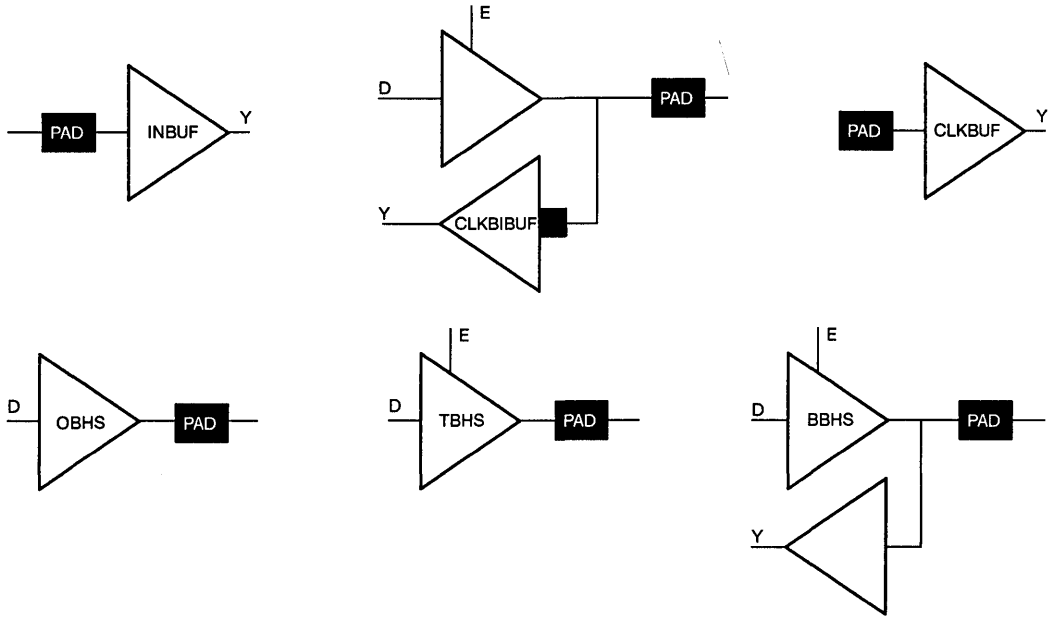
Non-Combinable Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
Data latch (continued)	with clear	DLC	Q = (G, D, !CLR, -)	1	
		DLC1	Q = (G, D, CLR, -)		1
		DLC1A	Q = (!G, D, CLR, -)		1
		DLC1F	QN = !(G, D, CLR, -)		1
		DLC1G	QN = !(!G, D, CLR, -)		1
		DLCA	Q = (!G, D, !CLR, -)	1	
	with enable	DLE	Q = (G, Q !E + D E, -, -)	1	
		DLE1D	QN = !(!G, !E !D + E QN, -, -)	1	
		DLE2A	Q = (!G, Q !E + D E, CLR, -)	1	1
		DLE2B	Q = (!G, D !E + Q E, !CLR, -)	1	
		DLE2C	Q = (!G, !E D + Q E, CLR, -)		1
		DLE3A	Q = (!G, E D + Q !E, -, PRE)		2
		DLE3B	Q = (!G, !E D + Q E, -, PRE)		1
		DLE3C	Q = (!G, !E D + Q E, -, !PRE)		1
		DLEA	Q = (G, Q E + D !E, -, -)	1	
		DLEB	Q = (!G, Q !E + D E, -, -)	1	
		DLEC	Q = (!G, Q E + D !E, -, -)	1	
	with multiplexed data	DLM	Q = (G, A !S + B S, -, -)	1	
		DLM2A	Q = (!G, A !S + B S, CLR, -)	1	1
		DLM3	Q = (G, D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1, -, -)	1	
		DLM3A	Q = (!G, D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1, -, -)	1	
		DLMA	Q = (!G, A !S + B S, -, -)	1	
	with multiplexed data and enable	DLME1A	Q = (!G, A !S !E + B S !E + E Q, -, -)	1	
	with preset	DLP1	Q = (G, D, -, PRE)		1
		DLP1A	Q = (!G, D, -, PRE)		1
		DLP1B	Q = (G, D, -, !PRE)		1
		DLP1C	Q = (!G, D, -, PRE)		1
		DLP1D	QN = !(G, D, -, !PRE)	1	
		DLP1E	QN = !(!G, D, -, !PRE)	1	
Clock Net Interface		CLKINT		clock modules = 1	
Tie-Off		VCC		modules = 0	
		GND		modules = 0	

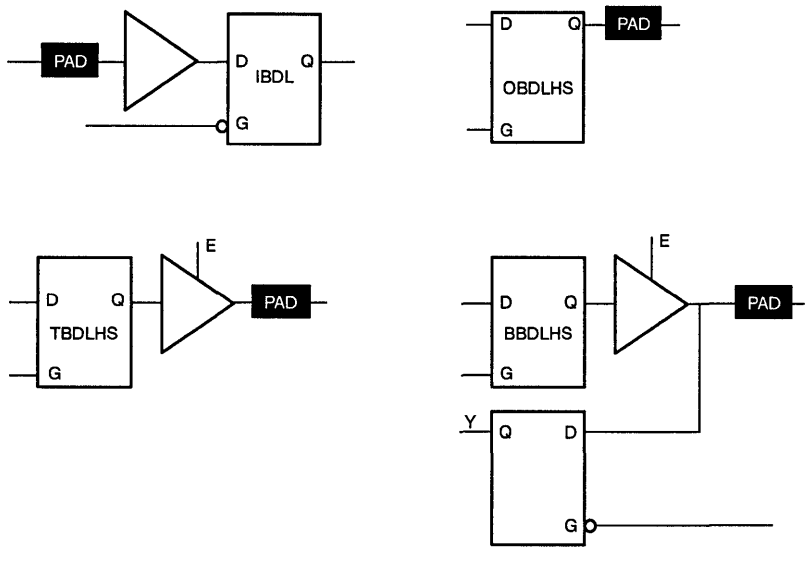
Hard Macro Symbols

I/O Buffers

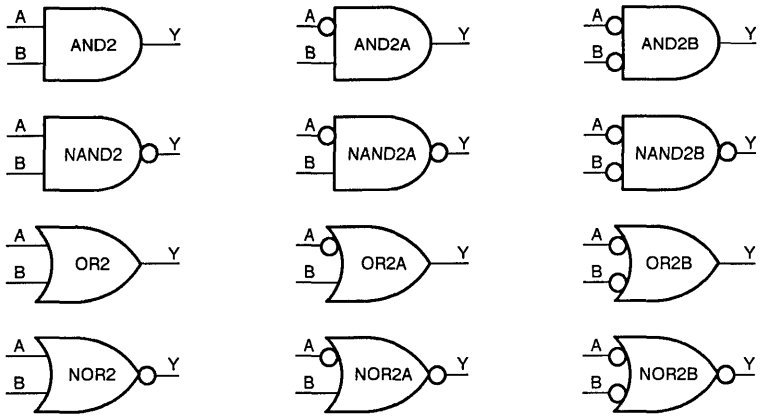
(I/O Module Count = 1)



I/O Buffers with Latches

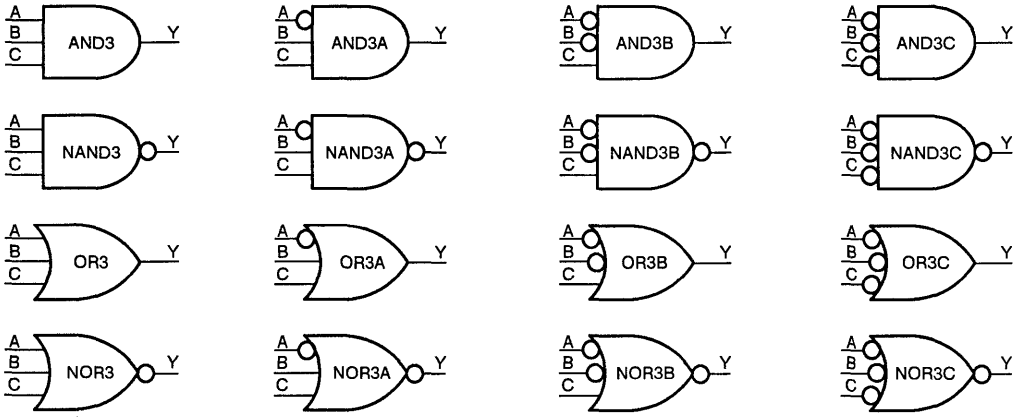


2-Input Gates
(Module Count = 1)



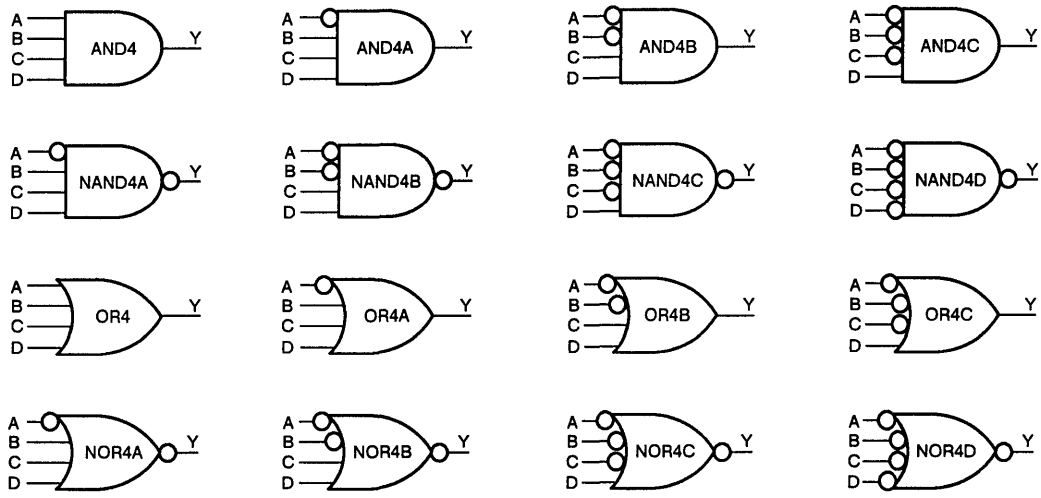
1

3-Input Gates
(Module Count = 1)



4-Input Gates

(Module Count = 1)



(Module Count = 2)

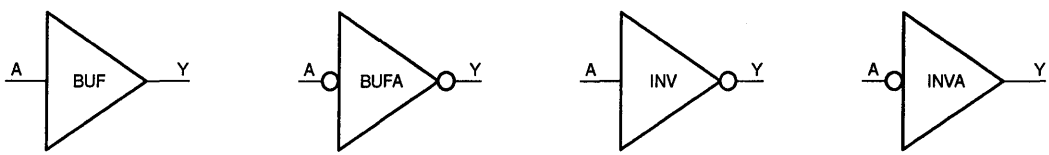
▲ Indicates extra delay input

5-Input Gates

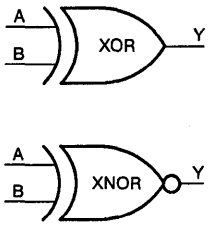
(Module Count = 1)

Buffers

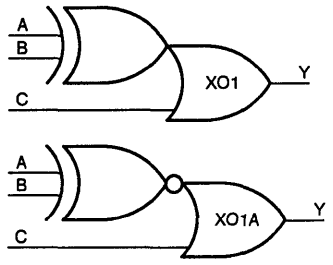
(Module Count = 1)



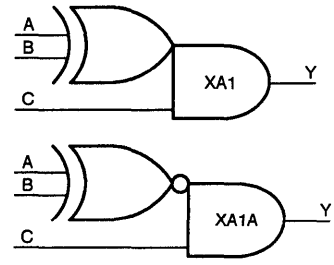
XOR Gates (Module Count = 1)



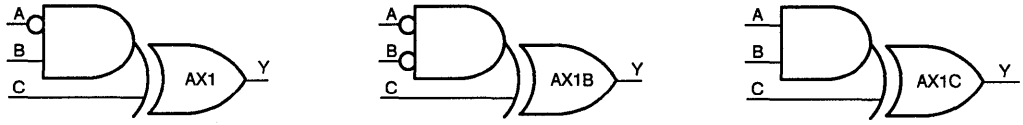
XOR-OR Gates (Module Count = 1)



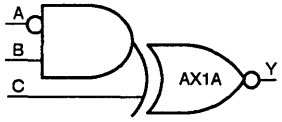
XOR-AND Gates (Module Count = 1)



AND-XOR Gates
(Module Count = 1)



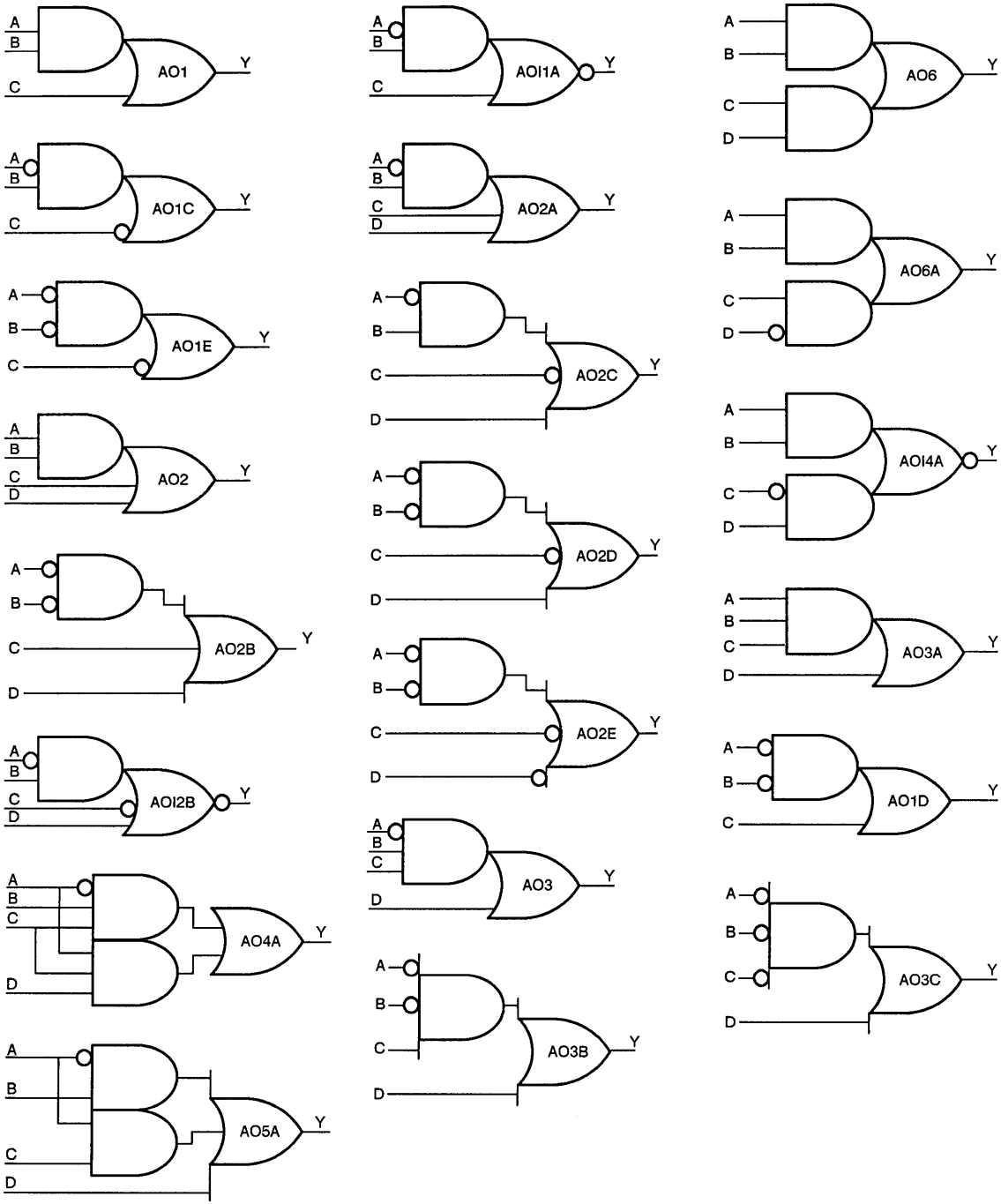
(Module Count = 2)



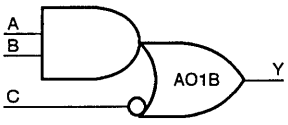
1

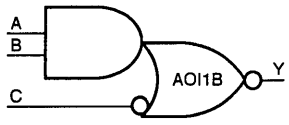
AND-OR Gates

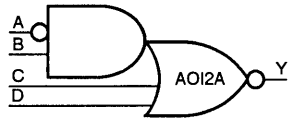
(Module Count = 1)

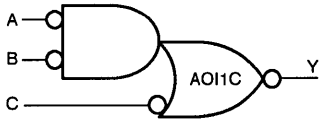


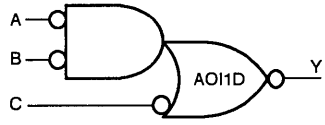
AND-OR Gates, continued
Module Count = 1)

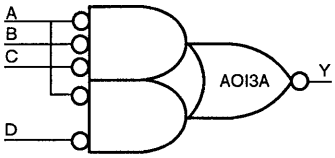


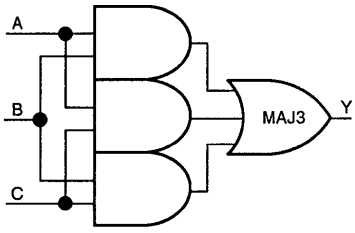


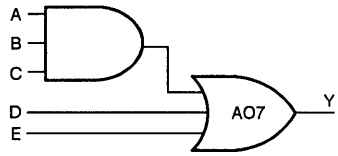


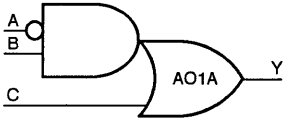


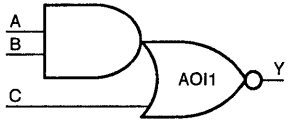




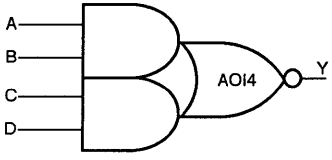


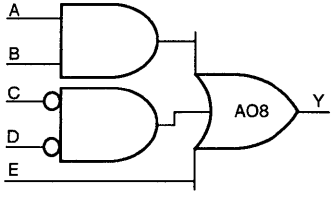


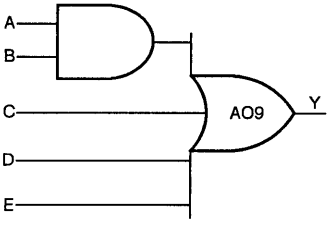


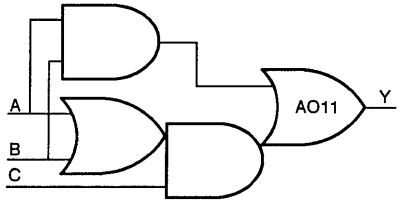


Module Count = 2)





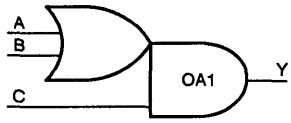


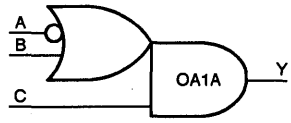


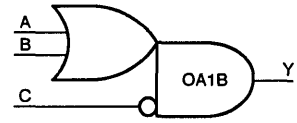
1

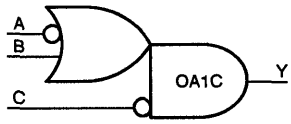
OR-AND Gates

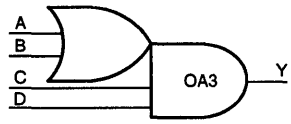
(Module Count = 1)

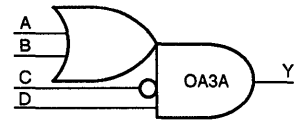


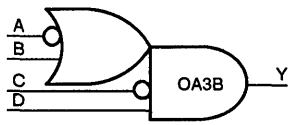


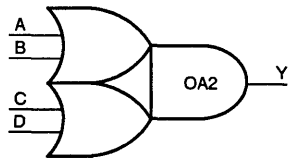


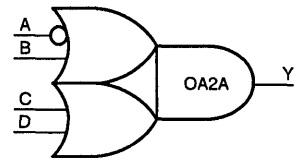


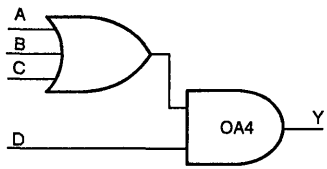


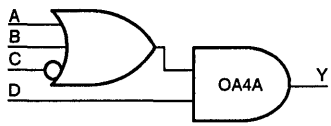


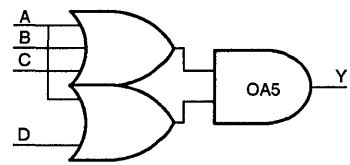


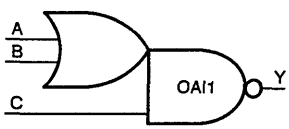


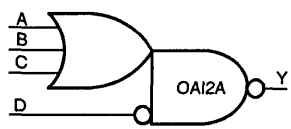


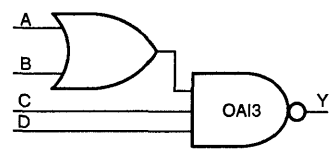


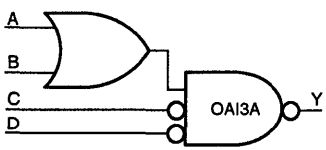


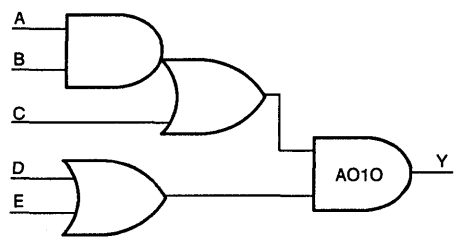






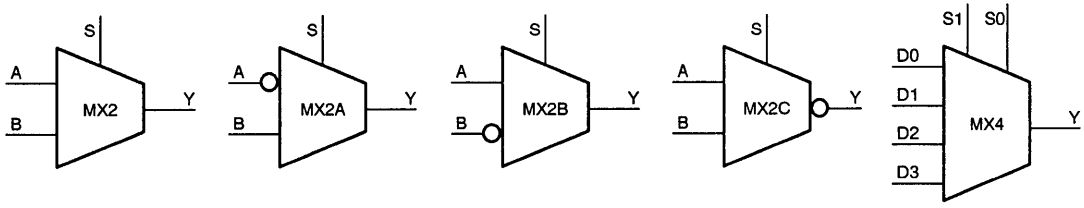




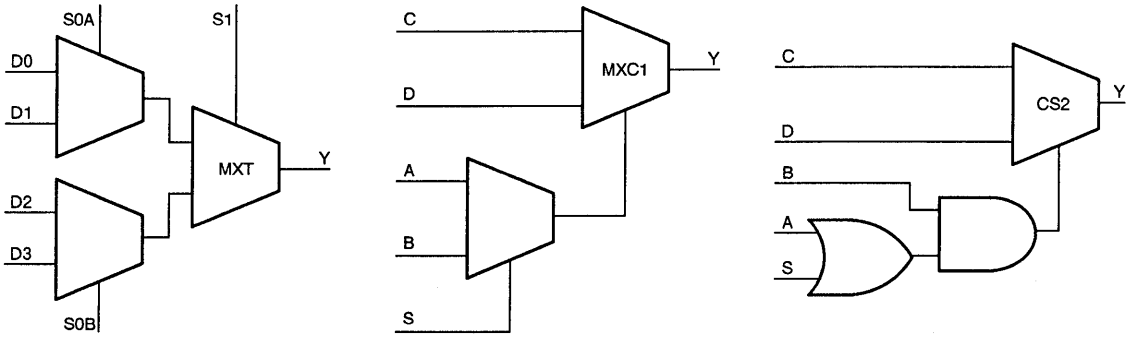


Multiplexors

(Module Count = 1)

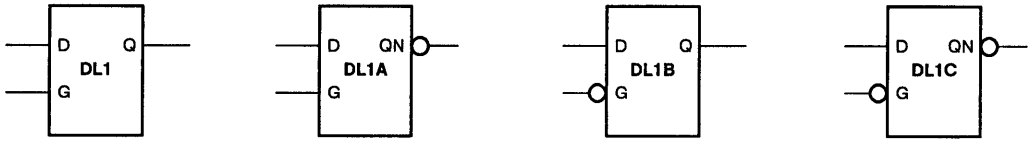


(Module Count = 2)



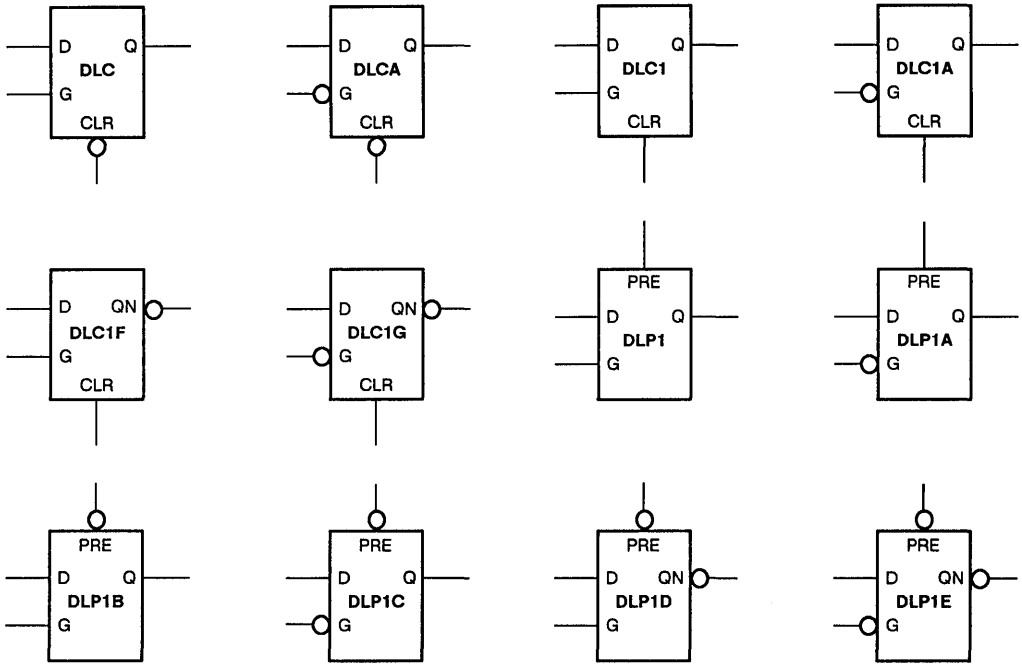
Latches

(Module Count = 1)

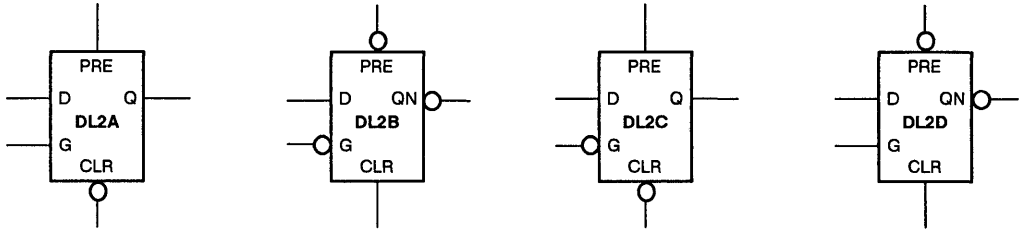


D-Latches with Clear

(Module Count = 1)

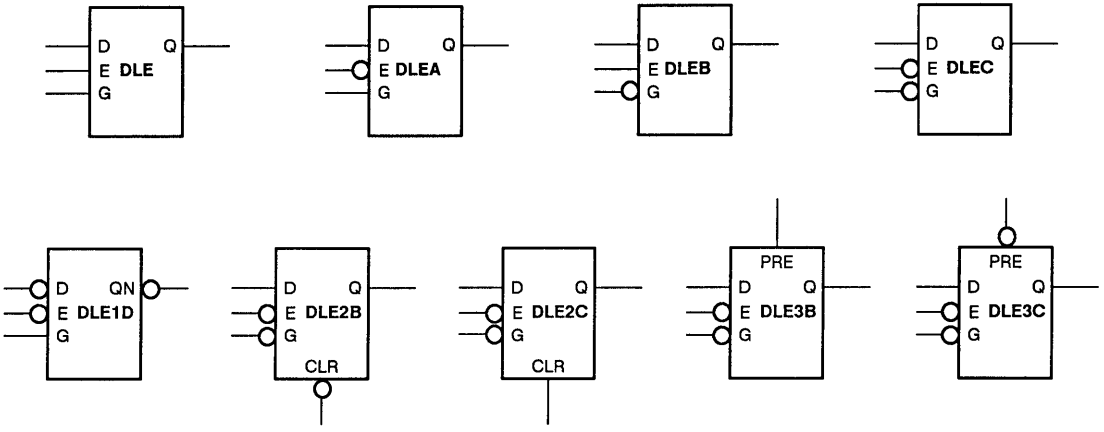


(Module Count = 2)

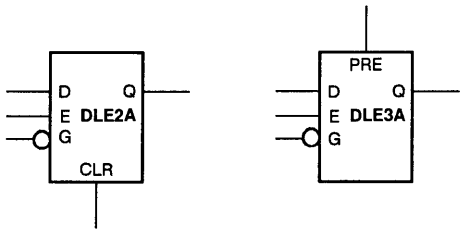


D-Latches with Enable

(Module Count = 1)

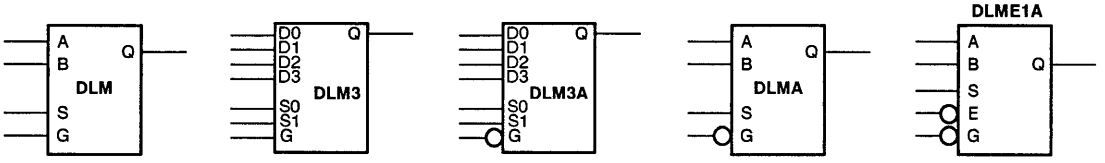


(Module Count = 2)

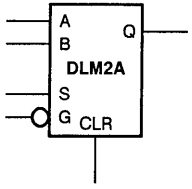


Mux Latches

(Module Count = 1)

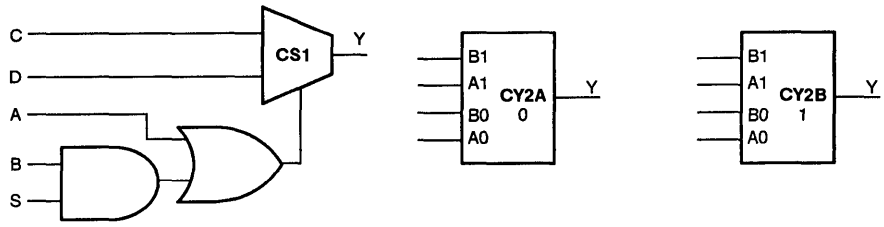


Module Count = 2)

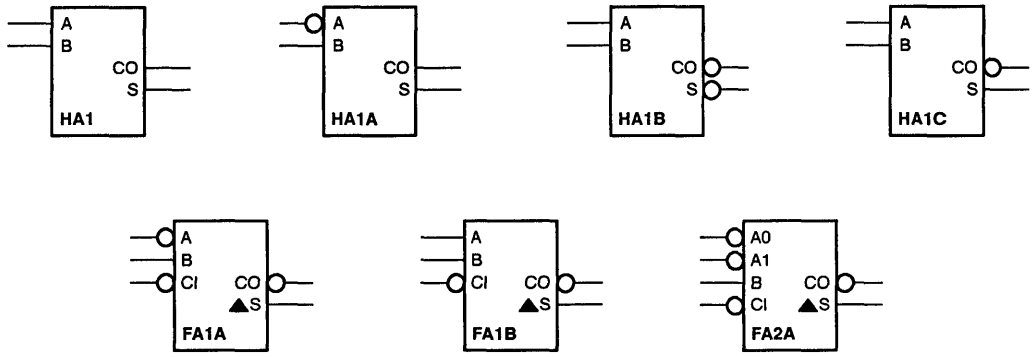


Adders

(Module Count = 1)



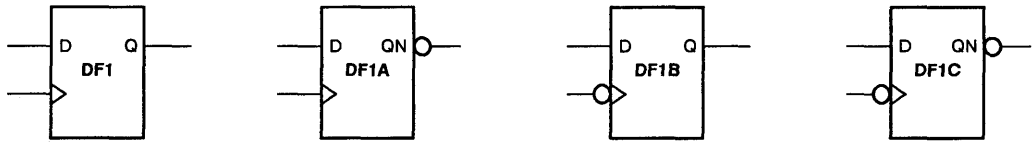
(Module Count = 2)



Macros FA1A, FA1B, and FA2A have two level delays from the inputs to the S outputs, as indicated by the▲

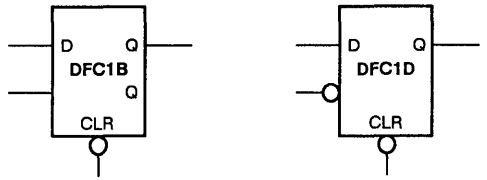
D-Type Flip-Flops

(Module Count = 1)

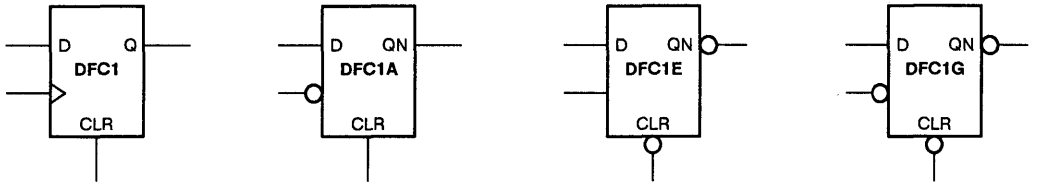


D-Type Flip-Flops with Clear

(Module Count = 1)

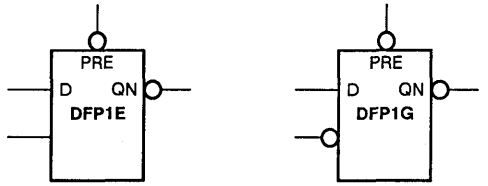


(Module Count = 2)

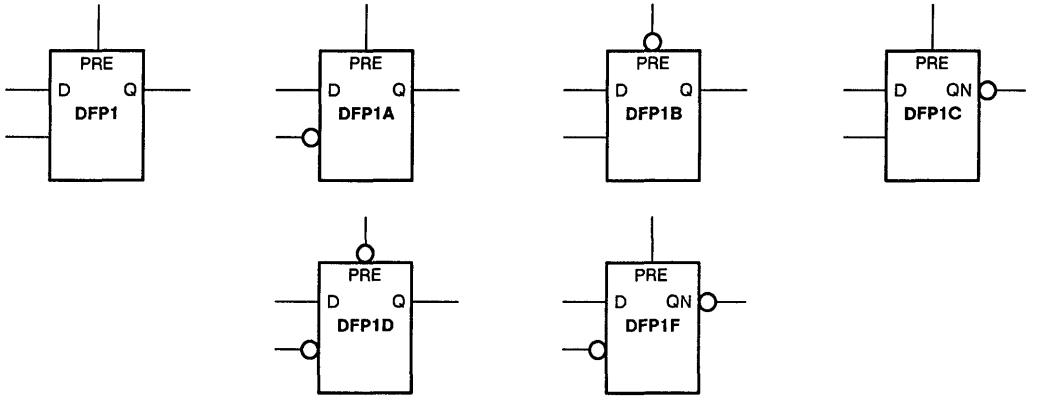


D-Type Flip-Flops with Preset

(Module Count = 1)

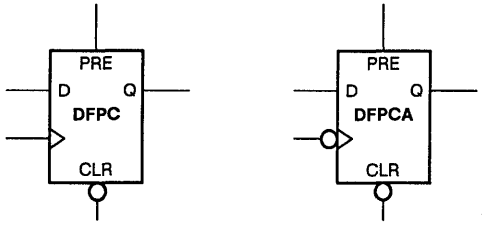


(Module Count = 2)



D-Type Flip-Flops with Preset and Clear

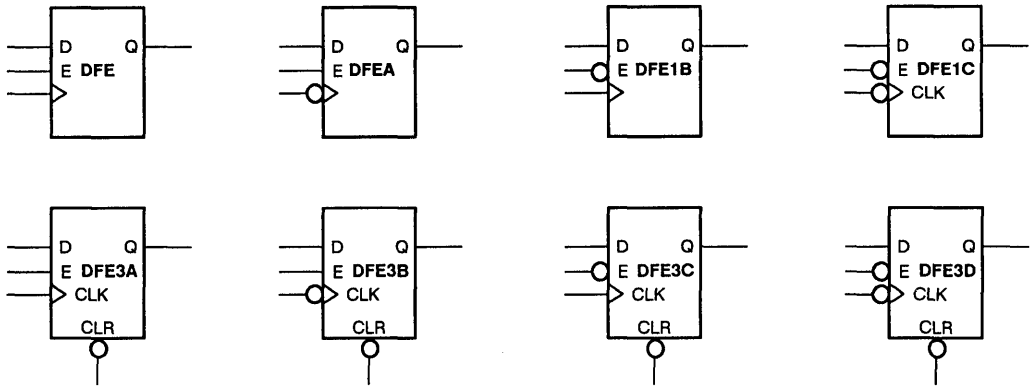
Module Count = 2)



1

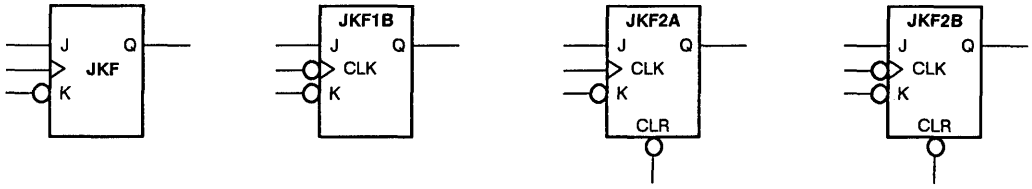
D-Type Flip-Flops with Enable

(Module Count = 1)

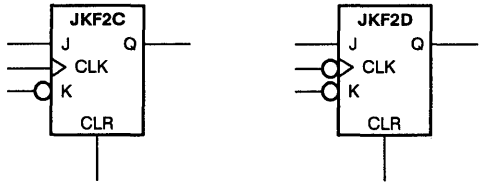


JK Flip-Flops

(Module Count = 1)

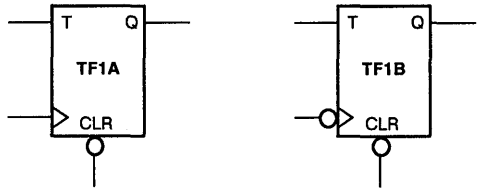


(Module Count = 2)



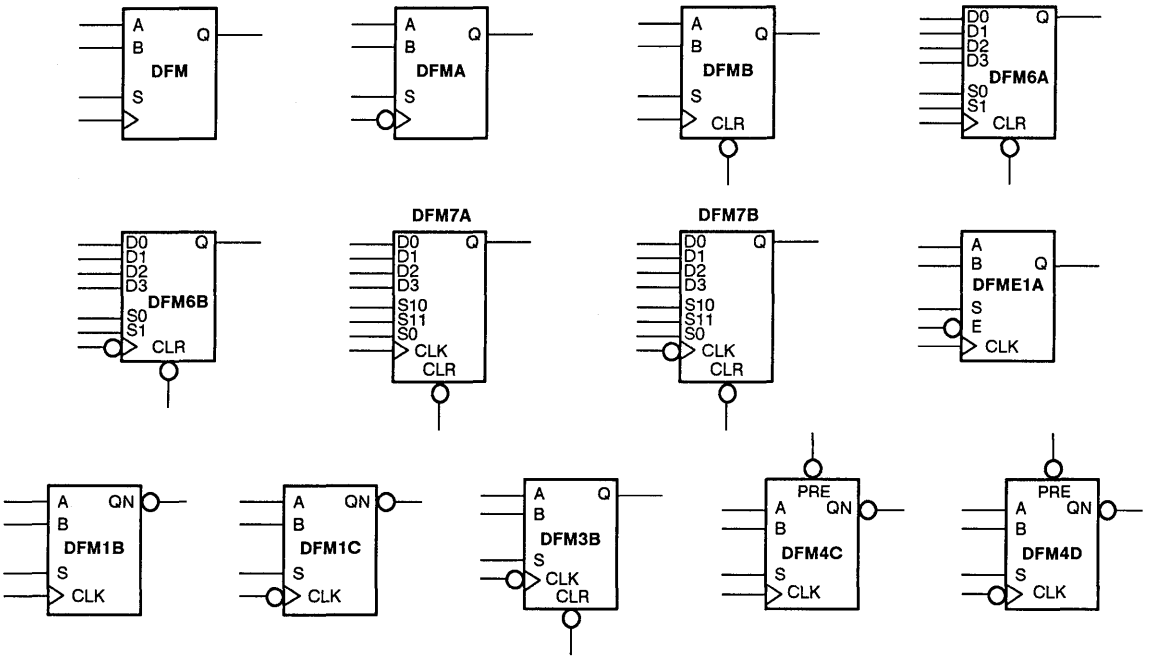
Toggle Flip-Flops

(Module Count = 1)

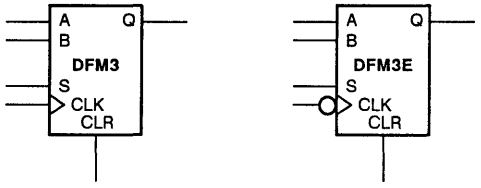


Mux Flip-Flops

(Module Count = 1)

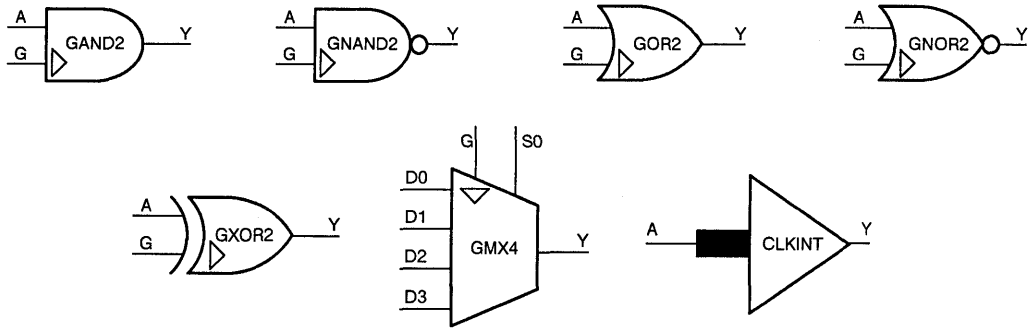


(Module Count = 2)



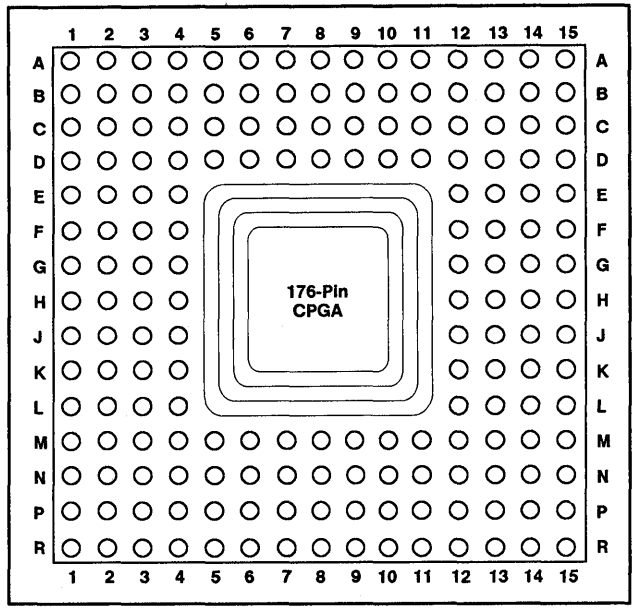
CLKBUF Interface Macros

(Module Count = 1)



▷ Indicates clock input for connection to the global clock networks.

Package Pin Assignments: 176-Pin CPGA
(Top View)

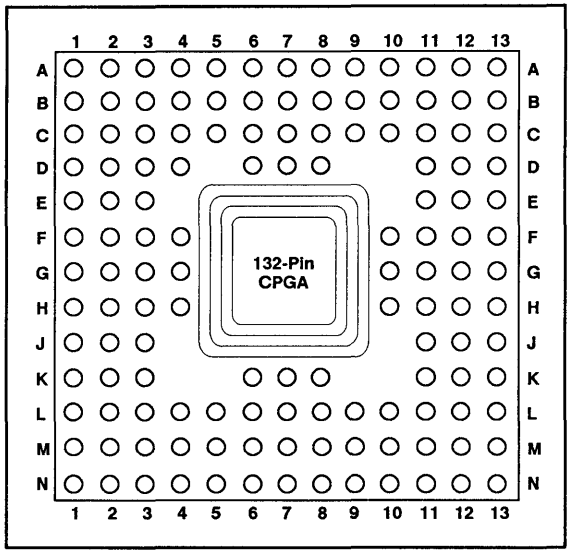


Signal	Pin No.	Location
PRA or I/O	152	C9
PRB or I/O	160	D7
MODE	2	C3
SDI or I/O	135	B14
SDO or I/O	87	P13
DCLK or I/O	175	B3
CLKA or I/O	154	A9
CLKB or I/O	158	B8
GND	1, 8, 18, 23, 33, 38, 45, 57, 67, 77, 89, 101, 106, 111, 121, 126, 133, 145, 156, 165	D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12, K12, J12, H12, F12, E12, D12, D10, C8, D6
V_{CC}	13, 24, 28, 52, 68, 82, 112, 116, 140, 155, 170	F4, H3, J4, M5, N8, M11, H13, G12, D11, D8, D5
V_{PP}	110	J14
V_{SV}	25, 113	H2, H14
V_{KS}	109	J13

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. V_{PP} = V_{CC}, except during device programming.
5. V_{SV} = V_{CC}, except during device programming.
6. V_{KS} = GND, except during device programming.

Package Pin Assignments: 132-Pin CPGA (Top View)

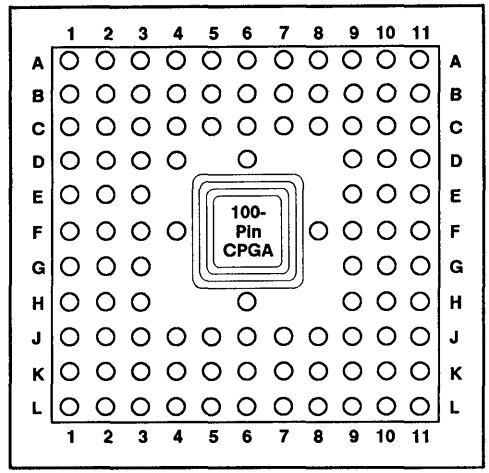


Signal	Pin No.	Location
PRA or I/O	113	B8
PRB or I/O	121	C6
MODE	2	A1
SDI or I/O	101	B12
SDO or I/O	65	N12
DCLK or I/O	132	C3
CLKA or I/O	115	B7
CLKB or I/O	119	B6
GND	9, 10, 26, 27, 41, 58, 59, 73, 74, 92, 93, 107, 108, 125, 126	E3, F4, J2, J3, L5, M9, L9, K12, J11, E12, E11, C9, B9, B5, C5
V_{CC}	18, 19, 49, 50, 83, 84, 116, 117	G3, G2, L7, K7, G10, G11, D7, C7
V_{PP}	82	G13
V_{SV}	17, 85	G4, G12
V_{KS}	81	H13

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

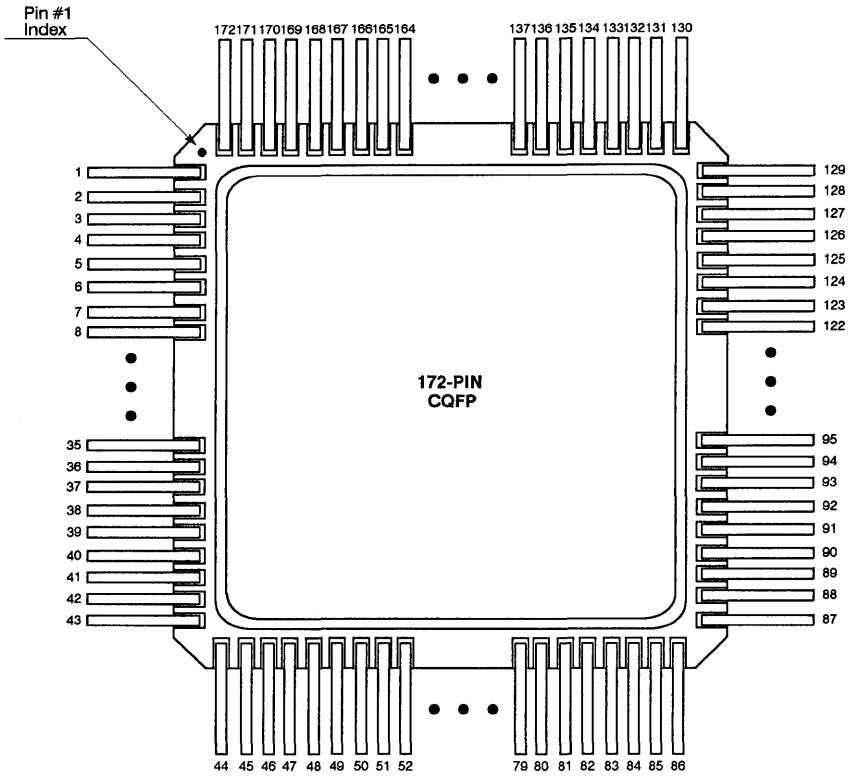
Package Pin Assignments: 100-Pin CPGA (Top View)



Signal	Pin No.	Location
PRA or I/O	85	A7
PRB or I/O	92	A4
MODE	2	C2
SDI or I/O	77	C8
SDO or I/O	50	J9
DCLK or I/O	100	C3
CLKA or I/O	87	C6
CLKB or I/O	90	D6
GND	7, 20, 32, 44, 55, 70, 82, 94	E3, G3, J5, J7, G9, D10, C7, C5
V_{CC}	15, 38, 64, 88	F3, K6, F9, B6
V_{PP}	63	F10
V_{SV}	14, 65	G1, E11
V_{KS}	62	F11

Notes:
1. All unassigned pins are available for use as I/Os.
2. Unused I/O pins are designated as outputs by ALS and driven low.
3. MODE = GND, except during device programming or debugging.
4. V_{PP} = V_{CC}, except during device programming.
5. V_{SV} = V_{CC}, except during device programming.
6. V_{KS} = GND, except during device programming.

Package Pin Assignments: 172-Pin CQFP (Top View)

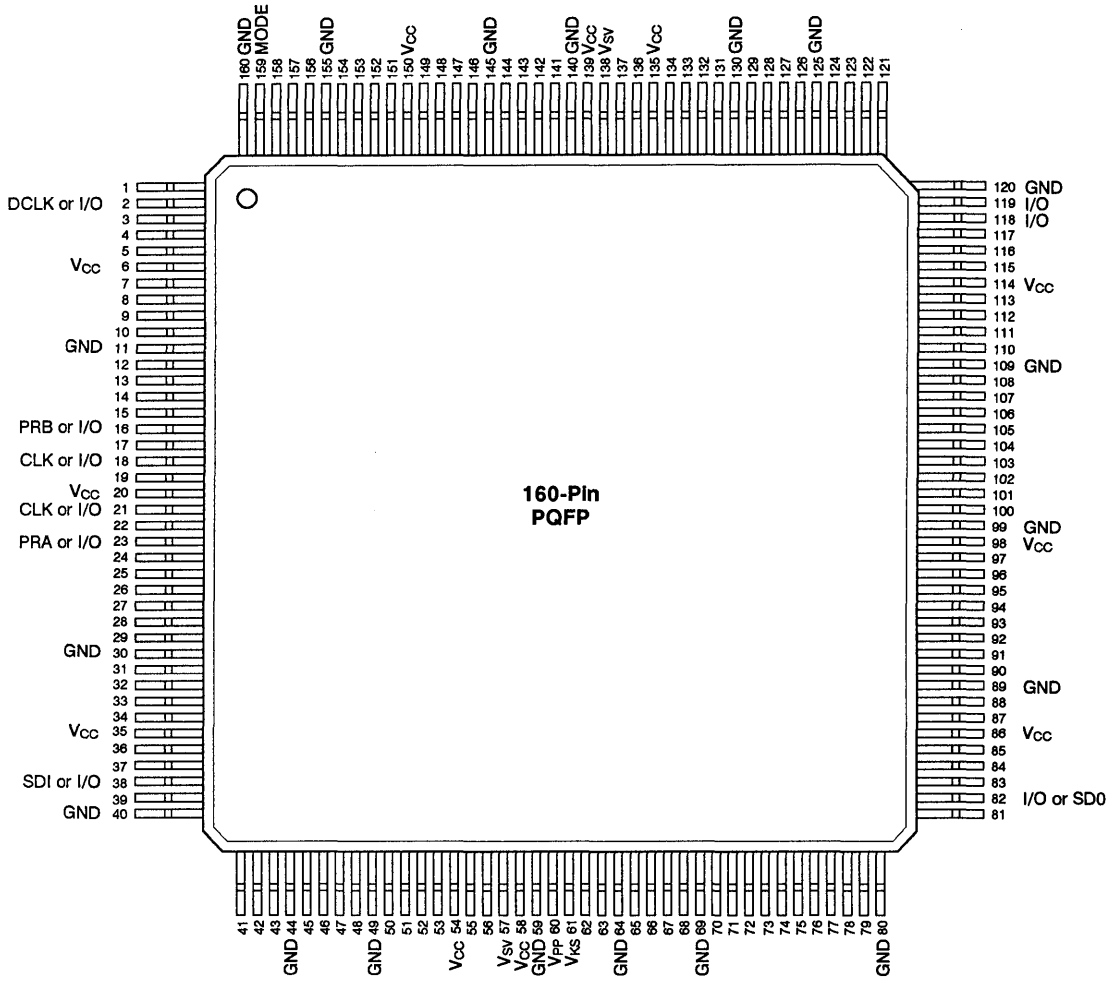


Signal	Pin Number
MODE	1
GND	7, 17, 22, 32, 37, 55, 65, 75, 98, 103, 108, 118, 123, 141, 152, 161
V_{CC}	12, 23 ,27, 50, 66, 80, 109, 113, 136, 151, 166
V_{SV}	24, 110
V_{KS}	106
V_{PP}	107
SDO or I/O	85
SDI or I/O	131
PRA or I/O	148
PRB or I/O	156
CLKA or I/O	150
CLKB or I/O	154
DCLK or I/O	171

Notes:

1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

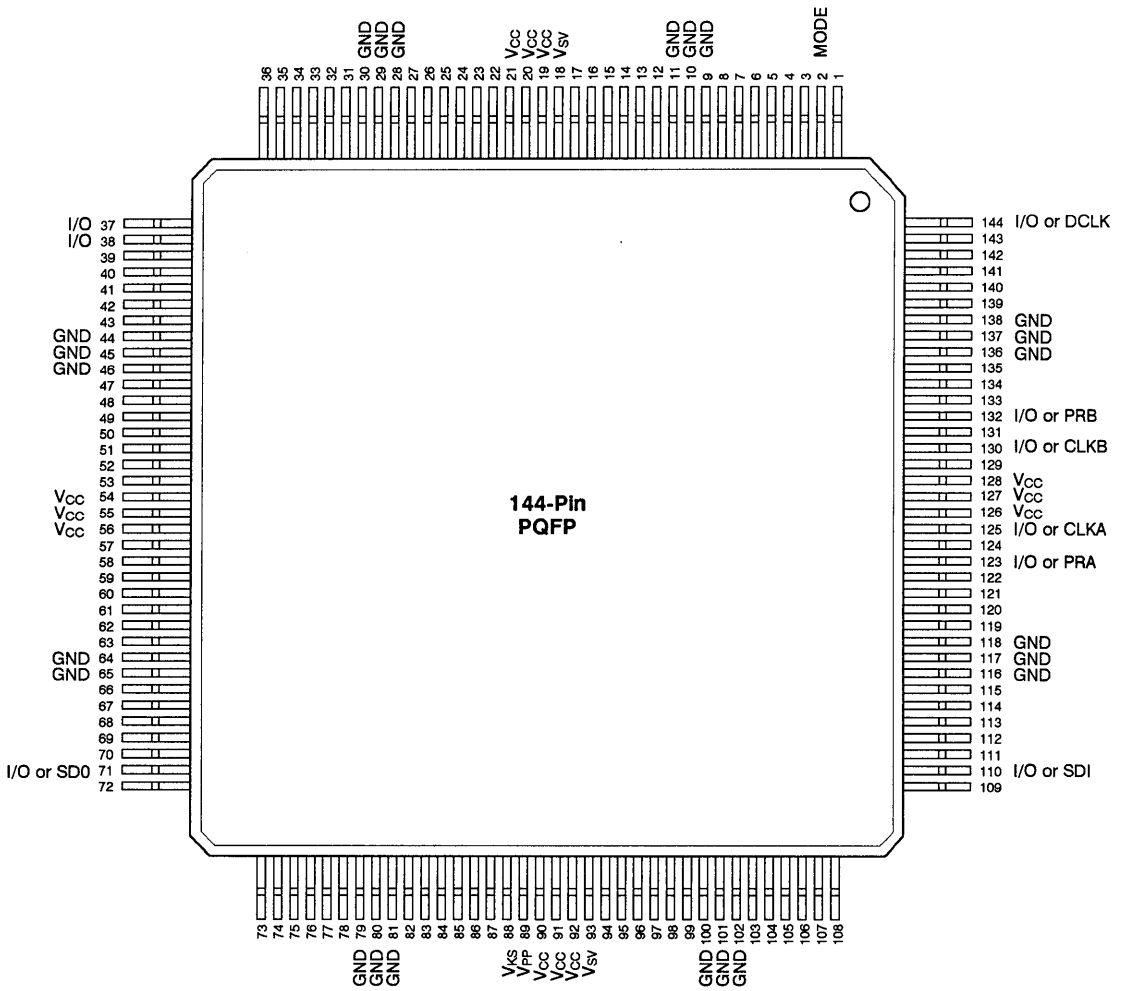
Package Pin Assignments: 160-Pin PQFP (Top View)



Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. V_{PP} = V_{CC}, except during device programming.
5. V_{SV} = V_{CC}, except during device programming.
6. V_{KS} = GND, except during device programming.

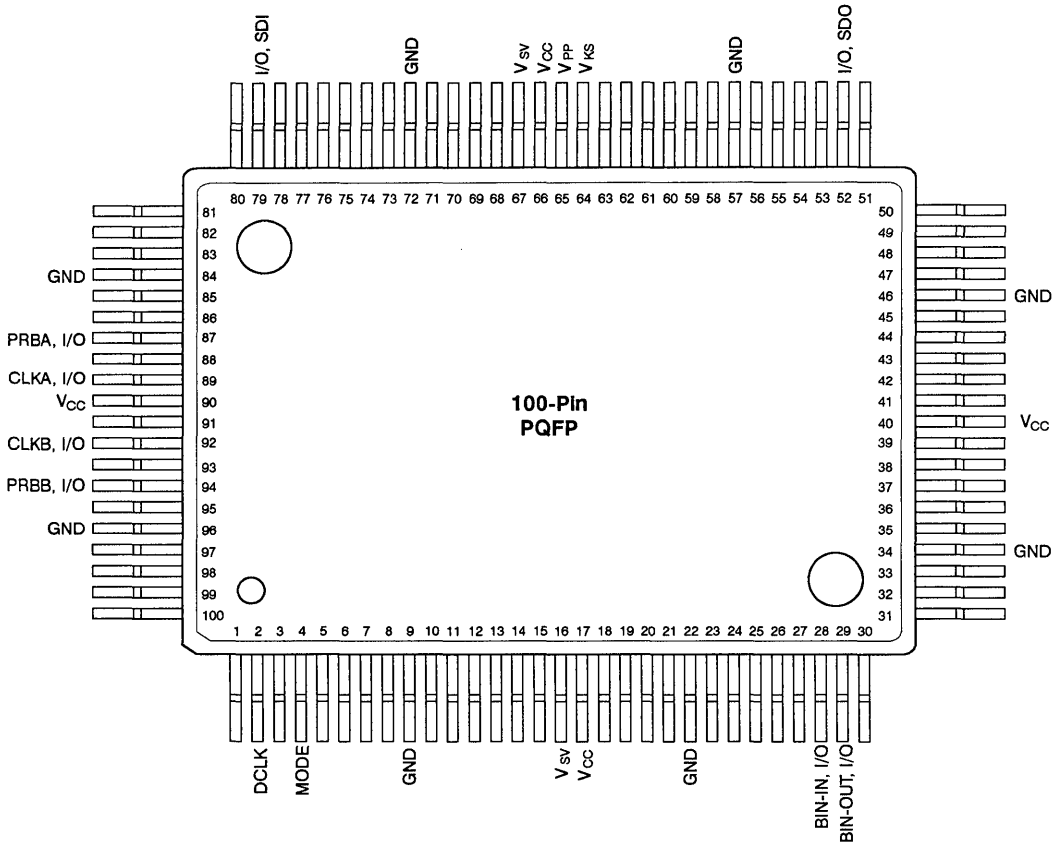
Package Pin Assignments: 144-Pin PQFP (Top View)



Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

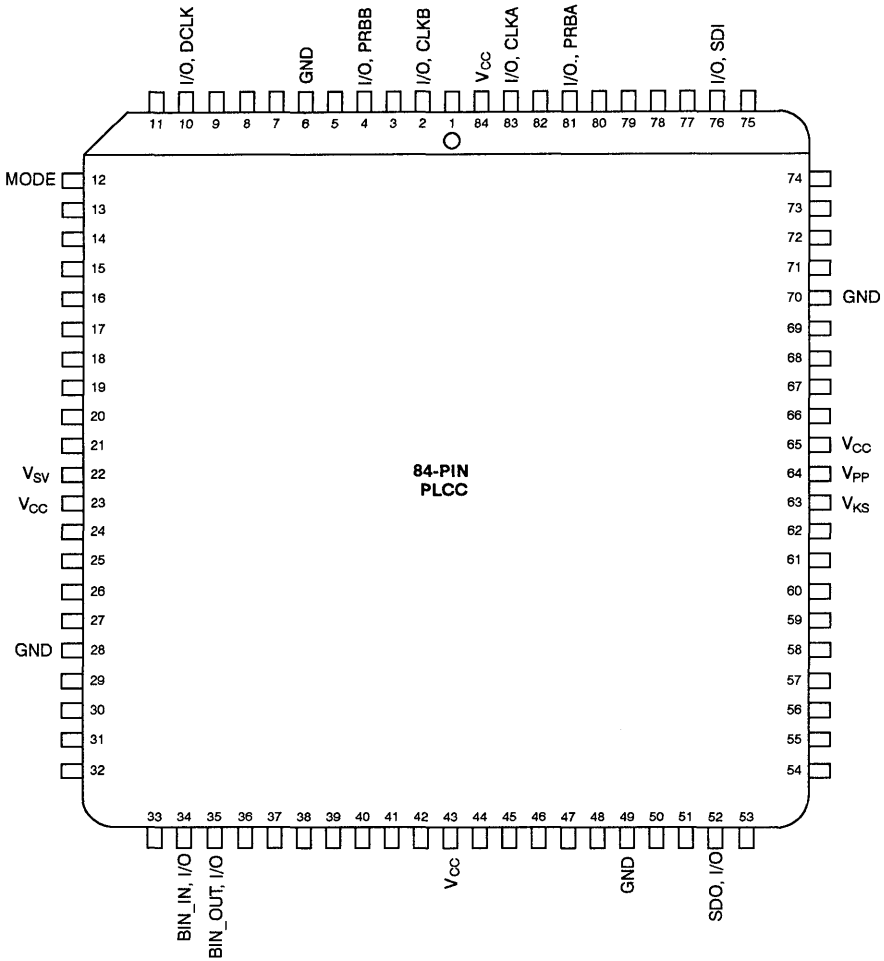
Package Pin Assignments: 100-Pin PQFP (Top View)



Notes:

1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

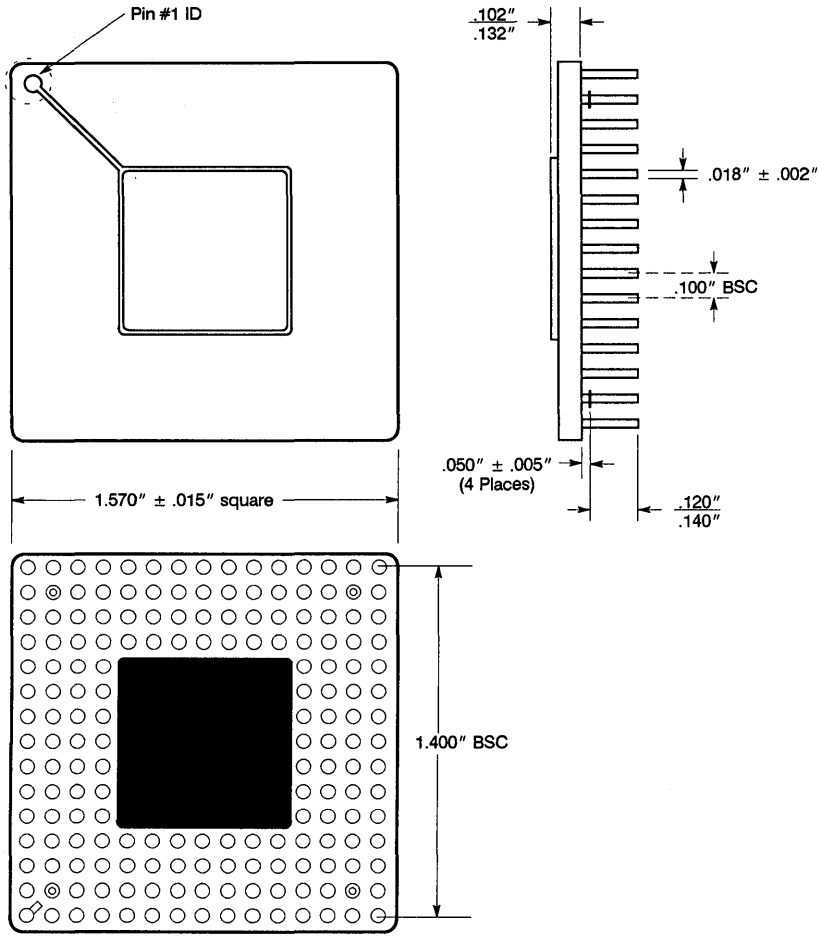
Package Pin Assignments: 84-Pin PLCC (Top View)



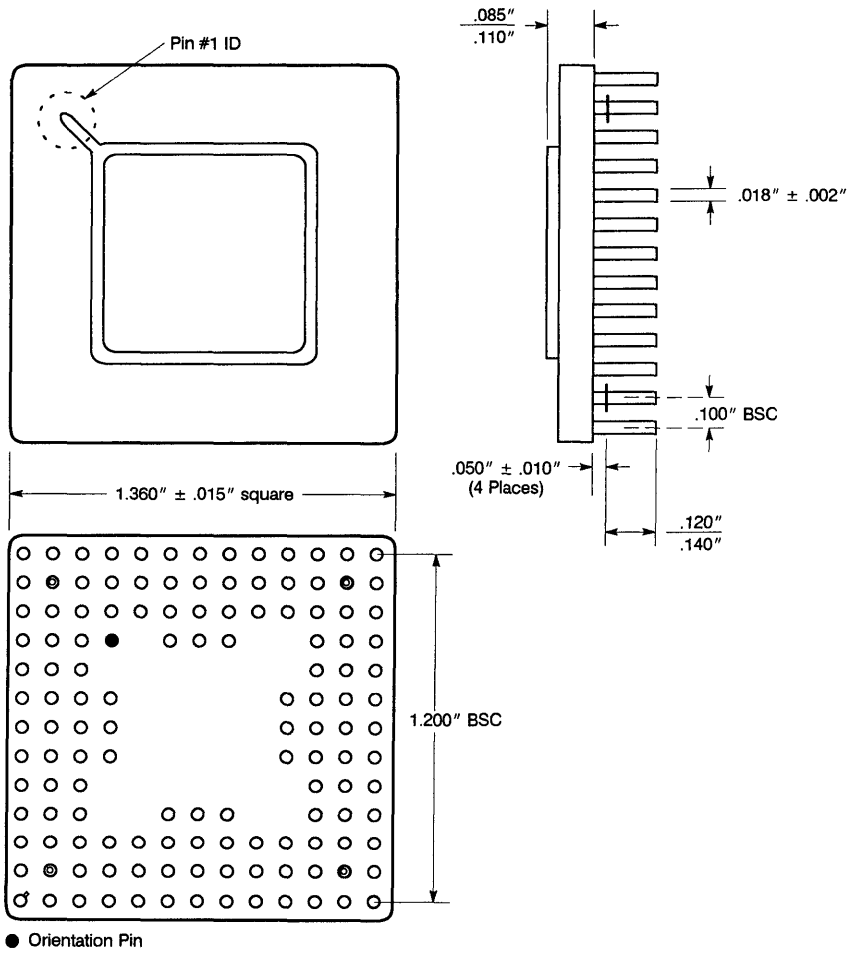
Notes:

1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

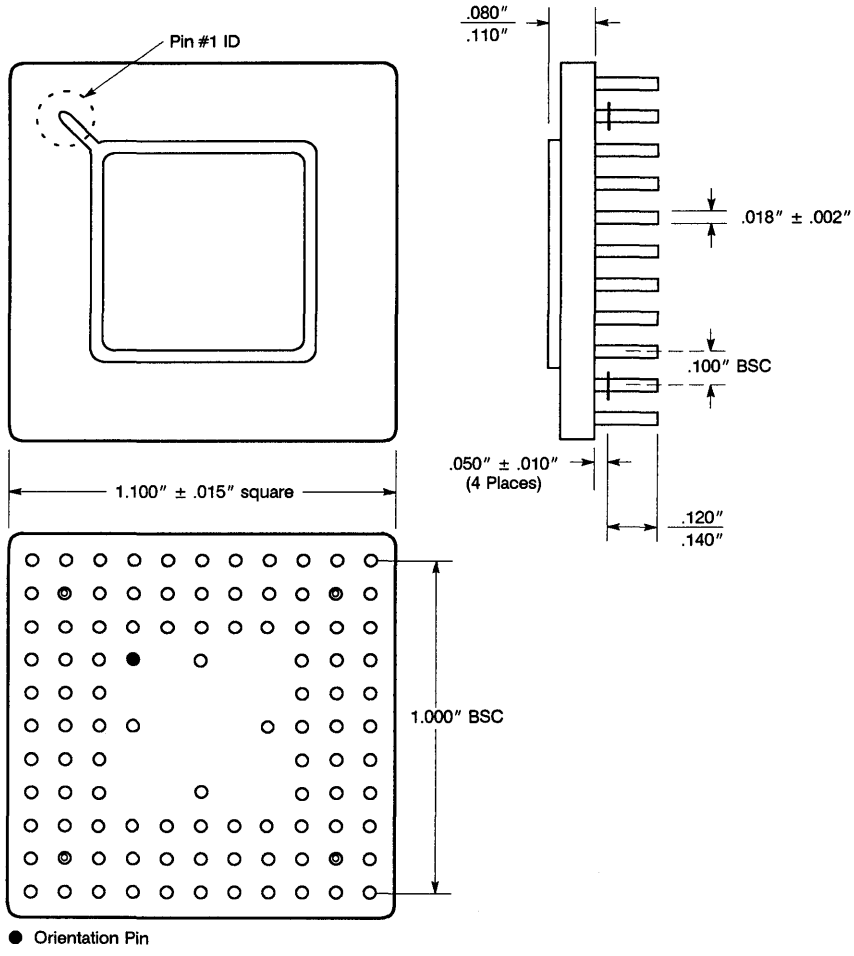
Package Mechanical Details: 176-Pin CPGA



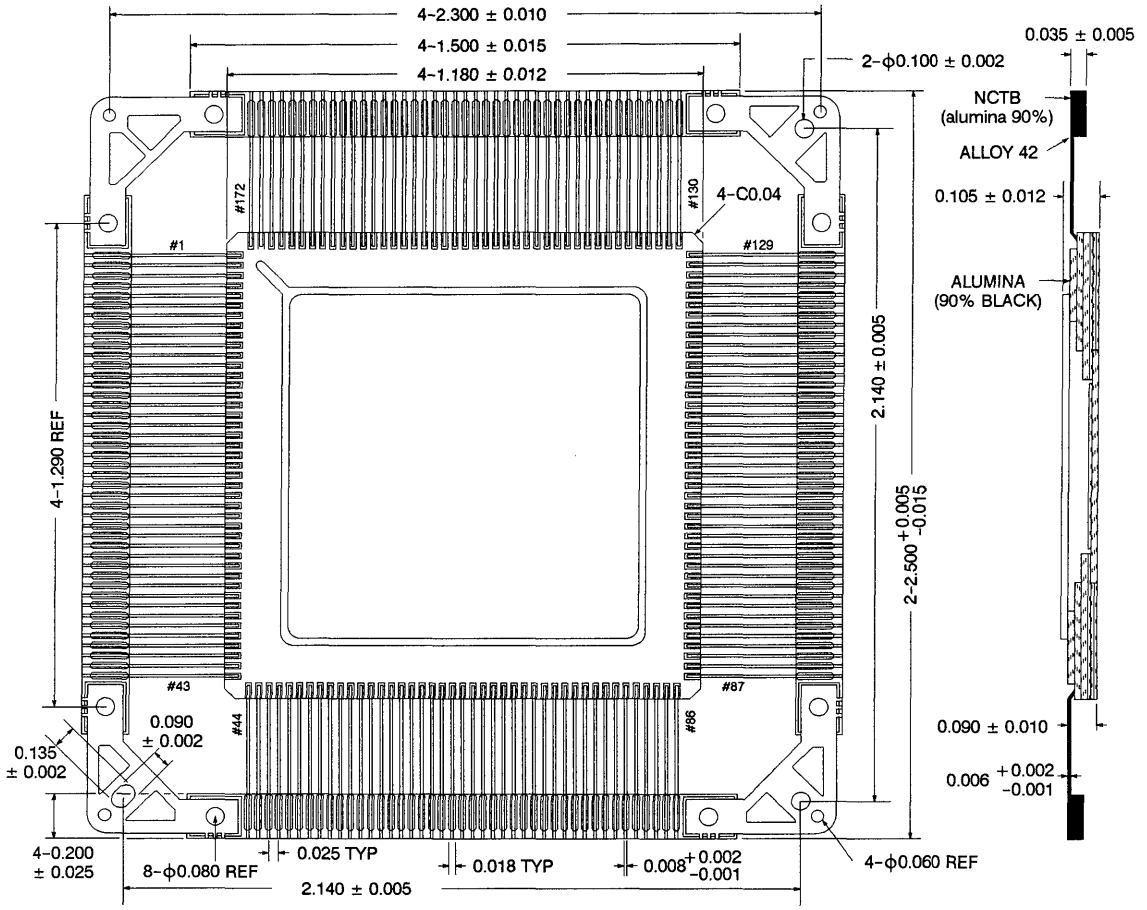
Package Mechanical Details: 132-Pin CPGA

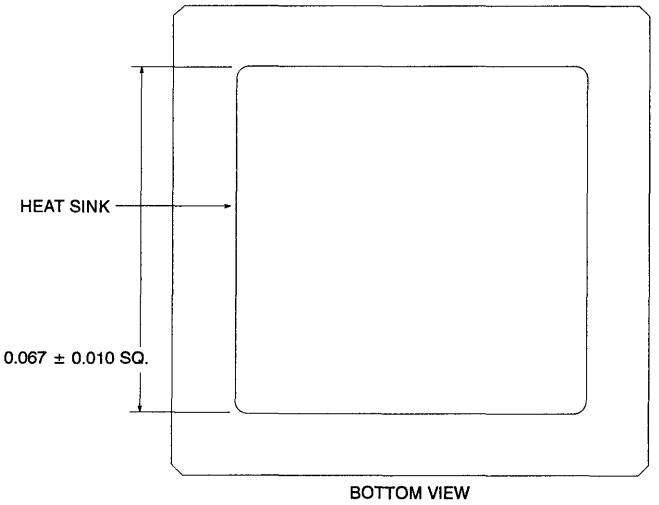


Package Mechanical Details: 100-Pin CPGA



Package Mechanical Details: 172-Pin CQFP

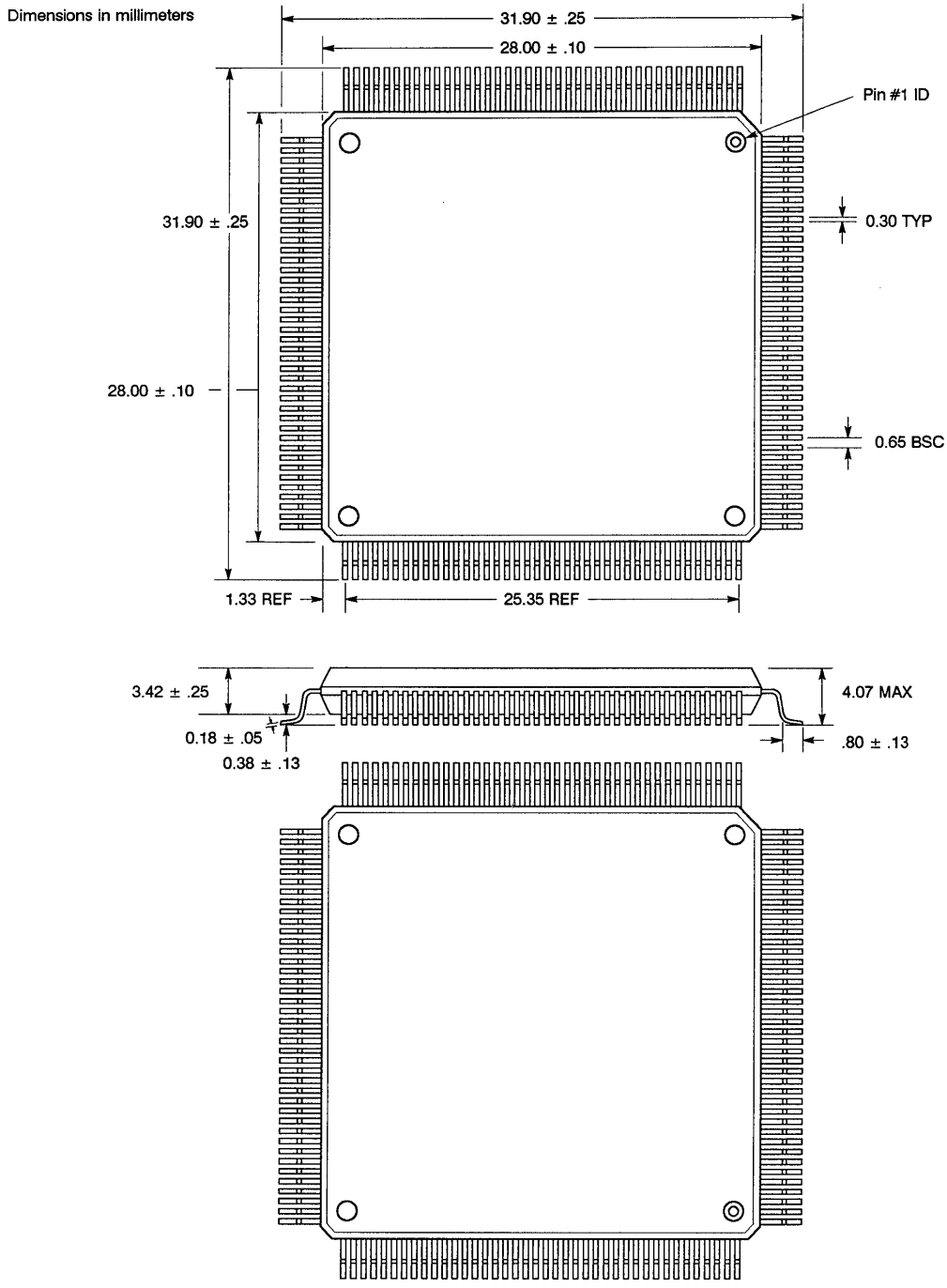




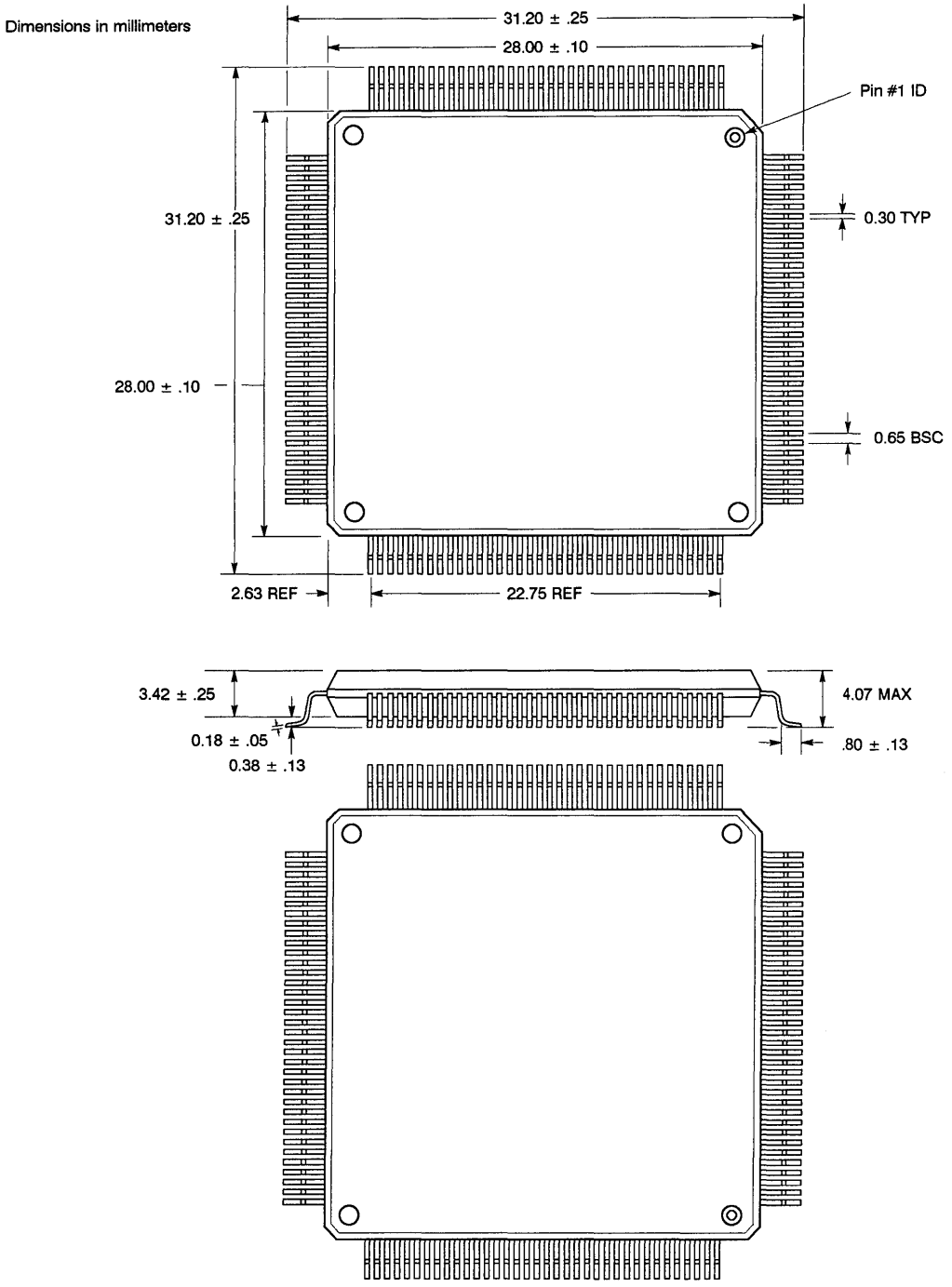
Notes:

1. All exposed metalized areas and leads are gold plated 100 microinches (2.5 μ mm) min. thickness over 80 to 350 microinches 2.0 to 8.9 μ mm) thickness of nickel.
2. Seal ring area is connected to GNDA.
3. Die attach pad is connected to GNDA.
4. GNDQ (4 PLS) is connected to GNDA.
5. Tolerances unless otherwise specified: ±1% N.L.T. ±0.005.

Package Mechanical Details: 160-Pin PQFP

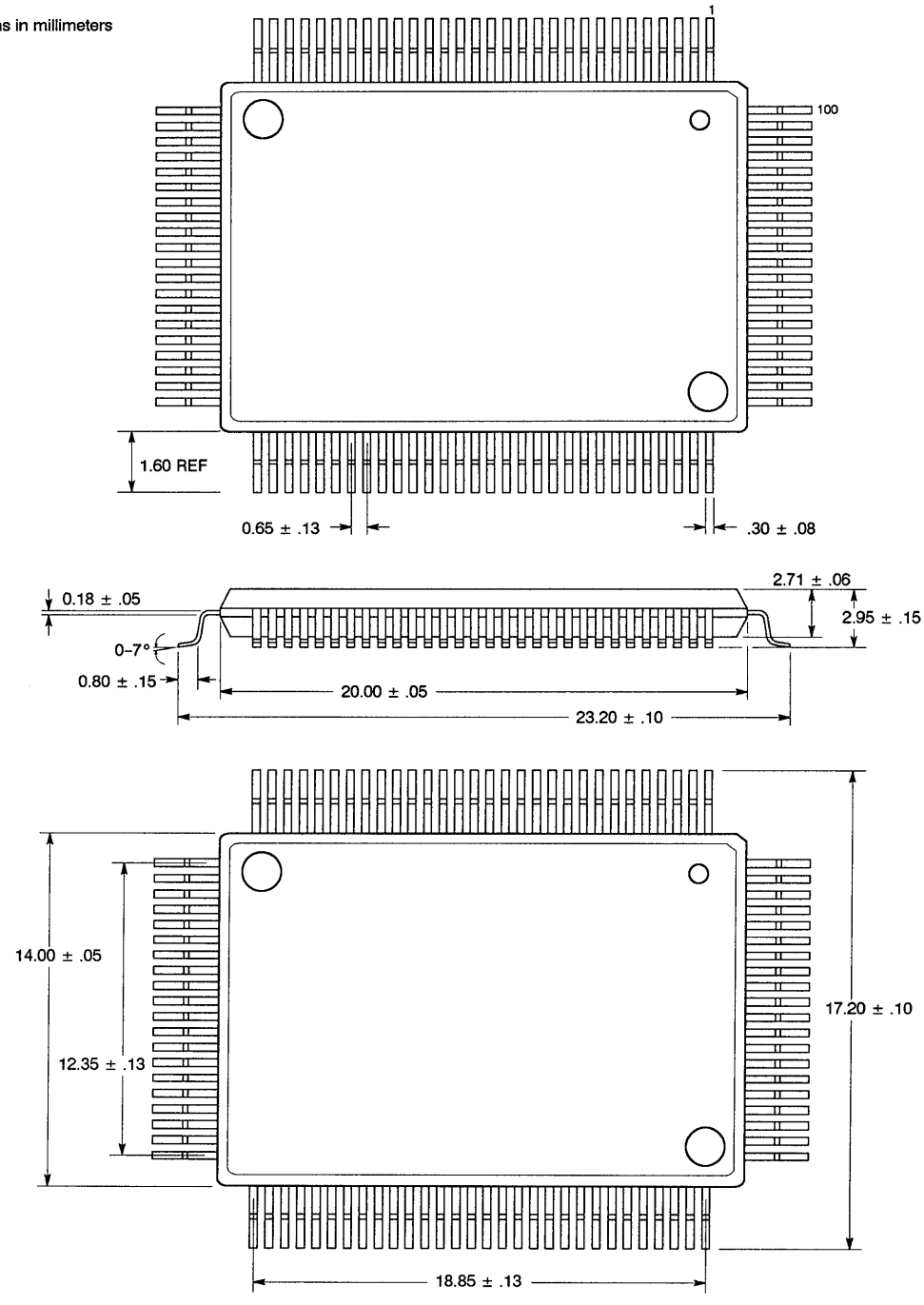


Package Mechanical Details: 144-Pin PQFP

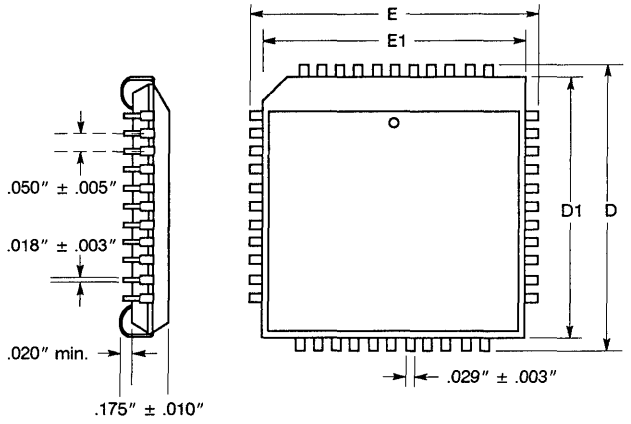


Package Mechanical Details: 100-Pin PQFP

Dimensions in millimeters



Package Mechanical Details: 84-Pin PLCC



Lead Count	D, E	D1, E1
44	.690" ± .005"	.655" ± .005"
68	.990" ± .005"	.955" ± .005"
84	1.190" ± .005"	1.155" ± .005"

Fast Clock to Out with ACT 2 I/O Latches

Applications Note

Introduction

In ACT™ 2 device designs, latched I/O buffer macros can be used to improve clock input to registered output performance. Flip-flops, developed from these I/O latch macros, can improve performance up to 34% over traditional approaches. This applications note compares the use of traditional approaches with the use of I/O latch macros in ACT 2 designs.

Two level-sensitive latches can be combined, as shown in Figure 1, to create a positive edge-sensitive flip-flop.

Where:

$T_{CO} = t_{CQ2}$
$T_{SU} = t_{CLKL} - t_{CQ1} - t_{NET} > t_{SU2}$
t_{SU2} = minimum setup time for slave

Master-Slave Flip-Flops

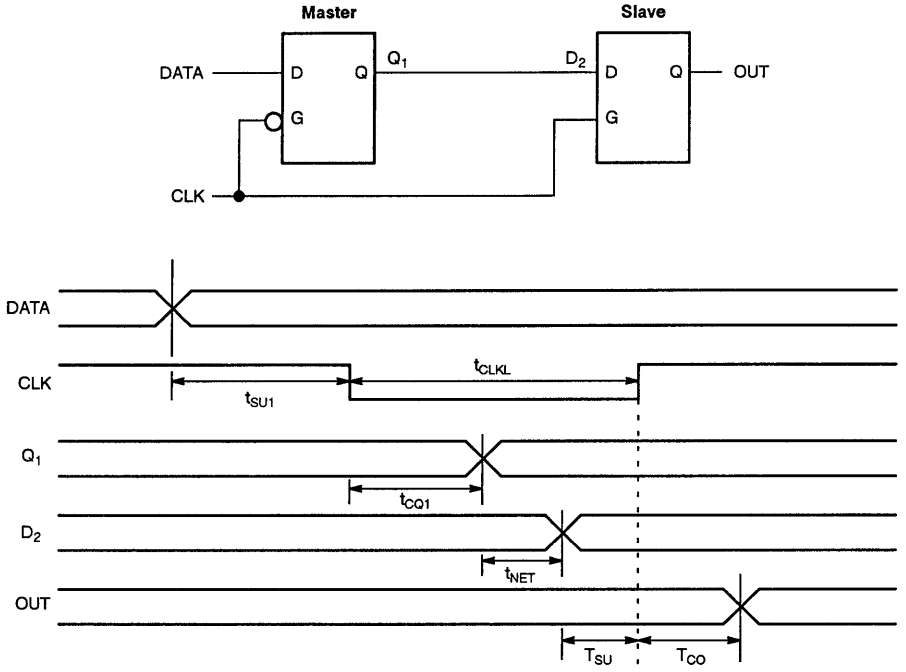
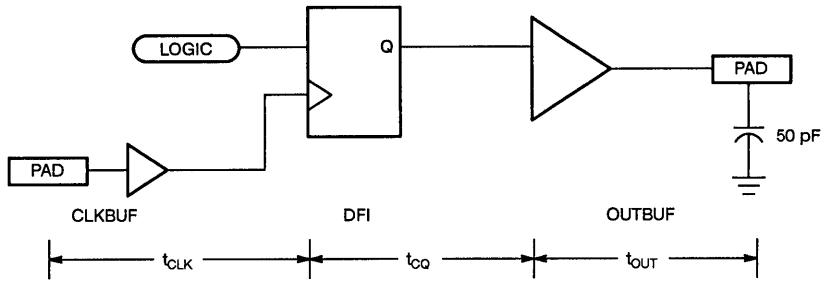


Figure 1. Master-Slave Flip-Flop

The clock to output delay of the resulting flip-flop is determined by the clock to output delay of the slave latch. The clock period low time (t_{CLKL}) must be greater than the clock to output delay of the master latch (t_{CQ1}) plus the net delay from the master latch output (t_{NET}) plus the setup time of the slave latch (t_{SU2}).

Constructing Registered Outputs

You can construct a registered output by combining a flip-flop macro with an output buffer as depicted in Figure 2. The clock to out delay for an A1280-1 under worst-case commercial conditions is 29.0 ns.

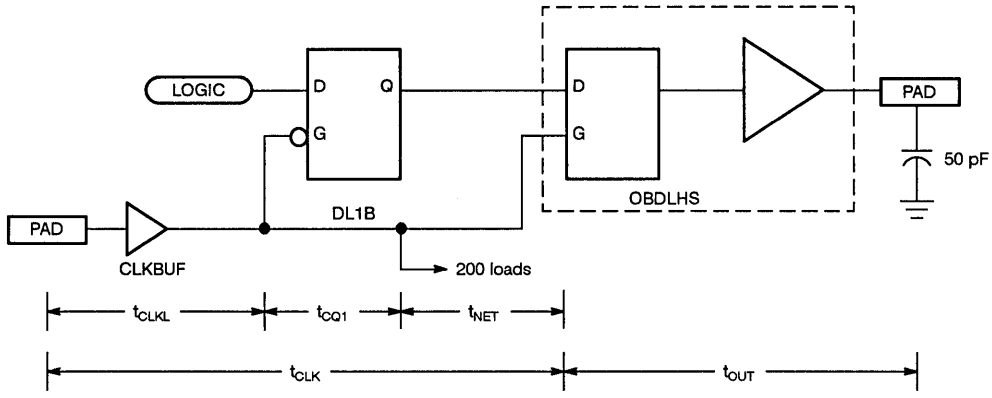


$T_{CO} = (t_{CLK} + t_{CQ} + t_{OUT}) = (12.7 + 7.9 + 8.4)\ ns = 29.0\ ns$

Figure 2. Conventional Registered Output

I/O Latch Flip-Flops

You can also construct a registered output as a master-slave flip-flop, using a latch from the macro library and a latched I/O as shown in Figure 3. In this case, the clock to out delay for an A1280-1 device under commercial worst-case conditions is 21.1 ns. In both cases, the loading on the global clock network is assumed to be equal to 200.



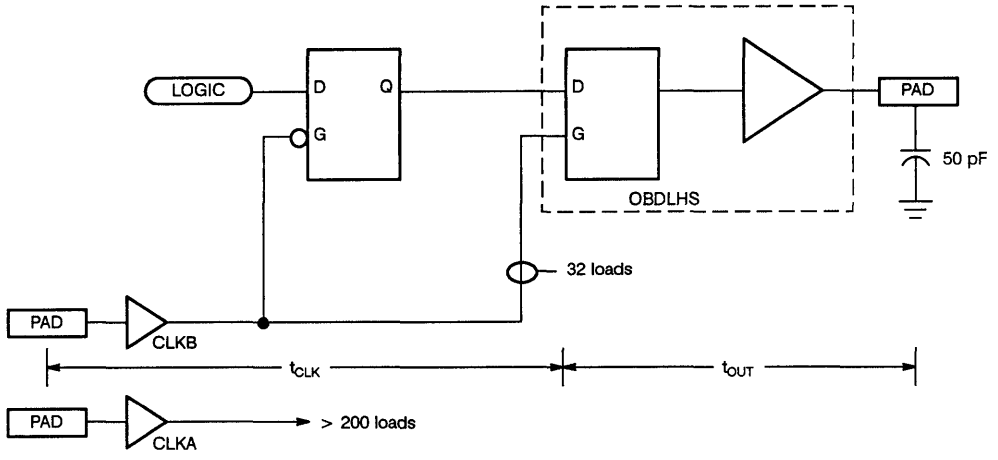
$T_{CO} = (t_{CLK} + t_{OUT}) = (12.7 + 8.4)\ ns = 21.1\ ns$

$T_{SU} = t_{CLKL} - t_{CQ1} - t_{NET} > t_{SU2}$

Figure 3. Master-Slave Registered Output

Dual Clock Approach

Sub-20 ns clock to out can be achieved by utilizing the second global clock network as an I/O clock. In this configuration, shown in Figure 4, CLKA drives the synchronous circuitry on the device and CLKB drives the I/O master-slave latches. Both clock networks are operating at the same frequency and must be connected together external to the device. In this case, a 19.1 ns clock to out delay can be achieved.



$T_{CO} = (t_{CLK} + t_{OUT}) = (10.7 + 8.4)$ ns $= 19.1$ ns

Figure 4. Dual Clock Master-Slave Registered Output

Alternately, an Inbuf can be used to drive the I/O latch, taking care to keep fan-out on the Inbuf less than four to achieve similar performance.

Implementation Rules

Actel strongly suggests following these rules when constructing flip-flops with the I/O latches.

1. Do not put combinatorial macros in the data path between master and slave latches. Added delay may prevent the flip-flop from operating properly.
2. Do not connect the master latch output to any loads except the I/O latch D input.
3. Use a latch made from a sequential module for the master stage. Sequential module latches have better timing characteristics. They also allow combining to take place that can improve the performance of the data being registered. The transparent-low sequential-module latches available are DL1B and DL1C.
4. Use net criticality to insure that the net delay does not violate the setup requirements of the slave latch (as defined in Figure 1). Verify the timing conditions after place and route is complete. Note that an asymmetrical duty cycle on the clock signal (>50% low time) will provide more tolerance on the allowable net delay between latches.
5. Design to combine. The Action Logic™ System (ALS) will automatically combine combinatorial logic into the D input of the DL1B latch if the combiner rules are met.

ACT™ 3 Field Programmable Gate Arrays

Advance Information

Features

- Gate Capacities from Less than 1,000 to Greater than 10,000 Gate Array Gates
- Gate Capacities from Less than 2,500 to Greater than 25,000 PLD/LCA™ Equivalent Gates
- Replace from 30 to 340 TTL Packages
- User I/Os from Less than 100 to Greater than 200
- I/O Performance of 10 ns Clock-to-Out
- 16-bit Counter Performance in Excess of 125 MHz
- System-Level Performance to 75 MHz
- Single-Module Sequential Functions
- Wide-Input Combinatorial Functions
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Four High-Speed Clock Networks
- I/O Drive to 12 mA
- Nonvolatile, User Programmable
- PQFP, PLCC and CPGA Packages

Product Family Profile

	From	To
Capacity		
Gate Array Equivalent Gates	< 1,000	> 10,000
PLD/LCA Equivalent Gates	< 2,500	> 25,000
TTL Equivalent Packages	30	340
User I/Os	< 100	> 200
Performance		
System Speed		75 MHz
16-bit Counters		> 125 MHz
CMOS Process	0.8 µm double-metal CMOS	

Description

The ACT™ 3 family, with devices spanning capacities from less than 1,000 gates to more than 10,000 gates, represents Actel's third generation of field programmable gate arrays. The ACT 3 family provides a group of high performance system solutions, delivering 16-bit counter designs in excess of 125 MHz operation, and supporting system performance of up to 75 MHz operation. The ACT 3 family offers an abundance of I/Os ranging from less than 100 pins to over 200 pins (see Figure 1). The devices are implemented in a silicon gate, 0.8 µm, scaled double-metal CMOS process, and employ Actel's patented PLICE® antifuse technology.

Based on Actel's patented channeled array architecture, the ACT 3 family provides significant enhancements to gate density and performance while maintaining upward compatibility with the ACT 1 and ACT 2 design environments.

ACT 3 devices are designed to meet two primary logic integration requirements: high speed and high user I/O. ACT 3 provides the highest-performance, general-purpose programmable solution available, and the unprecedented design flexibility of the highest pin-to-gate ratios available. The high performance of the ACT 3 family has been achieved through evolutionary enhancements to Actel's proven two-module general-purpose FPGA architecture. These enhancements include four high-speed clock distribution networks and 10 ns clock-to-out I/O modules. The two-module architecture consists of combinatorial and combinatorial-sequential modules. A block diagram of the ACT 3 architecture is shown in Figure 2.

The ACT 3 family is supported by the Action Logic™ System (ALS), which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and debug and diagnostic probe capabilities. The Action Logic System is available on Sun™, HP® and Apollo® workstations, and on 386/486 PC platforms.

ACT 3 Architecture

The ACT 3 family architecture is an evolutionary upgrade from the ACT 2 family. After extensive research into alternate logic module architectures, Actel found that the ACT 2 two-module design is optimal for most applications. The small, simple structure of the logic modules has been retained, with a single enhancement to the sequential logic module. These numerous, general-purpose logic modules constitute a design architecture that provides a high-performance solution for a wide range of applications, as shown in Figure 3.

The I/O module is enhanced significantly, allowing more complex logic functions to be implemented in the I/O module. This significantly increases performance of key device parameters, like clock-to-output. Clocking flexibility is also enhanced over the ACT 2 family with the inclusion of two high-speed dedicated clocks in addition to the two routed clocks. A block diagram of the family architecture is shown in Figure 4.

Two-Module Design

ACT 3 architecture uses the proven multiplexor-based combinatorial module (C-Module) of ACT 2 devices, and an enhanced version of the ACT 2 multiplexor-based combinatorial-sequential module (S-Module). The ACT 3 S-Module combinatorial logic preceding the register is equivalent to the combinatorial logic within the C-module. This allows for more complex logic functions to be implemented in a single level of logic and makes logic synthesis more efficient due to the regular combinatorial structure throughout the device.

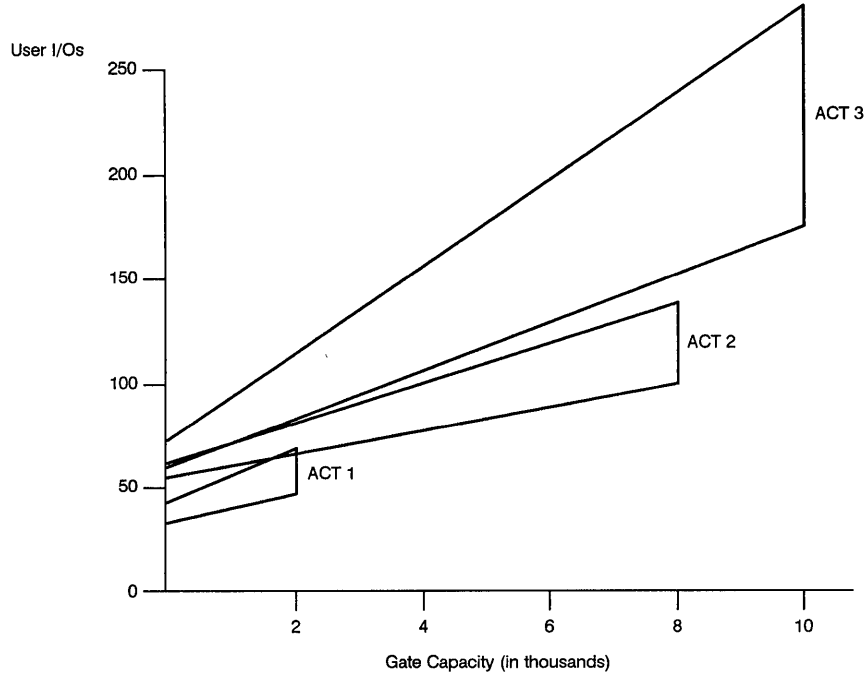


Figure 1. ACT 3 Offers an Abundance of I/Os

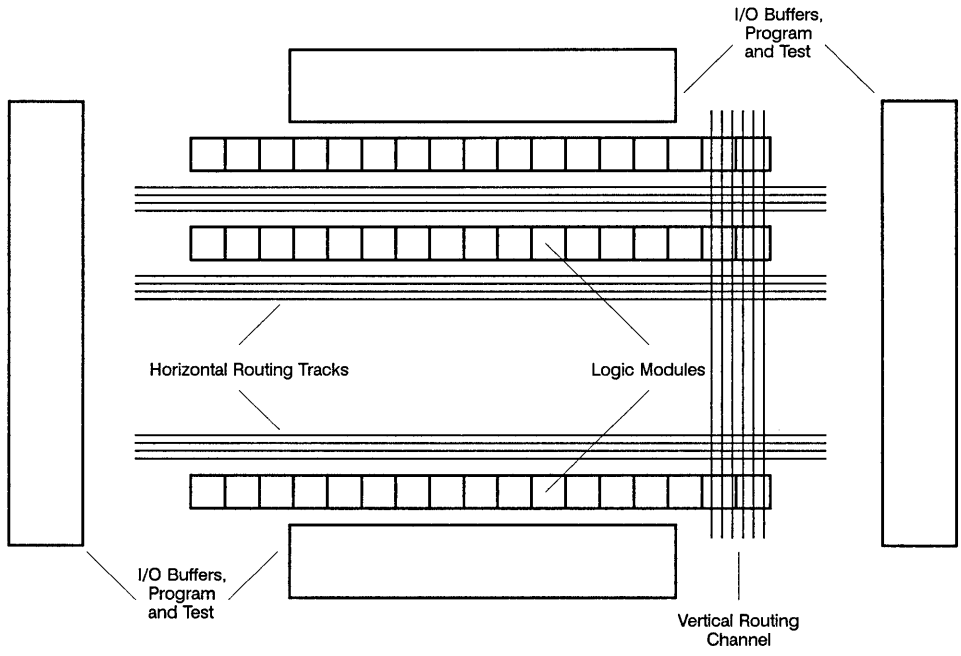


Figure 2. Block Diagram of ACT 3 Architecture

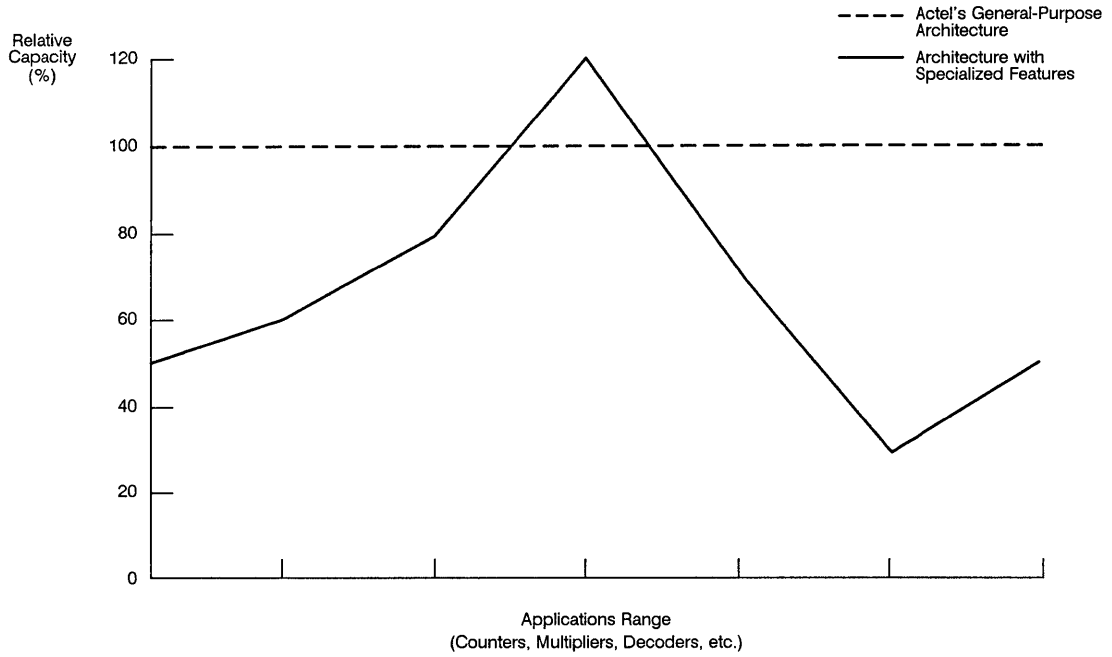


Figure 3. Actel's General-Purpose Architecture Addresses All Applications

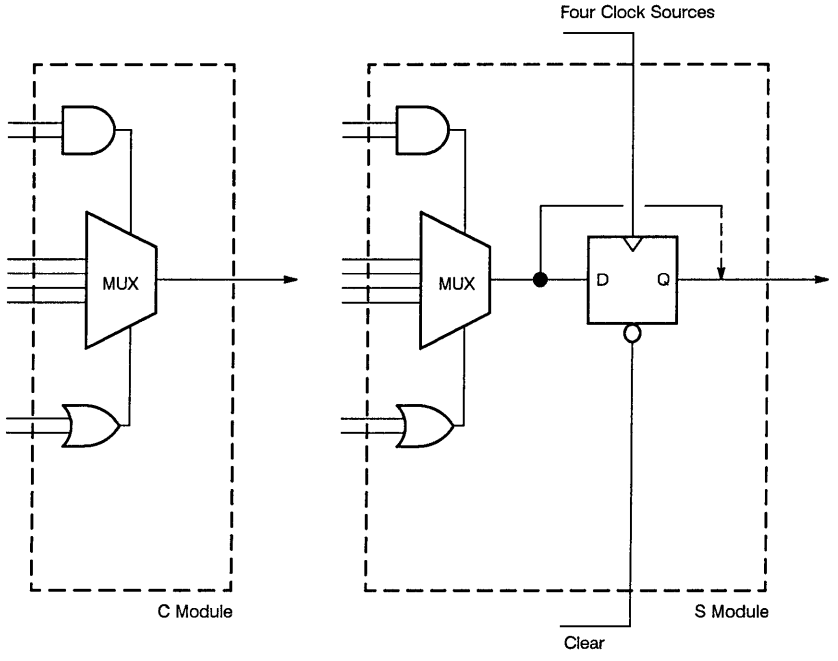


Figure 4. Logic Modules Use Identical Combinatorial Logic

Interconnect Routing Using the PLICE Antifuse

Interconnections between logic modules are made using the PLICE antifuse. The interconnections use a segmented wiring channel similar to channeled gate arrays. The horizontal and vertical channel segments vary in length, and are tuned to allow automatic place and route of the most interconnect-intensive applications. All speed-critical module-to-module connections are accomplished with only two low-resistance antifuse elements. Most connections are implemented in either two or three antifuse elements. No connections require more than four antifuse elements in a path.

I/O Module

The ACT 3 I/O module is a significant enhancement over the ACT 2 latch-based I/O module. The ACT 3 I/O module contains input and output registers and a register hold function that allows selective updating of the I/O module register. Thus, the register can be used for more complex logic functions in addition to simple timing functions. In particular, microprocessor based systems will benefit from the selective update capability of the ACT 3 I/O module. A variety of feedback options on the I/O module allow registered outputs, registered inputs, or direct inputs to be selected as input to the array. Each I/O module contains a slew control feature, which allows output rise and fall times to be tailored to the particular application. The block diagram for the ACT 3 I/O module is shown in Figure 5.

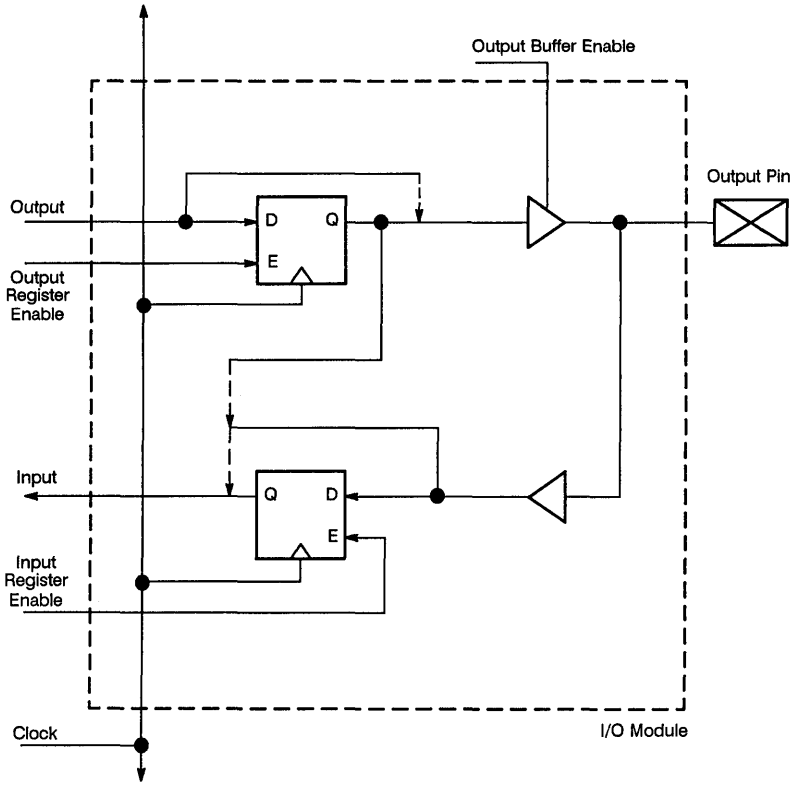


Figure 5. I/O Module with Registered Inputs and Outputs

Clocking Options

The ACT 3 family provides four clock distribution networks, twice the networks offered by the ACT 2 family. In addition to two routed clocks, ACT 3 provides two dedicated clocking sources: one for the array and one for the I/O module. The routed clocks are compatible with the ACT 2 family and are optimized for light to medium loaded clocking nets. They can also be used for special high fanout nets, such as reset or enable. The dedicated clock networks are optimized for high fanout nets in either the array or the I/O module. Since these clocks are dedicated, no special circuitry is required to route the clock signals. This results in a very controlled, high-speed clocking network for the large fanout portion of the design. The high-speed clock-to-output capability of the ACT 3 family is a direct result of the dedicated clock in the I/O module.

Programmable I/O Pins

Each I/O pin is available as an input, output, three-state, or bidirectional buffer. Inputs are TTL and CMOS compatible. Output drive levels meet 12 mA TTL and 6 mA HCT standards.

Designing with ACT 3

Design Methodology

The simple, highly regular logic module architecture of the ACT 3 family is ideal for synthesis optimization. The ALS design environment supports a wide variety of popular design approaches for schematic entry and synthesis. Synthesis libraries for top-down design also are available. Boolean entry and state machine design are supported with the ALES™ logic optimizer tool. In addition, ALS software provides 100 percent automatic placement and routing at up to 95 percent module utilization.

Hard and Soft Macros

Designing within the Actel design environment is accomplished through a building block approach. Over 250 logic function macros are provided in the ACT 3 design libraries. Hard macros range from simple SSI gates such as AND, NOR, and exclusive OR to more complex functions such as flip-flops with 4:1 multiplexed data inputs. Hard macros are implemented within the ACT 3 architecture by utilizing one or more C-Modules and/or S-Modules. Over 150 of these macros are implemented within a single logic module, although several two-module macros are available. One- and two-module macros have a small propagation delay variance, which allows accurate performance prediction.

Soft macros comprise multiple hard macros connected to form complex functions ranging from MSI functions to 16-bit counters and accumulators. A large number of TTL equivalent hard and soft macros also are provided.

Design Compatibility

The design libraries for ACT 3 are fully upward compatible from the ACT 1 and ACT 2 design libraries. ACT 1 and ACT 2 designs can be converted to equivalent gate-count ACT 3 arrays. The Activator®2 programmer supports the ACT 3 family; this single programming unit also supports ACT 1 and ACT 2 device families.

Reliability

Actel builds the most reliable FPGAs in the industry, with overall reliability ratings of less than 10 Failures-In-Time (FITs), corresponding to a useful life of more than 40 years. Actel FPGAs have been production-proven, with over 1 million devices shipped and over 130 billion antifuses manufactured. Actel devices are fully tested prior to shipment, with an outgoing defect level of only 122 ppm.

ACT™ 1 and ACT 2 Military Field Programmable Gate Arrays

ACT 1 Features

- Up to 2000 Gate Array Gates (6000 PLD/LCA™ equivalent gates)
- Replaces up to 53 TTL Packages
- Replaces up to 17 20-Pin PAL Packages
- Design Library with over 250 Macros
- Single Logic Module Architecture
- Up to 547 Logic Modules
- Up to 273 Flip-Flops
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Built-In High-Speed Clock Distribution Network
- I/O Drive to 4 mA
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment

ACT 2 Features

- Up to 8000 Gate Array Gates (20,000 PLD/LCA™ equivalent gates)
- Replace up to 210 TTL Packages
- Replace up to 69 20-Pin PAL Packages
- Design Library with over 250 Macros
- Single-Module Sequential Functions
- Wide-Input Combinatorial Functions
- Up to 1232 Programmable Logic Modules
- Up to 998 Flip-Flops
- 16-Bit Counter Performance to 50 MHz (MIL Temp)
- 16-Bit Accumulator Performance to 25 MHz (MIL Temp)
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Two High-Speed, Low-Skew Clock Networks
- I/O Drive to 6 mA
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment

1

Product Family Profile

Family	ACT 2		ACT 1	
Device	**A1280**	**A1240**	**A1020A**	**A1010A**
Capacity				
Gate Array Equivalent Gates	8,000	4,000	2,000	1,200
PLD/LCA Equivalent Gates	20,000	10,000	6,000	3,000
TTL Equivalent Packages	210	105	53	34
20-Pin PAL Equivalent Packages	69	34	17	12
Logic Modules	1,232	684	547	295
S-Modules	624	348		
C-Modules	608	336		
Flip-Flops (maximum)	998	565	273	147
Routing Resources				
Horizontal Tracks/Channel	36	36	22	22
Vertical Tracks/Column	15	15	13	13
PLICE® Antifuse Elements	750,000	400,000		
User I/Os (maximum)	140	104	69	57
Packages[1]	176 CPGA 172 CQFP	132 CPGA	84 CPGA 84 CQFP 44/68/84 JQCC	84 CPGA
Performance (MIL Temp)				
16-Bit Counters	39 MHz	50 MHz	39 MHz[2]	39 MHz[2]
16-Bit Accumulators	23 MHz	25 MHz	20 MHz[2]	20 MHz[2]
CMOS Process	1.2 µm	1.2 µm	1.2 µm	1.2 µm

Note:

1. See product plan on page 1-130 for package availability.
2. Performance is based on a -1 speed graded device at worst-case military operating conditions.

High Reliability, Low Risk Solution

Actel builds the most reliable field programmable gate arrays (FPGAs) in the industry, with overall antifuse reliability ratings of less than 10 Failures-In-Time (FITs), corresponding to a useful life of more than 40 years. Actel FPGAs have been production-proven, with over one million devices shipped and over 130 billion antifuses manufactured. Actel devices are fully tested prior to shipment, with an outgoing defect level of only 122 ppm. (Further reliability data is available in the "Actel Reliability Report.")

100% Tested Product

Device functionality is fully tested before shipment and during device programming. Routing tracks, logic modules, and programming, debug, and test circuits are 100% tested before shipment. Antifuse integrity also is tested before shipment. Programming algorithms are tested when a device is programmed using Actel's Activator 1 or 2® programming stations.

Benefits

No cost risk — Once you have an Action Logic™ System (ALS), Actel's CAE software and programming package, you can produce as many chips as you like for just the cost of the device itself, with no NRE charges to eat up your development budget each time you want to try out a new design.

No time risk — After entering your design, placement and routing is automatic, and programming the device takes only about 5 to 15 minutes for an average design. You save time in the design entry process by using tools that are familiar to you. The Action Logic System software interfaces to popular CAE software such as Mentor Graphics®, Valid™, OrCAD™, HP DCS, and Viewlogic® and runs on popular platforms such as Apollo®, HP, Sun™, and 386/486™ PC compatible machines.

No reliability risk — The PLICE™ antifuse is a one-time programmable, nonvolatile connection. Since Actel devices are permanently programmed, no downloading from EPROM or SRAM storage is required. Inadvertent erasure is impossible and there is no need to reload the program after power disruptions. Both the PLICE antifuse and the base process are radiation tolerant. Fabrication using a low-power CMOS process means cooler junction temperatures. Actel's non-PLD architecture delivers lower dynamic operating current. Our reliability tests show a very low failure rate of 91 FITs at 90 °C junction temperature with no degradation in AC performance. Special stress testing at wafer test eliminates infant mortalities prior to packaging.

No security risk — Reverse engineering of programmed Actel devices from optical or electrical data is extremely difficult. Programmed antifuses cannot be identified from a photograph or by using a SEM. The antifuse map cannot be deciphered either electrically or by microprobing. Each device has a silicon signature that identifies its origins, down to the wafer lot and fabrication facility.

No testing risk — Unprogrammed Actel parts are fully tested at the factory. This includes the logic modules, interconnect tracks, and I/Os. AC performance is assured by special speed path tests, and programming circuitry is verified on test antifuses. During the programming process, an algorithm is run to assure that all antifuses are correctly programmed. In addition, Actel's Actionprobe™ diagnostic tools allow 100% observability of all internal nodes to check and debug your design.

ACT 1 Description

The ACT 1 family of FPGAs offers a variety of package, speed, and application combinations. Devices are implemented in silicon gate, 1.2-micron two-level metal CMOS, and they employ Actel's PLICE antifuse technology. The unique architecture offers gate array flexibility, high performance, and instant turnaround through user programming. Device utilization is typically 95% of available logic modules.

ACT 1 devices also provide system designers with unique on-chip diagnostic probe capabilities, allowing convenient testing and debugging. Additional features include an on-chip clock driver with a hardwired distribution network. The network provides efficient clock distribution with minimum skew.

The user-definable I/Os are capable of driving at both TTL and CMOS drive levels. Available packages include ceramic J-leaded chip carriers, ceramic quad flatpack, and ceramic pin grid array.

A security fuse may be programmed to disable all further programming and to protect the design from being copied or reverse engineered.

ACT 2 Description

The ACT 2 family represents Actel's second generation of FPGAs. The ACT 2 family presents a two-module architecture consisting of C-Modules and S-Modules. These modules are optimized for both combinatorial and sequential designs (see Figure 1). Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining upward compatibility with the ACT 1 design environment. The devices are implemented in silicon gate, 1.2-µm, two-level metal CMOS, and employ Actel's PLICE antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance, and fast time-to-production through user programming.

The ACT 2 family is supported by the ALS, which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and debug and diagnostic probe capabilities. The Action Logic System is supported on the following platforms: 386/486 PC, Sun, HP and Apollo workstations. It provides CAE interfaces to the following design environments: Valid, Viewlogic, Mentor Graphics, HP DCS and OrCAD.

ACT 1 Architecture

ACT 1 devices consist of a matrix of logic modules arranged in rows separated by wiring channels. This array is surrounded by a ring of peripheral circuits including I/O buffers, testability circuits, and diagnostic probe circuits providing real-time diagnostic capability. Between rows of logic modules are routing channels containing sets of segmented metal tracks with PLICE antifuses. Each channel has 22 signal tracks. Vertical routing is permitted via 13 vertical tracks per logic module column. The resulting network allows arbitrary and flexible interconnections between logic modules and I/O modules.

The ACT 1 Logic Module

The ACT 1 logic module is an 8-input, one-output logic circuit chosen for the wide range of functions it implements and for its efficient use of interconnect routing resources (Figure 1).

The logic module can implement the four basic logic functions (NAND, AND, OR, and NOR) in gates of two, three, or four inputs. Each function may have many versions, with different combinations of active-low inputs. The logic module can also implement a variety of D-latches, exclusivity function, AND-ORs, and OR-ANDs. No dedicated hardwired latches or flip-flops are required in the array since latches and flip-flops may be constructed from logic modules wherever needed in the application.

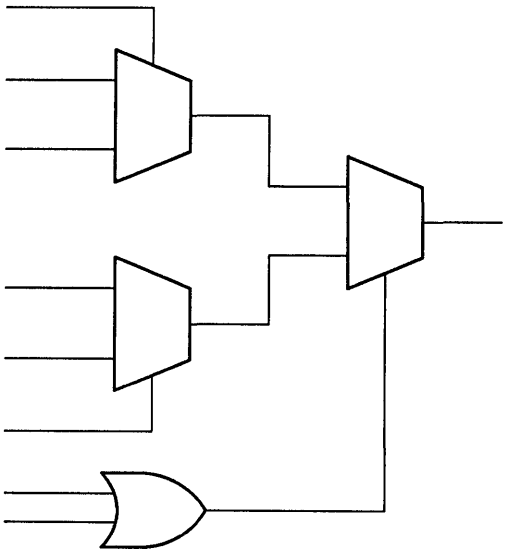


Figure 1. ACT 1 Logic Module

Programmable I/O Pins

Each I/O pin can be configured as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Outputs sink or source 4 mA at TTL levels. See Electrical Specifications for additional I/O buffer specifications.

Probe Pin

ACT 1 devices have two independent diagnostic probe pins. These pins allow the user to observe any two internal signals by entering the appropriate net name in the diagnostic software. Signals may be viewed on a logic analyzer using Actel's Actionprobe diagnostic tools. The probe pins can also be used as user-defined I/Os when debugging is finished.

ACT 2 Architecture

This section of the datasheet is meant to familiarize the user with the architecture of ACT 2 family devices. A generic description of the family will first be presented, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. Diagrams for the A1280 and A1240 are provided at the end of the datasheet. The additional circuitry required to program and test the devices will not be covered.

Array Topology

The ACT 2 family architecture is composed of five key elements or building blocks: Logic modules, I/O modules, Routing Tracks, Global Clock Networks, and Probe Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os.

Table 1. Array Sizes

Device	Rows	Columns	Logic	I/O
A1280	18	82	1232	140
A1240	14	62	684	104

The Logic and I/O modules are arranged in a two-dimensional array (Figure 2). There are three types of modules: Logic, I/O, and Bin. Logic and I/O modules are available as user resources. Bin modules are used during testing and are not available to users.

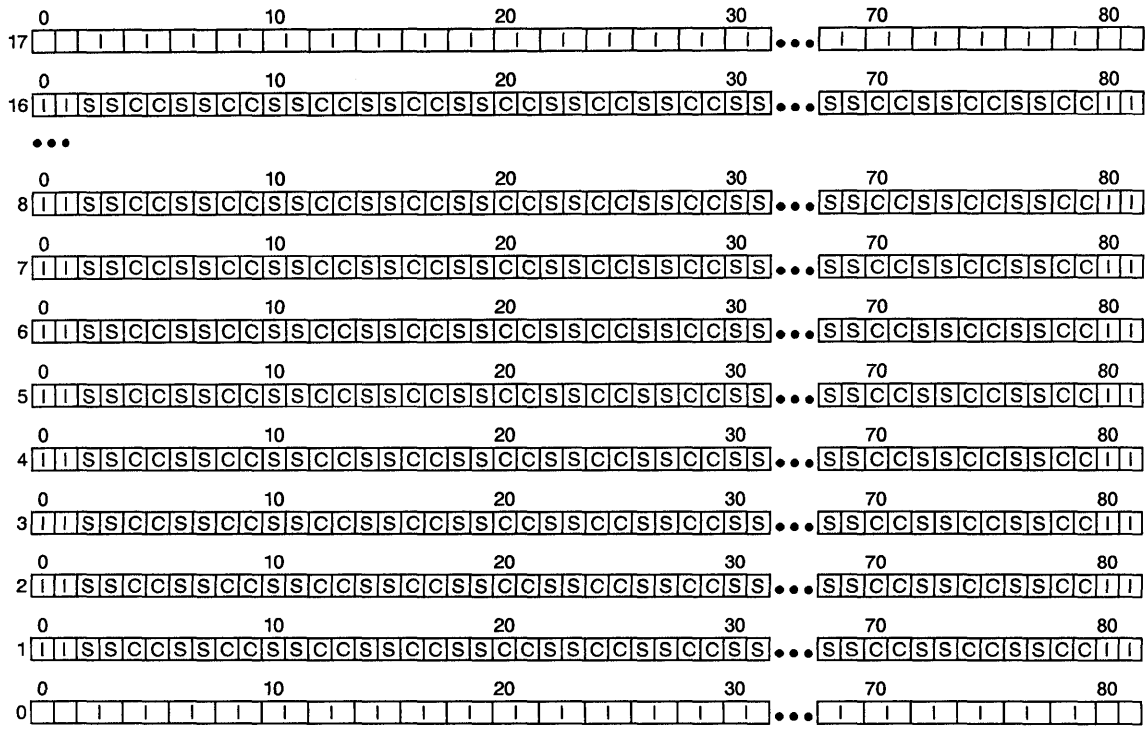


Figure 2. Actel 1280 Simplified Floor Plan

Logic Modules

Logic modules are classified into two types: combinatorial C-modules and sequential S-modules (see Figures 3 and 4). The C-module is an enhanced version of the Act 1 family logic module optimized to implement high fan-in combinatorial macros, such as 5-input AND, 5-input OR, etc. The S-module is designed to implement high speed flip-flop functions within a single module. S-modules also include combinatorial logic, which allows an additional level of logic to be implemented without additional propagation delay. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating pairs (shown in Figure 2) and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). I/O-modules are arranged around the periphery of the array.

The combinatorial module (shown in Figure 3) implements the following function:

Z = !S1 * (D00 * !S0 + D01 * S0) + S1 * (D10 * !S0 + D11 * S0)

where:

S0 = A0 * B0
S1 = A1 + B1

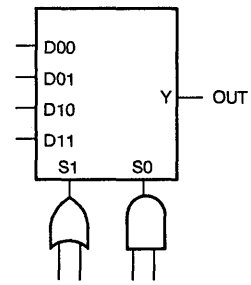


Figure 3. C-Module Implementation

The sequential module implements this same function Z, followed by a sequential block. The sequential block can be configured to implement either a D-type flip-flop or transparent latch. It can also be fully transparent so that S-modules can be used to implement purely combinatorial functions. The function of the sequential module is determined by the macro selection from the design library of hard macros. Allowable S-module implementations are shown in Figure 4.

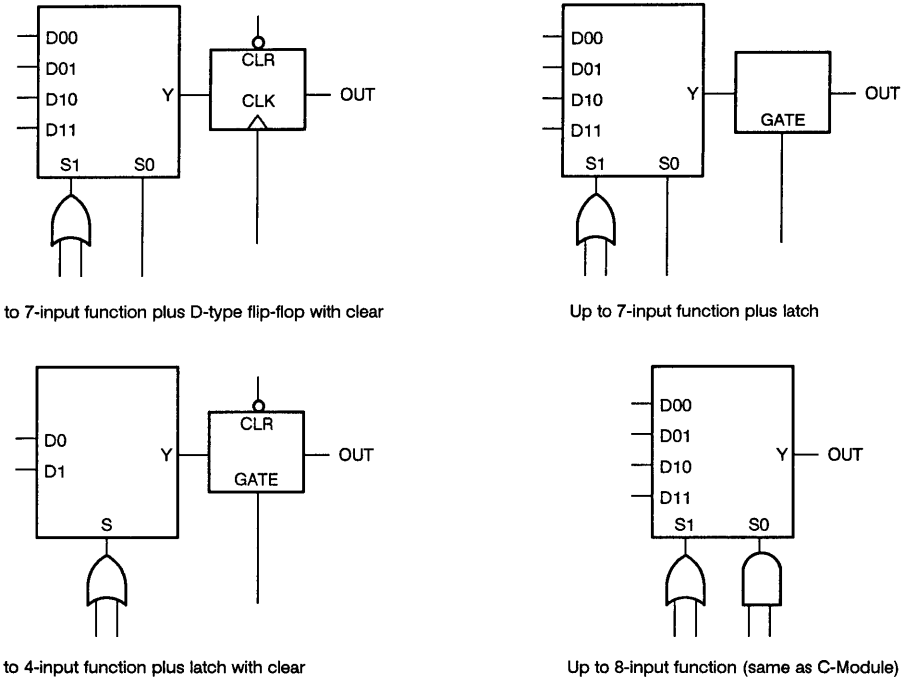


Figure 4. S-Module Implementations

I/Os

The I/O architecture consists of pad drivers located near the bonding pads and I/O modules located in the array. Top/bottom I/O modules are located in the top and bottom rows respectively. Side I/O modules occupy the leftmost two columns and the rightmost two columns of the array. The function of all I/O modules is identical, but the top/bottom I/O modules have a different routing interface to the array than the side I/O modules. I/Os implement a variety of user functions determined by library macro selection.

Special Purpose I/Os

Certain I/O pads are temporarily used for programming and testing the device. During normal user operation, these special I/O pads are identical to other I/O pads. The following special I/O pads and their functions are shown in Table 2.

Table 2. Special I/O Pads

SDI	Serial Data In
SDIO	Serial Data Out
BININ	Binning Circuit In
BINOUT	Binning Circuit Out
DCLK	Serial Data Clock In
PRA	Probe A Output
PRB	Probe B Output

Two other pads, CLKA and CLKB, also differ from normal I/Os in that they can be used to drive the global clock networks. Power, Ground, and Programming pads are not considered I/O functions. Their function is summarized as follows:

VCCA, VCCQ, VCCI	Power
GNDA, GNDQ, GNDI	Circuit Ground
VSV, VKS	Programming Pads
MODE	Program/Debug Control

I/O Pads

I/O pads are located on the periphery of the die and consist of the bonding pad, the high-drive CMOS drivers, and the TTL level-shifter inputs. Each I/O pad is associated with a specific I/O module. Connections form the I/O pad to the I/O module are made using the signals DATAOUT, DATAIN and EN (shown in Figure 5).

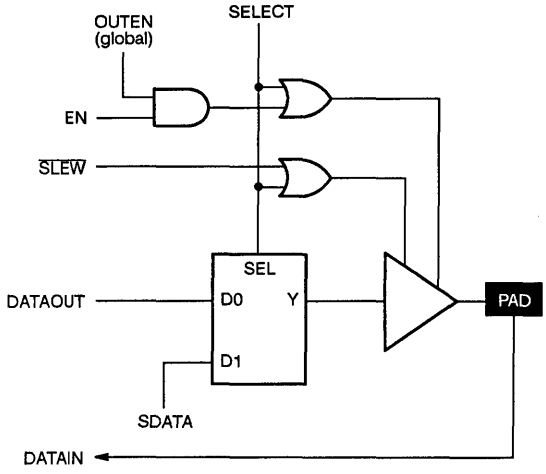


Figure 5. I/O Pad Signals

I/O Modules

There are two types of I/O modules: side and top/bottom. The I/O module schematic is shown in Figure 6. In the side I/O modules, there are two inputs supplying the data to be output from the chip: UO1 and UO2. (UO stands for user output). Two are used so that the router can choose to take the signal from either the routing channel above or the routing channel below the I/O module. The top/bottom I/O modules interact with only one channel and therefore have only one UO input.

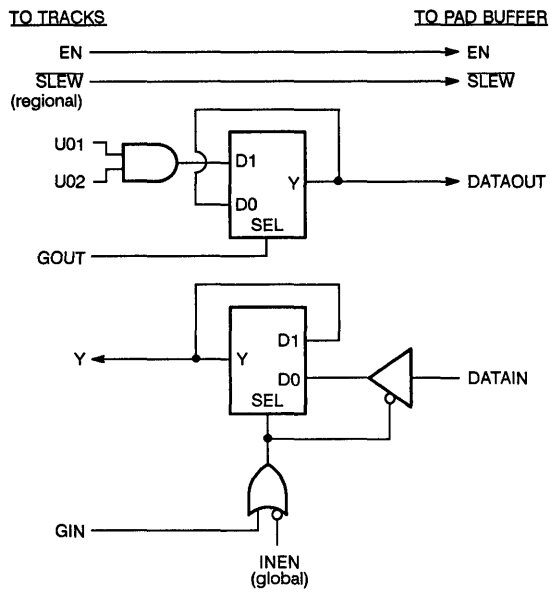


Figure 6. I/O Module

The EN input enables the tristate output buffer. The global signals INEN and OUTEN (Figure 5) are used to disable the inputs and outputs during certain test modes. Latches are provided in the input and output path. When GOUT is low, the output signal on UO1/UO2 is latched. When it is high, the latch is transparent. The latch can be used as the second stage of a rising-edge flip-flop as described in the Applications note accompanying this data sheet. GIN is the reverse of GOUT. When GIN is high, the input data is latched; when it is low, the input latch becomes transparent.

The output of the module, Y, is used for data being input to the chip. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below it (similar to logic modules). Side I/O modules may also connect to the array through nondedicated Long Vertical Tracks (LVTs). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom must be routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section). As a result, I/O signals connected to I/O modules on either the top or bottom of the array may incur a slight delay penalty (~1nS) over signals connected to I/O modules on the sides.

Routing Structure

The ACT 2 architecture uses Vertical and Horizontal routing tracks to interconnect the various Logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into pieces called segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 7. Nondedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

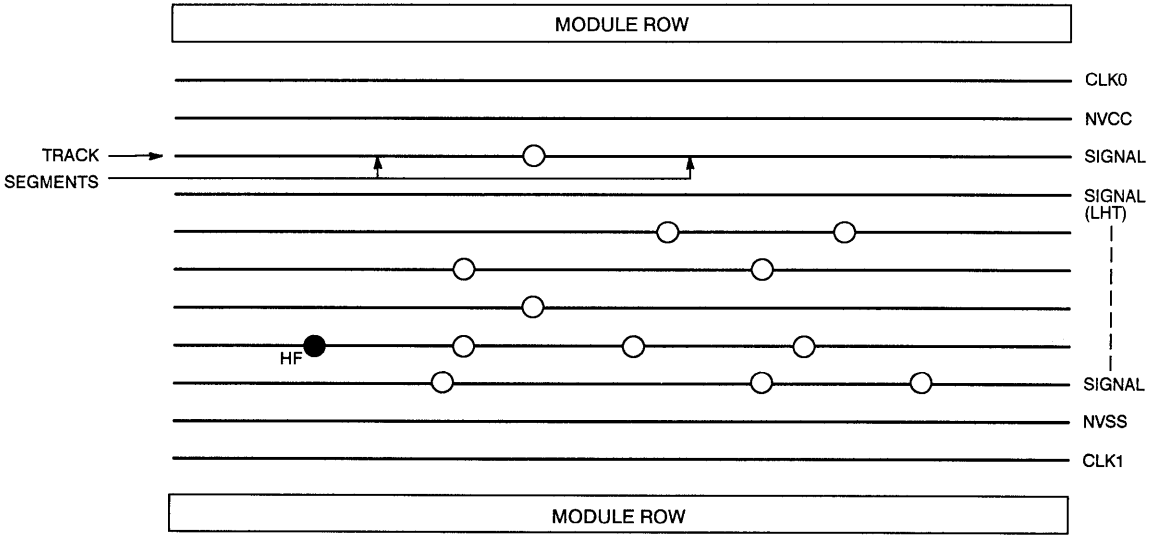


Figure 7. Horizontal Routing Tracks and Segments

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 8.

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PAL®s. The use of antifuses to implement a Programmable Logic Device results in highly testable structures as well as efficient programming algorithms. The structure is highly testable because there are no pre-existing connections, therefore temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Antifuse Structures

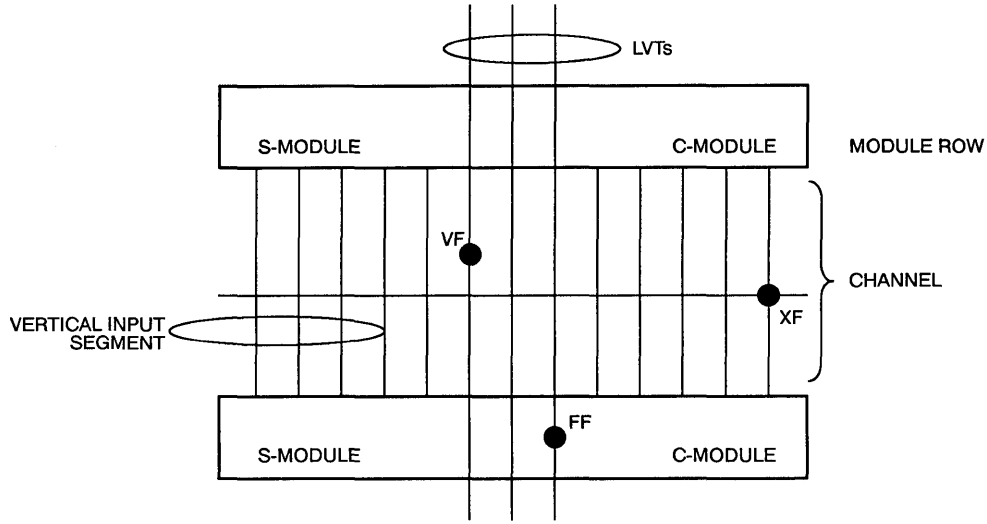


Figure 8. Vertical Routing Tracks and Segments

Antifuse Connections

Four types of antifuse connections are used in the routing structure of the Act 2 array. (The physical structure of the antifuse is identical in each case, only the usage differs.) The four types are:

XF	Cross connected antifuse	Most intersections of horizontal and vertical tracks have an XF that connects the perpendicular tracks.
HF	Horizontally connected antifuse	Adjacent segments in the same horizontal track are connected end-to-end by an HF.
VF	Vertically connected antifuse	Some long vertical tracks are divided into two segments. Adjacent long segments are connected end-to-end by a VF.
FF	"Fast-Fuse" antifuse	The FF connects a module output directly to a long vertical track.

Examples of all four antifuse connections are shown in Figures 7 and 8.

Antifuse Programming

The ACT 2 family uses the PLICE antifuse developed by Actel. The PLICE element is programmed by placing a high voltage (~20 V) across the element and supplying current (~5 mA) for a short duration (< 1mS). In the ACT 2 architecture, most antifuses are programmed to ~500 ohms resistance, except for the F-fuses which are programmed to ~250 ohms. The programming circuits are transparent to the user.

Clock Networks

Two low-skew, high fan-out clock distribution networks are provided in the Act 2 architecture (Figure 9). These networks are referred to as CLK0 and CLK1. Each network has a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows:

1. externally from the CLKA pad
2. externally from the CLKB pad
3. internally from the CLKINA input
4. internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

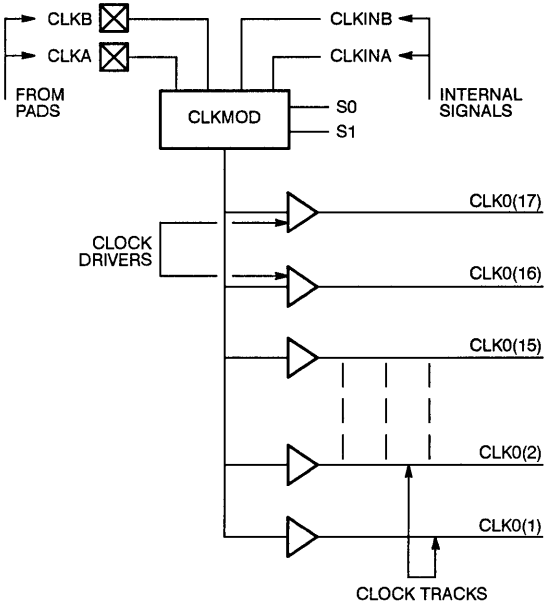


Figure 9. Clock Networks

The user configures the clock module by selecting one of two clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used.

The clock input pads may also be used as normal I/Os, by-passing the clock networks.

Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

Vertical tracks span the vertical height of the array. The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive (off), which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active (on) to verify the continuity of the metal tracks. Vertical input segments span only one channel. Inputs to the array modules come either from the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below (Figure 10).

Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 10, so that only four vertical tracks are required.

LVT Connections

Outputs may also connect to nondedicated segments, (LVTs). Each module pair in the array shares three LVTs that span the length of column as shown in Figure 9. Any module in the column pair can connect to one of the LVTs in the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, by-passing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

Antifuse Connections

In general every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

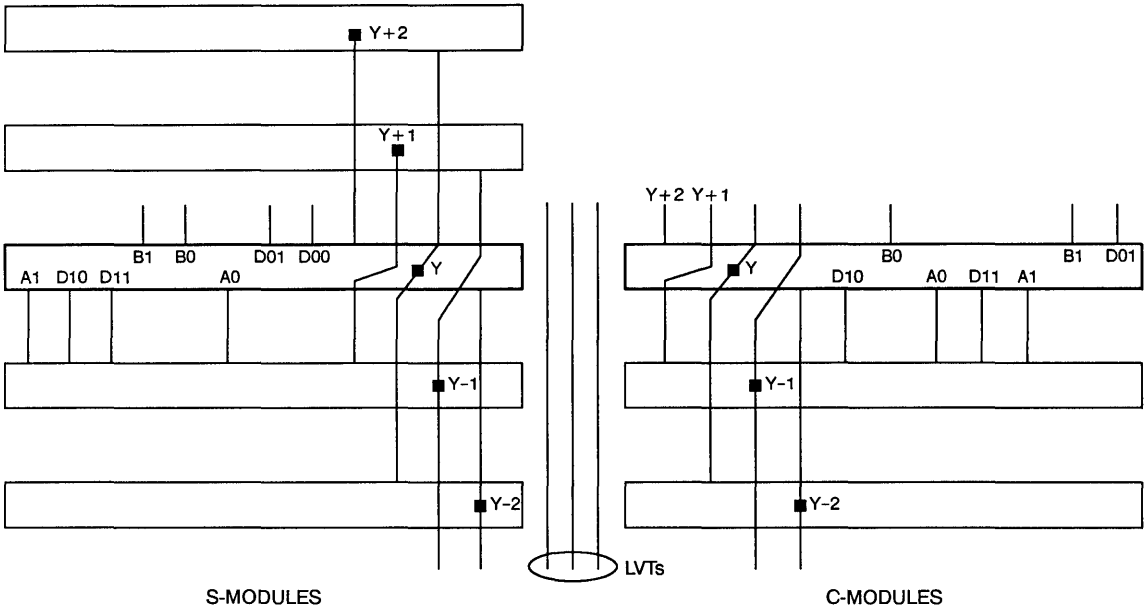


Figure 10. Logic Module Routing Interface

Clock Connections

To minimize loading on the clock networks, only a subset of inputs has fuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-Module. Both of these are illustrated in Figure 11.

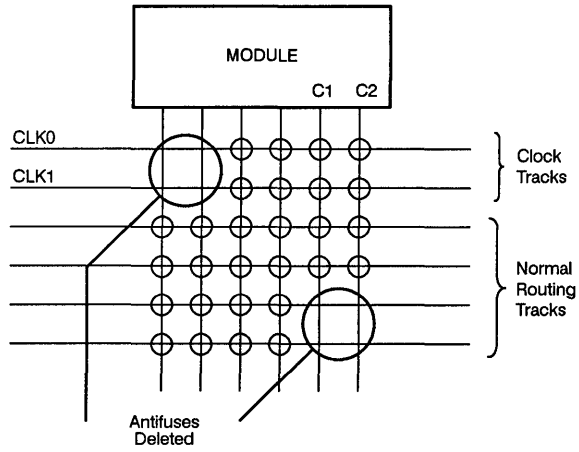


Figure 11.

Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the external pins: MODE, SDI, and DCLK. The function of these pins is summarized below. When MODE is low (GND), the device is in normal or user mode. When MODE is high (VCC), the device is placed into one of several programming or test states. The SDI pin (when MODE is high) is used to input serial data to the Mode register and various address registers surrounding the array. Data is clocked into these registers using the DCLK pin. The registers are connected as a long series of shift registers as shown in Figure 12. The Mode register determines the test or programming state of the device. Many of the test modes are used during wafer sort and final test at the factory. Other test modes are used during programming in the Activator 2, and some of the modes are available only after programming. The Actionprobe function is one such function available to users.

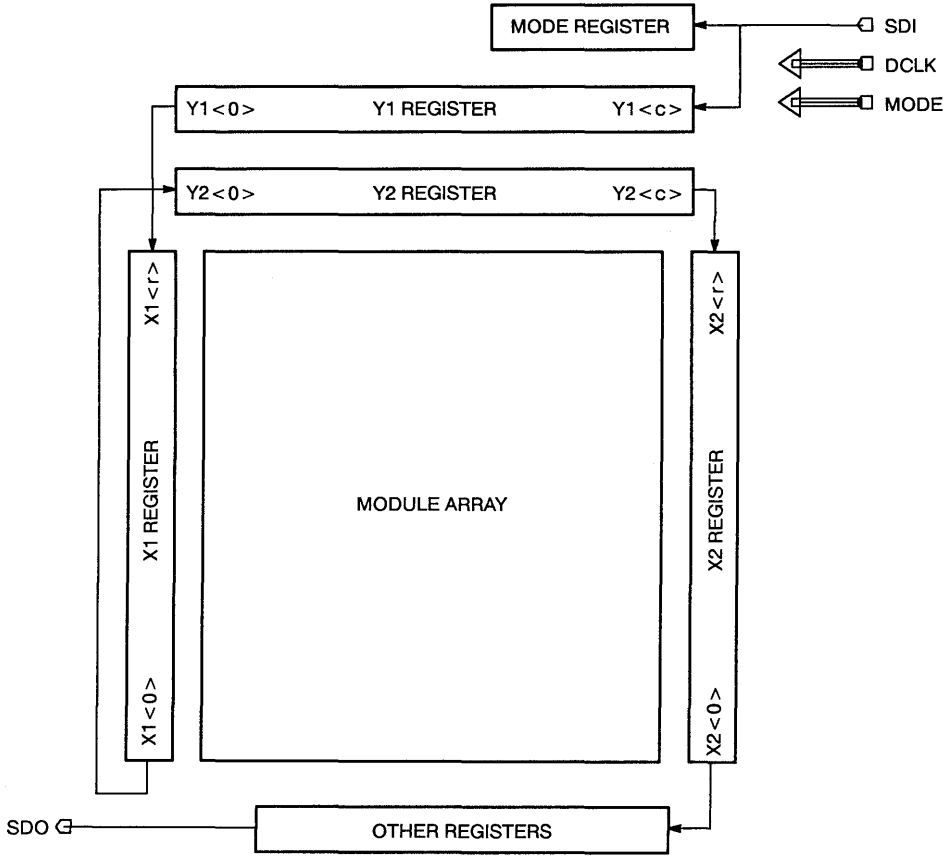


Figure 12. ACT 2 Shift Register

Actionprobe

If a device has been successfully programmed and the security fuse has not been programmed, any internal logic or I/O module output can be observed using the Actionprobe circuitry and the PRA and/or PRB pins. The Actionprobe Diagnostic system provides the software and hardware required to perform real-time debugging. The software automatically performs the following functions.

A pattern of "1s" and "0s" is shifted into the device from the SDI pin at each positive edge transition of DCLK. The complete sequence contains 10 bits of counter, 21 bits of Mode Register, n bits of zeros (filler of unused fields, where n depends on the particular device type), R bits of X2, C bits of Y2, R bits of X1, C bits of Y1, and a stop bit ("0" or "1"). After the stop bit has been shifted in, DCLK is left high (see definitions below). X1 and Y1 represent the (X,Y) location in the array for the Actionprobe output, PRA.

X2 and Y2 represent the (X,Y) location in the array for the Actionprobe output, PRB. R and C are the row and column size as defined in Table 1. The filler bits, counter pattern, and Mode register pattern are shown in Table 3. Addressing for rows and columns is active high, i.e. unselected rows and columns are "zeros" and the selected row and column is "high." The timing sequence is shown in Figure 13. The recommended frequency is 10 MHz with 10 nS setup and hold times allowing for SDI and DCLK transitions. The selected module output will be present at the PRA or PRB output approximately 20 nS after the stop-bit transition.

Table 3. Bit Stream Definitions for Actionprobe Diagnostics

Device	Probe_Mode	Filler (n)	Counter_Pattern	Mode_Register_Pattern	# of clocks
A1280	Probe A only	443	0011011111	000000110001111100000	675
A1280	Probe B only	443	0011011111	000000101001111100000	675
A1280	Probe A and B	443	0011011111	000000111001111100000	675
A1240	Probe A only	361	1111000001	000000110001111100000	541
A1240	Probe B only	361	1111000001	000000101001111100000	541
A1240	Probe A and B	361	1111000001	000000111001111100000	541
A1225	Probe A only	308	1101011010	000000110001111100000	458
A1225	Probe B only	308	1101011010	000000101001111100000	458
A1225	Probe A and B	308	1101011010	000000111001111100000	458

For Example: Selecting PRA for A1280 results in the following bit stream:

0011011111_000000110001111100000_
(443 zeros)_X2<0>...X2<17>_Y2<81>...Y2<0>_X1<0>...X1<0>...X1<17>_Y1<0>...Y1<81>_0,

where "_" is used for clarity only.

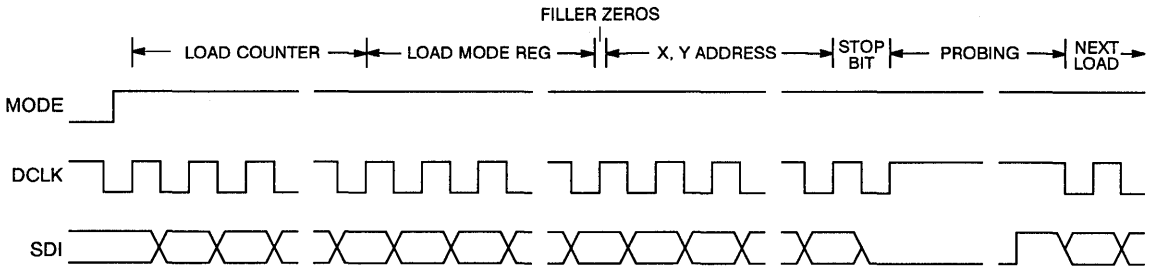
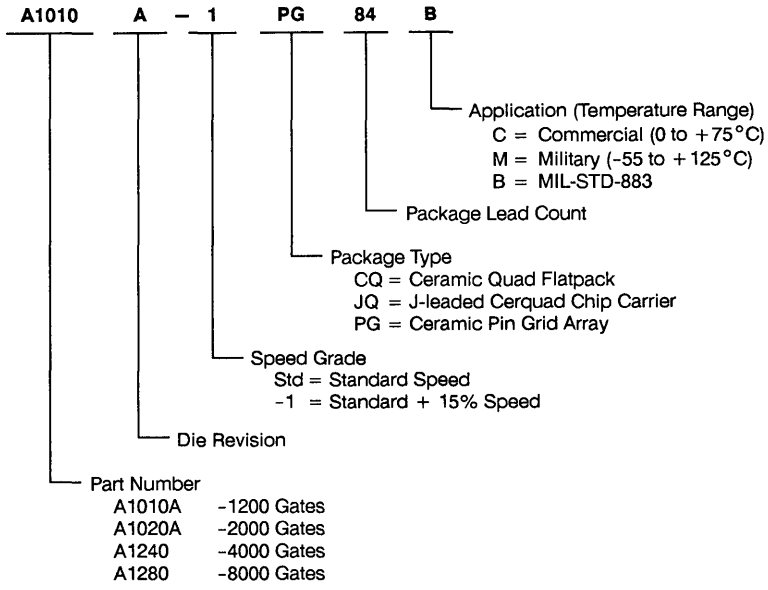


Figure 13. Timing Waveforms

Military Device Ordering Information



1

SMD Drawing Number to Actel Part Number Cross Reference

SMD Number	Cage Number	Actel Part Number
5962-9096401MZX	0J4Z0	A1010A-PG84B
5962-9096501MXX	0J4Z0	A1020A-JQ44B
5962-9096501MYX	0J4Z0	A1020A-JQ68B
5962-9096501MZX	0J4Z0	A1020A-JQ84B
5962-9096501MUX	0J4Z0	A1020A-PG84B
5962-9096501MTX	0J4Z0	A1020A-CQ84B

Product Plan

	Speed Grade		Application			
	Std	-1*	C	M	B	E
A1280 Device						
176-pin Ceramic Pin Grid Array (PG)	✓	P	✓	✓	✓	–
172-pin Ceramic Quad Flatpack (CQ)	✓	P	✓	✓	✓	✓
A1240 Device						
132-pin Ceramic Pin Grid Array (PG)	✓	P	✓	✓	✓	–
A1020A Device						
84-pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	✓	–
84-pin Ceramic Quad Flatpack (CQ)	✓	✓	✓	✓	✓	✓
84-pin J-leaded Cerquad Chip Carrier (JQ)	✓	✓	✓	✓	✓	–
68-pin J-leaded Cerquad Chip Carrier (JQ)	✓	✓	✓	✓	✓	–
44-pin J-leaded Cerquad Chip Carrier (JQ)	✓	✓	✓	✓	✓	–
A1010A Device						
84-pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	✓	–

Applications: C = Commercial, M = Military, B = MIL-STD-883C, E = Extended Flow

Availability: ✓ = Available, P = Planned, – = Not Planned

* Speed Grade: -1 = 15% faster than Standard

Device Resources

			User I/Os							
			CPGA			CQFP		JQCC		
Device	Logic Modules	Gates	176-pin	132-pin	84-pin	172-pin	84-pin	84-pin	68-pin	44-pin
A1280	1232	8000	140	–	–	140	–	–	–	–
A1240	684	4000	–	104	–	–	–	–	–	–
A1020A	547	2000	–	–	69	–	69	69	57	34
A1020A	295	1200	–	–	57	–	–	–	–	–

Pin Description

CLKA Clock A (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground (Input)

Input LOW supply voltage.

I/O Input/Output (Input, Output)

I/O pins function as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

MODE Mode (Input)

The MODE pin controls the use of multi-function pins (DCLK, PRA, PRB, SDI, SDO). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os.

NC No Connection

This pin is not connected to circuitry within the device.

PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDO Serial Data Output (Output)

Serial data output for diagnostic probe. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} Supply Voltage (Input)

Input HIGH supply voltage.

V_{KS} Programming Voltage (Input)

Input supply voltage used for device programming. This pin must be connected to GND during normal operation.

V_{PP} Programming Voltage (Input)

Input supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

V_{SV} Programming Voltage (Input)

Input supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

Actel Military Product Flow

Step	Screen	883C—Class B 883C Method	883C—Class B Requirement	Military Datasheet Requirement
1.0	Internal Visual	2010, Test Condition B	100%	100%
2.0	Temperature Cycling	1010, Test Condition C	100%	100%
3.0	Constant Acceleration	2001, Test Condition E (min), Y1, Orientation only	100%	100%
4.0	Seal	1014		
	a. Fine		100%	100%
	b. Gross		100%	100%
5.0	Visual Inspection		100%	100%
6.0	Pre Burn-in Electrical Parameters	In accordance with Actel applicable device specifications	100%	N/A
7.0	Burn-in Test	1015 Condition D 160 hours @ 125°C Min.	100%	N/A
8.0	Interim (post burn-in) Electrical Parameters	In accordance with Actel applicable device specifications	100%	100% (as final test)
9.0	Percent Defective Allowable	5%	All Lots	N/A
10.0	Final Electrical Test	In accordance with Actel applicable device specifications		
	a. Static Tests (1) 25°C (Subgroup 1, Table I, 5005) (2) -55°C and +125°C. (Subgroups 2, 3, Table I, 5005)		100%	100%
	b. Dynamic and Functional Tests (1) 25°C (Subgroup 7, Table I, 5005) (2) -55°C and +125°C. (Subgroups 8A and 8B, Table I, 5005)		100%	100%
	c. Switching Tests at 25°C (Subgroup 9, Table I, 5005)		100%	100%
11.0	Qualification or Quality Conformance Inspection Test Sample Selection (Group A)	5005	All Lots	N/A
12.0	External Visual	2009	100%	Actel specification

Actel Extended Flow[1, 2]

	Screen	Method	Requirement
1.	Wafer Lot Acceptance[3]	5007 with step coverage waiver	All Lots
2.	Destructive In-Line Bond Pull[4]	2011, condition D	Sample
3.	Internal Visual	2010, condition A	100%
4.	Temperature Cycling	1010, condition C	100%
5.	Constant Acceleration	2001, condition E (min) Y_1 orientation only	100%
6.	Visual Inspection	2009	100%
7.	Particle Impact Noise Detection	2020, condition A	100%
8.	Serialization		100%
9.	Pre Burn-in Electrical Parameters	In accordance with Actel applicable device specification	100%
10.	Burn-in Test	1015, 240 hours @ 125°C minimum	100%
11.	Interim (Post Burn-in) Electrical Parameters	In accordance with Actel applicable device specification	100%
12.	Reverse Bias Burn-in	1015, condition A or C, 72 hours @ 150°C minimum	100%
13.	Interim (Post Burn-in) Electrical Parameters	In accordance with Actel applicable device specification	100%
14.	Percent Defective Allowable (PDA) Calculation	5%, 3% functional parameters @ 25°C	All Lots
15.	Final Electrical Test	In accordance with Actel applicable device specification	100%
	a. Static Tests		100%
	(1) 25°C (Subgroup 1, Table 1)	5005	
	(2) -55°C and 125°C (Subgroups 2, 3, Table 1)	5005	
	b. Dynamic or Functional Tests		100%
	(1) 25°C (Subgroup 4 or 7, Table 1)	5005	
	(2) -55°C and 125°C (Subgroups 5 and 6, or 8 a and b, Table 1)	5005	
	c. Switching Tests at 25°C (Subgroup 9, Table 1)	5005	100%
16.	Seal	1014	100%
	a. Fine		
	b. Gross		
17.	Radiographic	2012, two views	100%
18.	Qualification or Quality Conformance Inspection Test Sample Selection	5005	Per Group A
19.	External Visual	2009	100%

Notes:

1. Actel offers the Extended Flow in order to satisfy those customers that require additional screening beyond the requirements of MIL-STD-883C, Class B. Actel is compliant to the requirements of MIL-STD-883C, Paragraph 1.2.1, and MIL-M-38510 Appendix A. Actel is offering this extended flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883C Class S. The exceptions to Method 5004 are as shown in Notes 2–4 below.
2. Method 5004 requires 100% Radiation Latch-up testing to Method 1020. Actel will not be performing any radiation testing and this requirement must be waived in its entirety.
3. Wafer lot acceptance is performed to Method 5007, however the step coverage requirement as specified in Method 2018 must be waived.
4. Method 5004 requires a 100%, Non-Destructive Bond Pull to Method 2023. Actel substitutes a Non-Destructive Bond Pull to Method 2011, condition D on a sample basis only.

Absolute Maximum Ratings

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[1, 2, 3]	-0.5 to +7.0	Volts
V_I	Input Voltage	-0.5 to V_{CC} +0.5	Volts
V_O	Output Voltage	-0.5 to V_{CC} +0.5	Volts
I_{IK}	Input Clamp Current	±20	mA
I_{OK}	Output Clamp Current	±20	mA
I_{OK}	Continuous Output Current	±25	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Stresses beyond those listed above may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.

Notes:

1. $V_{PP} = V_{CC}$, except during device programming.
2. $V_{SV} = V_{CC}$, except during device programming.
3. V_{KS} = GEN, except during device programming.

Recommended Operating Conditions

Parameter	Commercial	Military	Units
Temperature Range[1]	0 to +70	-55 to +125	°C
Power Supply Tolerance	±5	±10	%V_{CC}

Note:

1. Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the maximum power dissipation for a CPGA 176-pin package at military temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. military temp. (°C)}}{\theta ja\ (°C/W)} = \frac{150°C - 125°C}{20\ °C/W} = 1.2\ W$$

Package Type	Pin Count	θjc	θja Still air	θja 300 ft/min.	Units
Ceramic Pin Grid Array	84	8	33	20	°C/W
	132	5	30	15	°C/W
	176	2	20	8	°C/W
Ceramic Quad Flatpack	84	5	40	30	°C/W
	172				
J-leaded Cerquad Chip Carrier	44	8	38	30	°C/W
	68	8	35	25	°C/W
	84	8	34	24	°C/W

ACT 1 Electrical Specifications

Parameter		Commercial		Military		Units
		Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = -4 mA)	3.84				V
	(I_{OH} = -3.2 mA)			3.7		V
V_{OL}[1]	(I_{OL} = 4 mA)			0.33	0.40	V
V_{IL}		-0.3	0.8	-0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500	ns
C_{IO} I/O Capacitance[2, 3]			10		10	pF
Standby Current, I_{CC}[4]			10		25	mA
Leakage Current[5]		-10	10	-10	10	µA
I_{OS} Output Short Circuit Current[6]	(V_O = V_{CC})	20	140	20	140	mA
	(V_O = GND)	-10	-100	-10	-100	mA

Notes:
1. Only one output tested at a time. V_{CC} = min.
2. Not tested, for information only.
3. Includes worst-case 84-pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.
4. Typical standby current = 3 mA. All outputs unloaded. All inputs = V_{CC} or GND.
5. V_O, V_{IN} = V_{CC} or GND.
6. Only one output tested at a time. Min. at V_{CC} = 4.5 V; Max. at V_{CC} = 5.5 V.

ACT 2 Electrical Specifications

Parameter		Commercial		Military		Units
		Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = -6 mA)	3.84				V
	(I_{OH} = -4 mA)			3.7		V
V_{OL}[1]	(I_{OL} = 6 mA)		0.33		0.40	
V_{IL}		-0.3	0.8	-0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500	ns
C_{IO} I/O Capacitance[2, 3]			10		10	pF
Standby Current, I_{CC}[4]			10		25	mA
Leakage Current[5]		-10	10	-10	10	µA

Notes:
1. Only one output tested at a time. V_{CC} = min.
2. Not tested, for information only.
3. Includes worst-case 176-pin CPGA package capacitance. V_{OUT} = 0 V, f = 1 MHz.
4. All outputs unloaded. All inputs = V_{CC} or GND.
5. V_O, V_{IN} = V_{CC} or GND.

ACT 1 Power Dissipation

The following formula is used to calculate total device dissipation.

Total Device Power (mW) = (0.20 x N x F1) + (0.085 x M x F2) + (0.80 x P x F3)

Where:

F1 = Average logic module switching rate in MHz

F2 = CLKBUF macro switching rate in MHz

F3 = Average I/O module switching rate in MHz

M = Number of Logic modules connected to the CLKBUF macro

N = Total number of Logic modules used in the design (including M)

P = Number of outputs loaded with 50 pF

Average switching rate of logic modules and of I/O modules is some fraction of the device operating frequency (usually CLKBUF). Logic modules and I/O modules switch states (from low-to-high or from high-to-low) only if the input data changes when the module is enabled. A conservative estimate for average logic module and I/O module switching rates (variables F1 and F3, respectively) is 10% of device clock driver frequency.

If the CLKBUF macro is not used in the design, eliminate the second term (including F2 and M variables) from the formula.

Sample A1020 Device Power Calculation

To illustrate the power calculation, consider a large design operating at high frequency. This sample design utilizes 85% of available logic modules on the A1020-series device (.85 x 547 = 465 logic modules used). The design contains 104 flip-flops (208 logic modules). Operating frequency of the design is 16 MHz. In this design, the CLKBUF macro drives the clock network. Logic modules and I/O modules are switching states at approximately 10% of the clock frequency rate (.10 x 16 MHz = 1.6 MHz). Sixteen outputs are loaded with 50 pF.

To summarize the design described above: N = 464; M = 208; F2 = 16; F1 = 4; F3 = 4; P = 16. Total device power can be calculated by substituting these values for variables in the device dissipation formula.

Total device power for this example =

(0.20 x 465 x 1.6) + (0.085 x 208 x 16) + (0.80 x 16 x 1.6) = 452 mW

ACT 2 Power Dissipation

$P = [I_{CC} + I_{active}] \cdot V_{CC} + I_{OL} \cdot V_{OL} \cdot N + I_{OH} \cdot (V_{CC} - V_{OH}) \cdot M$

Where:

I_{CC} is the current flowing when no inputs or outputs are changing.

I_{active} is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power

Static power dissipation is typically a small component of the overall power. From the values provided in the Electrical Specifications, the maximum static power (commercial) dissipation is:

10 mA x 5.25 V = 52.5 mW

The static power dissipated by TTL loads depends on the number of outputs that drive high or low and the DC lead current flowing. Again, this number is typically small. For instance, a 32-bit bus driving TTL loads will generate 42 mW ATT with all outputs driving low or 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power

The active power component in CMOS devices is frequency dependent and depends on the user's logic and the external I/O. Active power dissipation results from charging internal chip capacitance such as that associated with the interconnect, unprogrammed antifuses, module inputs, and module outputs plus external capacitance due to PC board traces and load device inputs. An additional component of active power dissipation is due to totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1.

$$\text{Power } (\mu W) = C_{EQ} \cdot V_{CC}^2 \cdot f \quad (1)$$

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CC} is power supply in volts.

f is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{active} at a specified frequency and voltage for each circuit component of interest. The results for ACT 2 devices are:

	C_{EQ} (pF)
Modules	7.7
Input Buffers	18.0
Output Buffers	25.0
Clock Buffer Loads	2.5

To calculate the active power that is dissipated from the complete design, you must solve Equation 1 for each component. In order to do this, you must know the switching frequency of each part of the logic. The exact equation is a piece-wise linear summation over all components, as shown in Equation 2.

$$\text{Power} = [(m \cdot 7.7 \cdot f_1) + (n \cdot 18.0 \cdot f_2) + (p \cdot (25.0 + C_L) \cdot f_3) + (q \cdot 2.5 \cdot f)] \cdot V_{CC}^2 \quad (2)$$

Where:

n = Number of logic modules switching at frequency f_1

m = Number of input buffers switching at frequency f_2

p = Number of output buffers switching at frequency f_3

q = Number of clock loads on the global clock network

f = Frequency of global clock

f_1 = Average logic module switching rate in MHz

f_2 = Average input buffer switching rate in MHz

f_3 = Average output buffer switching rate in MHz

C_L = Output load capacitance

Determining Average Switching Frequency

In order to determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following rules will help you to determine average switching frequency in logic circuits. These rules are meant to represent worst-case scenarios so that they can be generally used for predicting the upper limits of power dissipation. These rules are as follows:

Module Utilization = 80% of combinatorial modules

Average Module Frequency = F/10

Inputs = 1/3 of I/O

Average Input Frequency = F/5

Outputs = 2/3 of I/Os

Average Output Frequency = F/10

Clock Net 1 Loading = 40% of sequential modules

Clock Net 1 Frequency = F

Clock Net 2 Loading = 40% of sequential modules

Clock Net 2 Frequency = F/2

Estimated Power

The results of estimating active power are displayed in Figure 14. The graphs provide a simple guideline for estimating power. The tables may be interpolated when your application has different resource utilizations or frequencies.

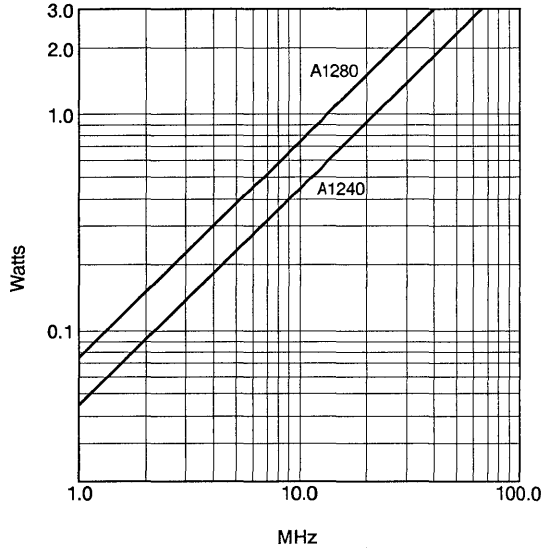
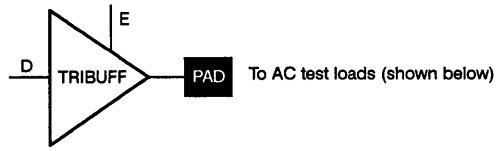
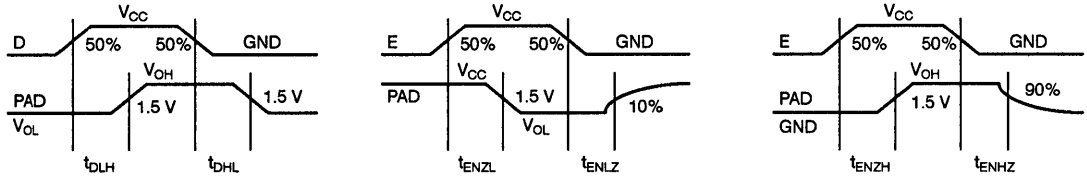


Figure 14. ACT 2 Power Estimates

Parameter Measurement

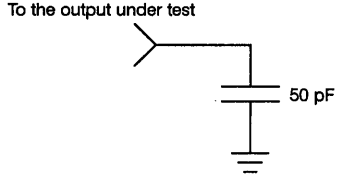
Output Buffer Delays



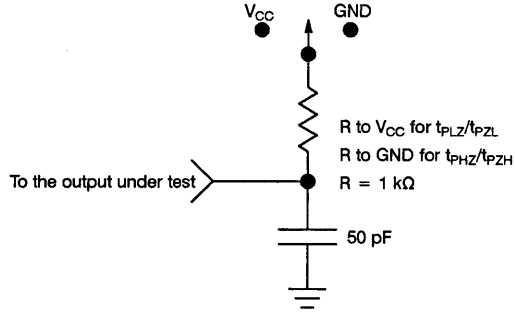


AC Test Loads

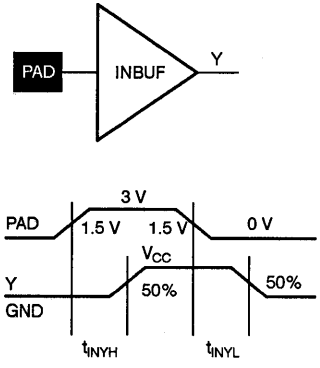
Load 1
(Used to measure propagation delay)



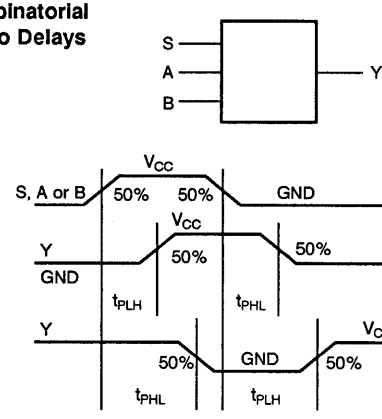
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

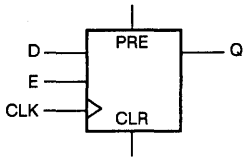


Combinatorial Macro Delays

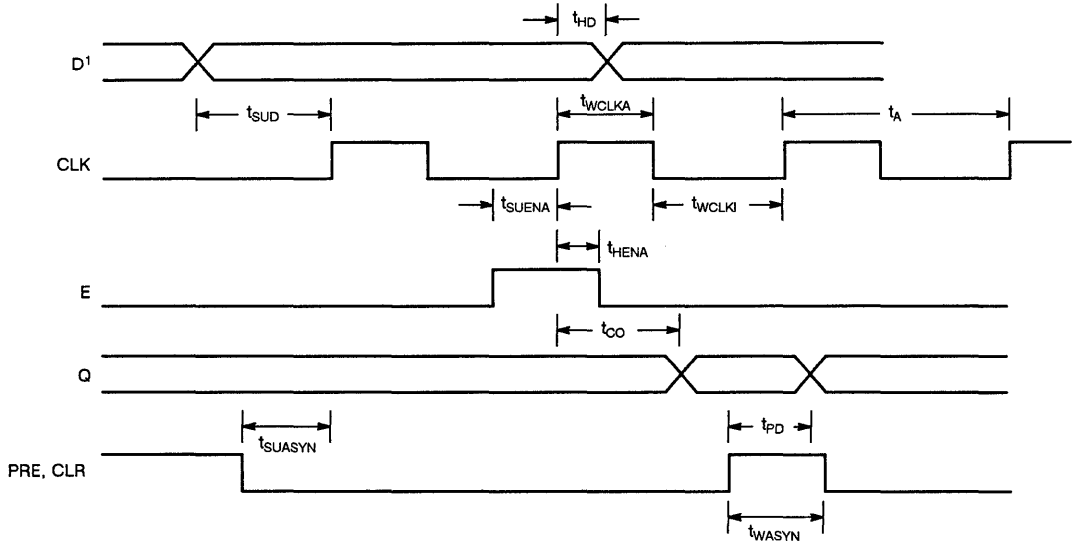


Sequential Timing Characteristics

Flip-Flops and Latches



(Positive edge triggered)



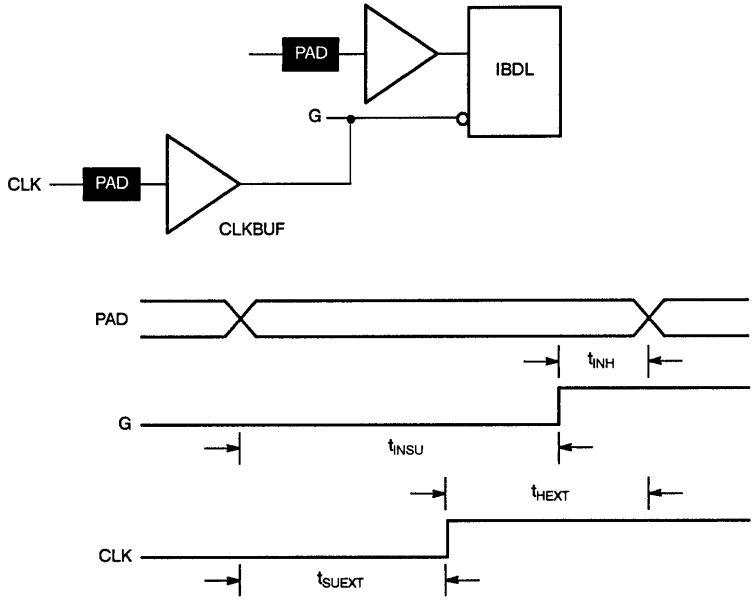
Notes:

1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

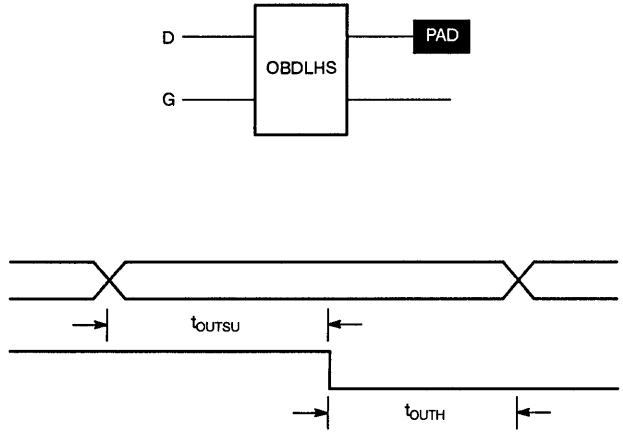
1

Sequential Timing Characteristics (continued)

Input Buffer Latches (ACT 2 only)



Output Buffer Latches (ACT 2 only)



Timing Characteristics

Timing characteristics for ACT arrays fall into three categories: family dependent, device dependent, and design dependent. The output buffer characteristics are common to all ACT 2 family members. Internal module delays are device dependent. Internal wiring delays between modules are design dependent. Design dependency means actual delays are not determined until after placement and routing of the users design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

The macro propagation delays shown in the Timing Characteristics tables include the module delay plus estimates derived from statistical analysis for wiring delay. This statistical estimate is based on fully utilized devices (90% module utilization).

Critical Nets and Typical Nets

Propagation delays are expressed for two types of nets: critical and typical. Critical nets are determined by net property assignment before placement and routing. Up to 6% of the nets in a design may be designated as *critical*, while 90% of the nets in a design are *typical*.

Fan-Out Dependency

Propagation delays depend on the fan-out (number of loads) driven by a macro. Delay time increases when fan-out increases due to the capacitive loading of the macro's inputs, as well as the interconnect's resistance and capacitance.

Long Tracks

Some nets in the design use *long tracks*. Long tracks are special routing resources that span multiple rows or columns or modules, and are used frequently in large fan-out (> 10) situations. Long tracks employ three and sometimes four antifuse connections. This increased capacitance and resistance results in longer net delays for macros connected to long tracks. Typically up to 6% of the nets in a fully utilized device require long tracks. Long tracks contribute an additional 10 ns to 15 ns delay.

Timing Derating

Operating temperature, operating voltage, and device processing conditions, along with device die size and speed grade, account for variations in array timing characteristics. These variations are summarized into a derating factor for array typical timing specifications. The derating factors shown in the table below are based on the recommended operating conditions for applications. The derating curves in Figure 15 show worst-to-best case operating voltage range and best-to-worst case operating temperature range. The temperature derating curve is based on device junction temperature. Actual junction temperature is determined from Ambient Temperature, Power Dissipation, and Package Thermal characteristics.

ACT 1 Timing Derating Factor (x typical)

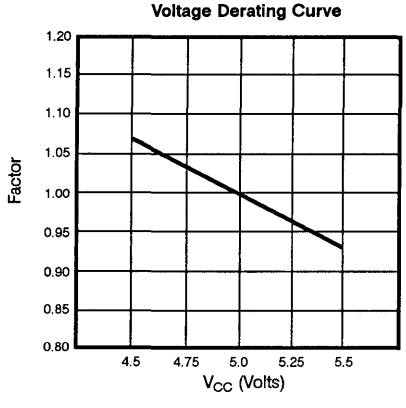
	Commercial		Military	
Speed Grade	Best-Case	Worst-Case	Best-Case	Worst-Case
Standard Speed	0.45	1.54	0.37	1.79
-1 Speed Grade	0.45	1.28	0.37	1.49

Note:
"Best-case" reflects maximum operating voltage, minimum operating temperature, and best-case processing. "Worst-case" reflects minimum operating voltage, maximum operating temperature, and worst-case processing. Best-case derating is based on sample data only and is not guaranteed.

ACT 2 Timing Derating Factor (x typical)

	Commercial		Military	
Speed Grade	Best-Case	Worst-Case	Best-Case	Worst-Case
Standard Speed	0.40	1.40	0.35	1.60

Note:
"Best-case" reflects maximum operating voltage, minimum operating temperature, and best-case processing. "Worst-case" reflects minimum operating voltage, maximum operating temperature, and worst-case processing. Best-case derating is based on sample data only and is not guaranteed.



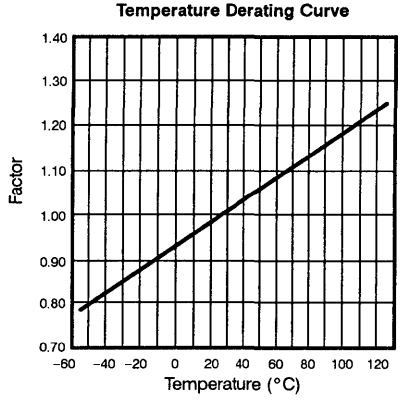


Figure 15. Derating Curves

ACT 1 Timing Characteristics

Logic Module Timing

V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; t_{PD} = 3.0 ns @ FO = 0

Single Logic Module Macros (e.g., most gates, latches, multiplexors)[1]

Parameter	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD}	Critical	5.4	5.8	6.2	8.5	Note 2	ns
t_{PD}	Typical	6.3	6.7	7.7	8.6	10.8	ns

Dual Logic Module Macros (e.g., adders, wide input gates)[1]

Parameter	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD}	Critical	9.2	9.6	10.0	12.3	Note 2	ns
t_{PD}	Typical	10.2	10.6	11.6	12.5	14.6	ns

Sequential Element Timing Characteristics

Parameter		Fan-Out					Units
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{SU}	Set Up Time, Data Latches	3.5	3.9	4.2	4.5	4.8	ns
t_{SU}	Set Up Time, Flip-Flops	3.9	3.9	3.9	3.9	3.9	ns
t_H	Hold Time	0	0	0	0	0	ns
t_W	Pulse Width, Minimum[3]	7.7	8.5	9.2	10.0	14.0	ns
t_{CQ}	Delay, Critical Net	5.4	5.8	6.2	8.5	Note 2	ns
t_{CQ}	Delay, Typical Net	6.3	6.7	7.7	8.6	10.8	ns

Notes:

1. Most flip-flops exhibit single module delays.
2. Critical nets have a maximum fan-out of six.
3. Minimum pulse width, t_W, applies to CLK, PRE, and CLR inputs.

ACT 1 Timing Characteristics (continued)

I/O Buffer Timing

V_{CC} = 5.0 V; T_A = 25°C; Process = Typical

INBUF Macros

Parameter	From – To	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PHL}	Pad to Y	6.9	7.6	8.9	10.7	14.3	ns
t_{PLH}	Pad to Y	5.9	6.5	7.7	8.4	12.4	ns

CLKBUF (High Fan-Out Clock Buffer) Macros

Parameter	FO = 40	FO = 160	FO = 320	Units
t_{PHL}	9.0	12.0	15.0	ns
t_{PLH}	9.0	12.0	15.0	ns

Notes:

1. A clock balancing feature is provided to minimize clock skew.
2. There is no limit to the number of loads that may be connected to the CLKBUF macro.

OUTBUF, TRIBUFF, and BIBUF Macros

C_L = 50 pF

Parameter	From – To	CMOS	TTL	Units
t_{PHL}	D to Pad	3.9	4.9	ns
t_{PLH}	D to Pad	7.2	5.7	ns
t_{PHZ}	E to Pad	5.2	3.4	ns
t_{PZH}	E to Pad	6.5	4.9	ns
t_{PLZ}	E to Pad	6.9	5.2	ns
t_{PZL}	E to Pad	4.9	5.9	ns

Change in Propagation Delay with Load Capacitance

Parameter	From – To	CMOS	TTL	Units
t_{PHL}	D to Pad	0.03	0.046	ns/pF
t_{PLH}	D to Pad	0.07	0.039	ns/pF
t_{PHZ}	E to Pad	0.08	0.046	ns/pF
t_{PZH}	E to Pad	0.07	0.039	ns/pF
t_{PLZ}	E to Pad	0.07	0.039	ns/pF
t_{PZL}	E to Pad	0.03	0.039	ns/pF

Notes:

1. The BIBUF macro input section exhibits the same delays as the INBUF macro.
2. Load capacitance delay delta can be extrapolated down to 15 pF minimum.

   Example:

   Delay for OUTBUF driving a 100-pF TTL load:

   t_{PHL} = 4.9 + (.046 x (100–50)) = 4.9 + 2.3 = 7.2 ns

   t_{PLH} = 5.7 + (.039 x (100–50)) = 5.7 + 2.0 = 7.7 ns

A1280 Timing Characteristics

Propagation Delays (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD1}	Single Module	Critical	4.5	5.0	5.5	6.0	–	ns
t_{PD1}	Single Module	Typical	5.7	6.2	6.7	8.2	11.7	ns
t_{PD2}	Dual Module	Critical	7.5	8.0	8.5	9.0	–	ns
t_{PD2}	Dual Module	Typical	8.7	9.2	9.7	11.2	14.7	ns
t_{CO}	Sequential Clk to Q	Critical	4.5	5.0	5.5	6.0	–	ns
t_{CO}	Sequential Clk to Q	Typical	5.7	6.2	6.7	8.2	11.7	ns
t_{GO}	Latch G to Q	Critical	4.5	5.0	5.5	6.0	–	ns
t_{GO}	Latch G to Q	Typical	5.7	6.2	6.7	8.2	11.7	ns
t_{PD}	Asynchronous to Q	Critical	4.5	5.0	5.5	6.0	–	ns
t_{PD}	Asynchronous to Q	Typical	5.7	6.2	6.7	8.2	11.7	ns

Sequential Timing Characteristics (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

		Commercial		Military		
Parameter	Description	Min.	Max.	Min.	Max.	Units
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		1.0		ns
t_{SUASYN}	Flip-Flop (Latch) Asynchronous Input Setup	1.0		2.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	5.0		7.5		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0	ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	7.5		9.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.5		9.0		ns
t_A	Flip-Flop (Latch) Clock Input Period	18.0		22.0		ns
t_{INH}	Input Buffer Latch Hold		2.0		2.5	ns
t_{INSU}	Input Buffer Latch Setup	-2.5		-3.5		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0	ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		1.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		48.0		39.0	MHz

Notes:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1280 Timing Characteristics (continued)

I/O Buffer Timing (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{INYH}	Pad to Y High	6.7	7.2	7.7	8.2	11.7	ns
t_{INYL}	Pad to Y Low	6.6	7.1	7.6	8.1	11.5	ns
t_{INGH}	G to Y High	6.6	7.2	7.7	8.2	11.7	ns
t_{INGL}	G to Y Low	6.4	6.9	7.5	8.0	11.4	ns

Global Clock Network (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 32	FO = 128	FO = 384	Units
t_{CKH}	Input Low to High	9.1	10.1	12.3	ns
t_{CKL}	Input High to Low	9.1	10.2	12.5	ns
t_{PWH}	Minimum Pulse Width High	6.0	6.0	6.0	ns
t_{PWL}	Minimum Pulse Width Low	6.0	6.0	6.0	ns
t_{CKSW}	Maximum Skew	0.5	1.0	2.5	ns
t_{SUEXT}	Input Latch External Setup	0.0	0.0	0.0	ns
t_{HEXT}	Input Latch External Hold	7.0	8.0	11.2	ns
t_P	Minimum Period	15.0	18.0	20.0	ns
f_{MAX}	Maximum Frequency	66.0	55.0	50.0	MHz

Output Buffer Timing (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	TTL	CMOS	Units
t_{DLH}	Data to Pad High	4.6	6.7	ns
t_{DHL}	Data to Pad Low	6.5	4.9	ns
t_{ENZH}	Enable Pad Z to High	8.3	8.3	ns
t_{ENZL}	Enable Pad Z to Low	5.5	5.5	ns
t_{ENHZ}	Enable Pad High to Z	4.5	4.5	ns
t_{ENLZ}	Enable Pad Low to Z	6.0	6.0	ns
t_{GLH}	G to Pad High	4.6	4.6	ns
t_{GHL}	G to Pad Low	6.5	6.5	ns
d_{TLH}	Delta Low to High	0.06	0.11	ns/pF
d_{THL}	Delta High to Low	0.11	0.08	ns/pF

A1240 Timing Characteristics

PRELIMINARY DATA

Propagation Delays (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD1}	Single Module	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{PD1}	Single Module	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{PD2}	Dual Module	Critical Net	7.5	8.0	8.5	9.0	–	ns
t_{PD2}	Dual Module	Typical Net	7.9	8.3	8.7	10.0	13.0	ns
t_{CO}	Sequential Clk to Q	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{CO}	Sequential Clk to Q	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{GO}	Latch G to Q	Critical Net	3.9	4.3	4.8	5.3	–	ns
t_{GO}	Latch G to Q	Typical Net	4.9	5.3	5.7	7.0	10.0	ns
t_{PD}	Asynchronous to Q	Critical	3.9	4.3	4.8	5.3	–	ns
t_{PD}	Asynchronous to Q	Typical	4.9	5.3	5.7	7.0	10.0	ns

Sequential Timing Characteristics (Over Worst-Case Recommended Operating Conditions; No Further Derating Required)

		Commercial		Military		
Parameter	Description	Min.	Max.	Min.	Max.	Units
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		1.0		ns
t_{SUASYN}	Flip-Flop (Latch) Asynchronous Input Setup	1.0		2.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	5.0		7.5		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0	ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	6.5		9.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.5		9.0		ns
t_A	Flip-Flop (Latch) Clock Input Period	15.0		20.0		ns
t_{INH}	Input Buffer Latch Hold		2.0		2.5	ns
t_{INSU}	Input Buffer Latch Setup	-2.5		-3.5		ns
t_{OUTH}	Output Buffer Latch Hold		0.0		0.0	ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		1.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		66.0		50.0	MHz

Notes:

1. Data applies to macros based on the sequential (S-type) module. Timing parameters for sequential macros constructed from C-type modules can be obtained from the ALS Timer utility.
2. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the G input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1240 Timing Characteristics (continued)

PRELIMINARY DATA

I/O Buffer Timing (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{INYH}	Pad to Y High	6.1	6.5	5.9	7.4	10.5	ns
t_{INYL}	Pad to Y Low	5.9	6.4	6.8	7.3	10.4	ns
t_{INGH}	G to Y High	6.1	6.5	5.9	7.4	10.5	ns
t_{INGL}	G to Y Low	5.9	6.4	6.8	7.3	10.4	ns

Global Clock Network (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	FO = 32	FO = 128	FO =256	Units
t_{CKH}	Input Low to High	9.1	10.1	11.2	ns
t_{CKL}	Input High to Low	9.1	10.2	11.3	ns
t_{PWH}	Minimum Pulse Width High	5.1	5.5	6.0	ns
t_{PWL}	Minimum Pulse Width Low	5.1	5.5	6.0	ns
t_{CKSW}	Maximum Skew	0.5	1.0	2.5	ns
t_{SUEXT}	Input Latch External Setup	0.0	0.0	0.0	ns
t_{HEXT}	Input Latch External Hold	7.0	8.0	11.2	ns
t_P	Minimum Period	12.0	15.0	16.6	ns
f_{MAX}	Maximum Frequency	80.0	66.0	60.0	MHz

Output Buffer Timing (V_{CC} = 5.0 V; T_A = 25°C; Process = Typical; Derating Required)

Parameter	Description	TTL	CMOS	Units
t_{DLH}	Data to Pad High	4.6	6.7	ns
t_{DHL}	Data to Pad Low	6.5	4.9	ns
t_{ENZH}	Enable Pad Z to High	8.3	8.3	ns
t_{ENZL}	Enable Pad Z to Low	5.5	5.5	ns
t_{ENHZ}	Enable Pad High to Z	4.5	4.5	ns
t_{ENLZ}	Enable Pad Low to Z	6.0	6.0	ns
t_{GLH}	G to Pad High	4.6	4.6	ns
t_{GHL}	G to Pad Low	6.5	6.5	ns
d_{TLH}	Delta Low to High	0.06	0.11	ns/pF
d_{THL}	Delta High to Low	0.11	0.08	ns/pF

ALS Design Environment

Hard and Soft Macros

Designing within the Actel design environment is accomplished through a building block approach. Over 250 logic function macros are provided in the ACT 1 and ACT 2 design libraries. Hard macros range from simple SSI gates such as AND, NOR, and exclusive OR to more complex functions such as flip-flops with 4:1 multiplexed data inputs.

Hard macros are implemented within the ACT 1 architecture by utilizing one or two modules. Hard macros are implemented within the ACT 2 architecture by utilizing one or more C-Modules and/or S-Modules. Over 150 of these macros are implemented within a single logic module, although several two-module macros are available. One- and two-module macros have a small propagation delay variance, which allows accurate performance prediction.

Soft macros comprise multiple hard macros connected to form complex functions ranging from MSI functions to 16-bit counters and accumulators. A large number of TTL equivalent hard and soft macros also are provided.

Design Compatibility

The design libraries for ACT 2 are fully upward compatible from the ACT 1 design libraries. ACT 1 designs can be converted to equivalent gate-count ACT 2 arrays. The Activator 2 programmer supports ACT 1 and ACT 2 device families.

ACT 1 Macro Library
Soft Macro Library Overview

Macro Name	Modules Required	Description	Levels of Logic
Counters			
CNT4A	17	4-bit loadable binary counter with clear	4
CNT4B	15	4-bit loadable bin counter w/ clr, active low carry in & carry out	4
UDCNT4A	24	4-bit up/down cntr w/ sync active low load, carry in & carry out	6
Decoders			
DEC2X4	4	2 to 4 decoder	1
DEC2X4A	4	2 to 4 decoder with active low outputs	1
DEC3X8	8	3 to 8 decoder	1
DEC3X8A	8	3 to 8 decoder with active low outputs	1
DEC4X16A	20	4 to 16 decoder with active low outputs	2
DECE2X4	4	2 to 4 decoder with enable	1
DECE2X4A	4	2 to 4 decoder with enable and active low outputs	1
DECE3X8	11	3 to 8 decoder with enable	2
DECE3X8A	11	3 to 8 decoder with enable and active low outputs	2
Latches and Registers			
DLC8A	8	Octal latch with clear	1
DLE8	8	Octal latch with enable	1
DLM8	8	Octal latch with mulitplexed inputs	1
REGE8A	20	Octal register with preset and clear, active high enable	2
REGE8B	20	Octal register with active low clock, preset and clear, active high enable	2
Adders			
FA1	3	One-bit full adder	3
FADD8	37	8-bit fast adder	4
FADD12	62	12-bit fast adder	5
FADD16	78	16-bit fast adder	5
FADD24	120	24-bit fast adder	6
FADD32	160	32-bit fast adder	7

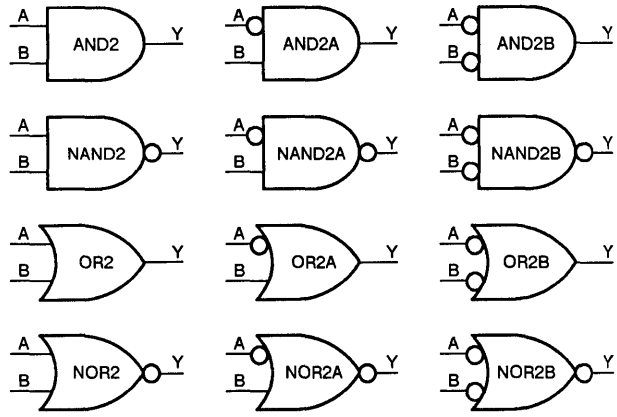
ACT 1 Macro Library
Soft Macro Library Overview (continued)

Macro Name	Modules Required	Description	Levels of Logic
Comparators			
ICMP4	5	4-bit identity comparator	2
ICMP8	9	8-bit identity comparator	3
MCMP16	93	16-bit magnitude comparator	5
MCMPC2	9	2-bit magnitude comparator with enables	3
MCMPC4	18	4-bit magnitude comparator with enables	4
MCMPC8	36	8-bit magnitude comparator with enables	6
Multiplexors			
MX8	3	8 to 1 multiplexor	2
MX8A	3	8 to 1 multiplexor with an active low output	2
MX16	5	16 to 1 multiplexor	2
Multipliers			
SMULT8	235	8 x 8 two's complement multiplier	Varies
Shift Registers			
SREG4A	8	4-bit shift register with clear	2
SREG8A	18	8-bit shift register with clear	2
TTL Replacements			
TA138	12	3 to 8 decoder with 3 enables and active low outputs	2
TA139	4	2 to 4 decoder with an enable and active low outputs	1
TA151	5	8 to 1 multiplexor with enable, true, and complementary outputs	3
TA153	2	4 to 1 multiplexor with active low enable	2
TA157	1	2 to 1 multiplexor with enable	1
TA161	22	4-bit sync counter w/ load, clear, count enables & ripple carry out	3
TA164	18	8-bit serial in, parallel out shift register	1
TA169	25	4-bit synchronous up/down counter	6
TA181	31	4-bit ALU	4
TA194	14	4-bit shift register	1
TA195	10	4-bit shift register	1
TA269	50	8-bit up/down cntr w/ clear, load, ripple carry output & enables	8
TA273	18	Octal register with clear	1
TA280	9	Parity generator and checker	4
TA377	16	Octal register with active low enable	1
Super Macros			
UART	189	Universal Asychronous Receiver/Transmitter	7-Tx 4-Rx
MC	102	DRAM Controller	Varies
DMA	225	Direct Memory Access Controller	Varies
SINT	180	SCSI Interface Controller	Varies

ACT 1 Macro Library
Hard Macro Library Overview

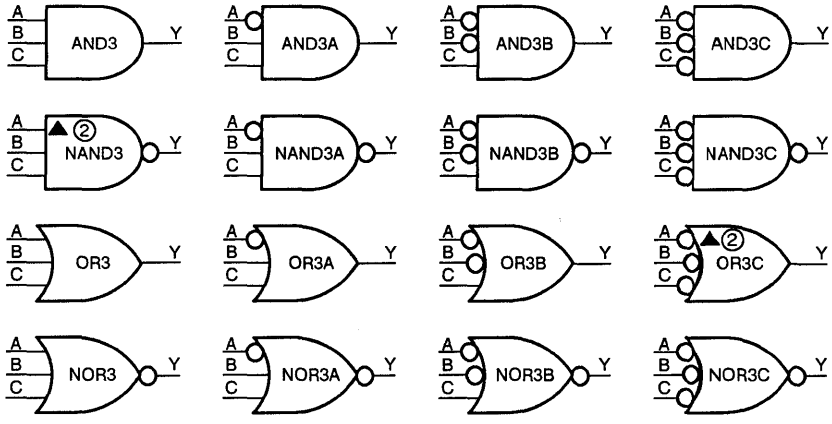
The following illustrations show all the available Hard Macros.

2-Input Gates (Module Count = 1)



3-Input Gates (Module Count = 1, unless indicated otherwise)

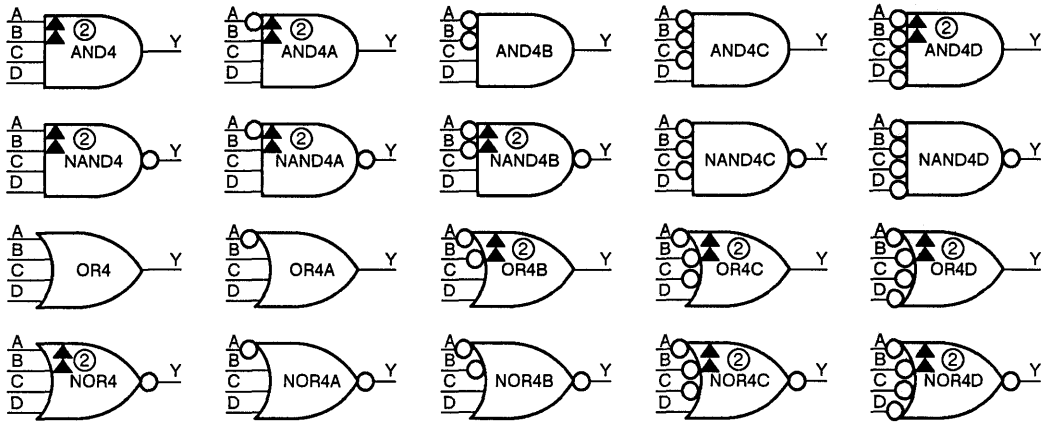
② Indicates 2-module macro
▲ Indicates extra delay input



ACT 1 Macro Library

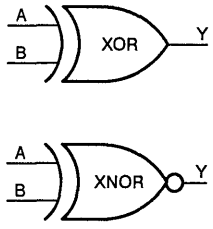
4-Input Gates (Module Count = 1, unless indicated otherwise)

② Indicates 2-module macro
▲ Indicates extra delay input

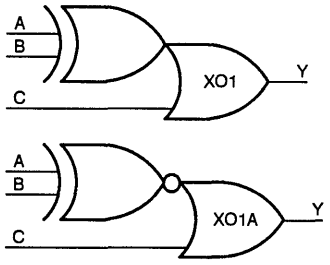


1

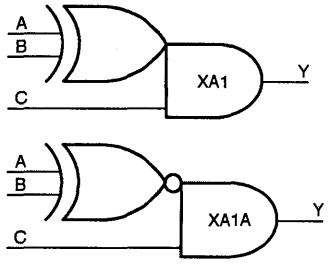
XOR Gates
(Module Count = 1)



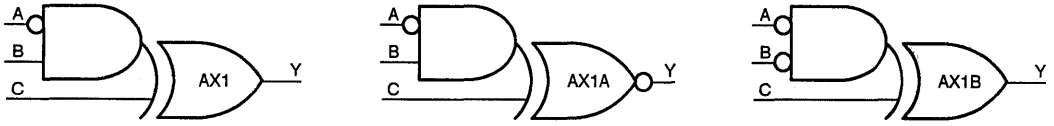
XOR-OR Gates
(Module Count = 1)



XOR-AND Gates
(Module Count = 1)



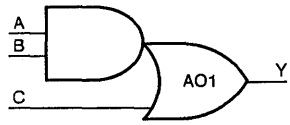
AND-XOR Gates
(Module Count = 1)

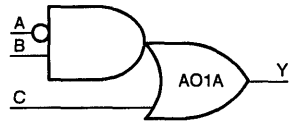


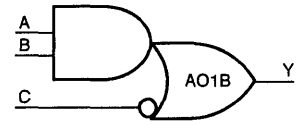
ACT 1 Macro Library

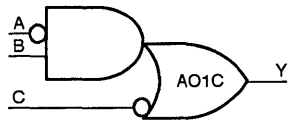
AND-OR Gates (Module Count = 1)

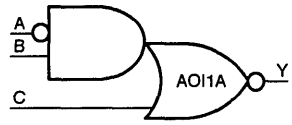
② Indicates 2-module macro
▲ Indicates extra delay input

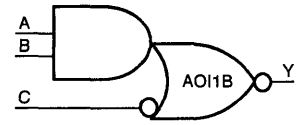


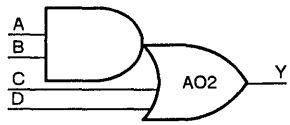


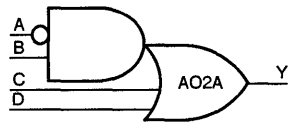


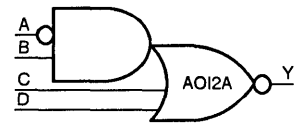


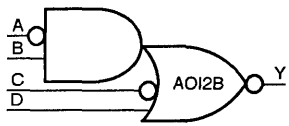


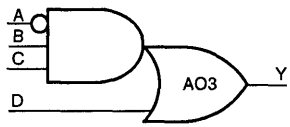


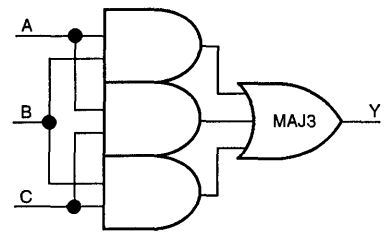


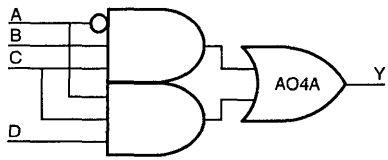


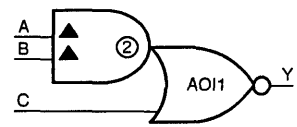


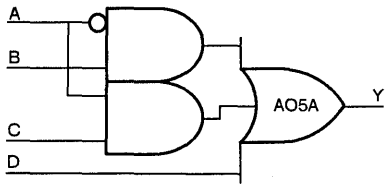


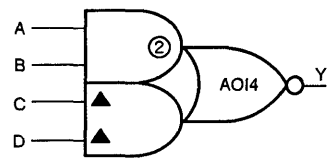


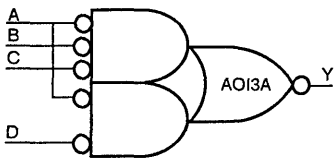








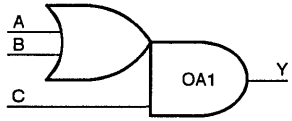


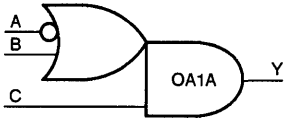


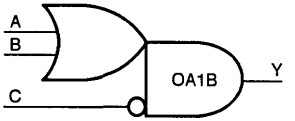
ACT 1 Macro Library

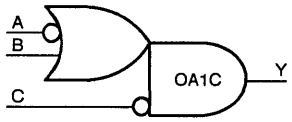
OR-AND Gates (Module Count = 1)

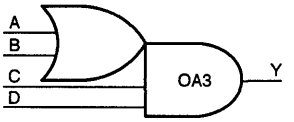
② Indicates 2-module macro
▲ Indicates extra delay input

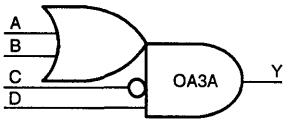


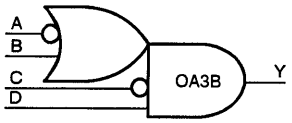


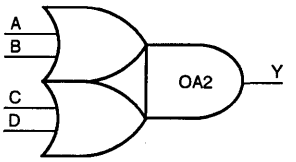


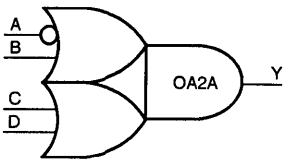


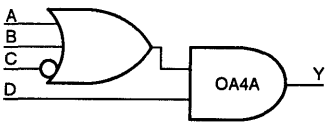


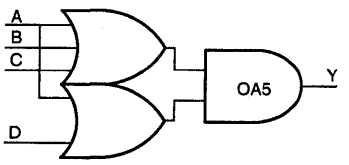


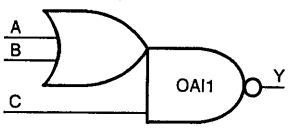


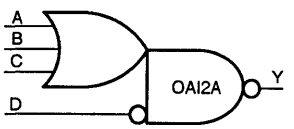


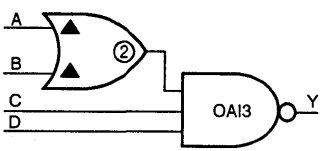






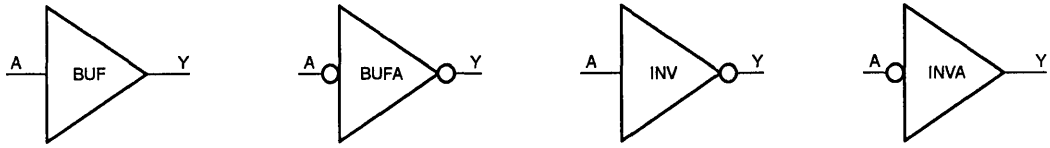




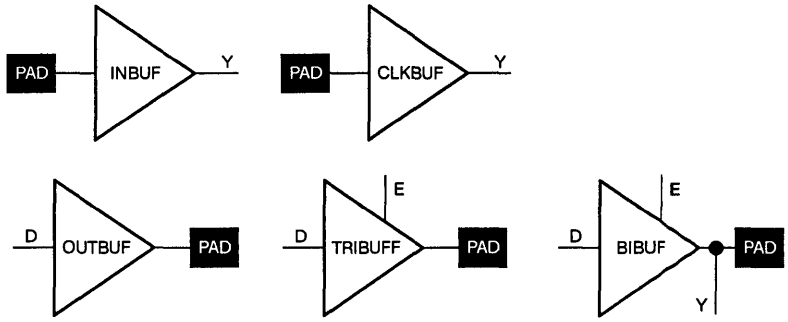


ACT 1 Macro Library

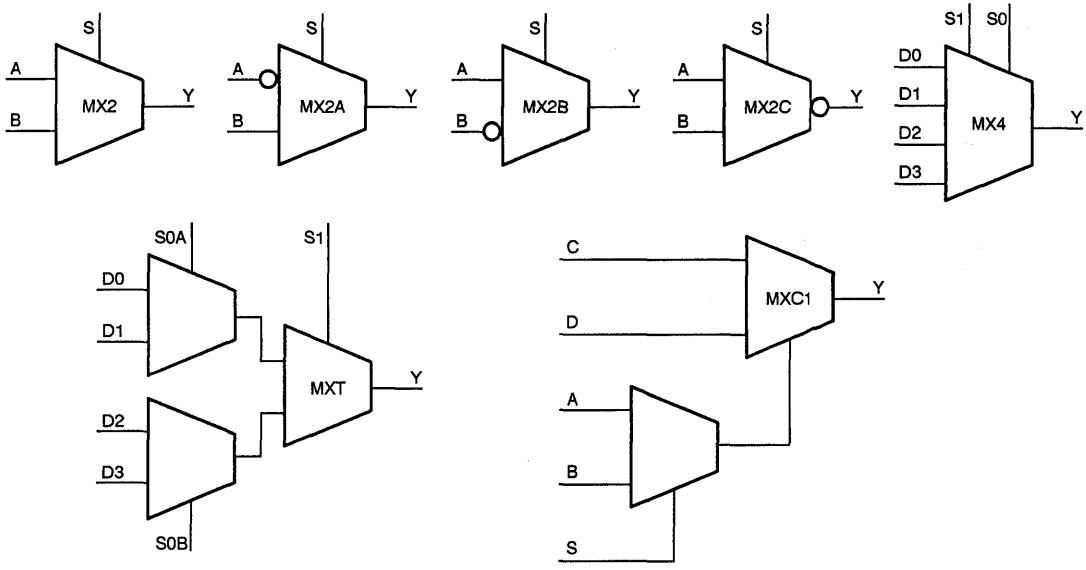
Buffers (Module Count = 1)



I/O Buffers (I/O Module Count = 1)

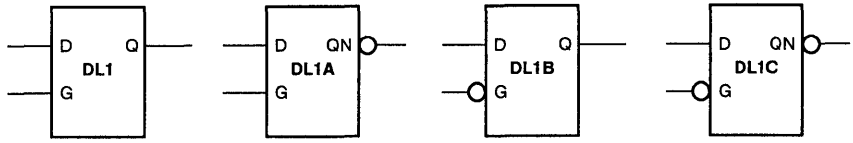


Multiplexors (Module Count = 1)

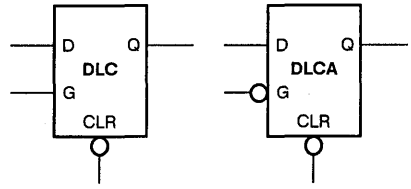


ACT 1 Macro Library

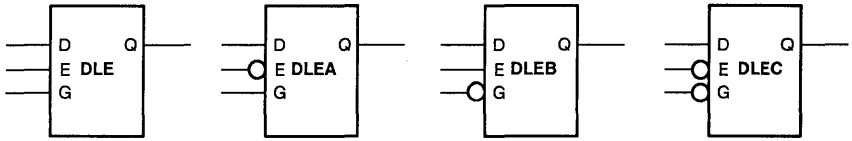
Latches (Module Count = 1)



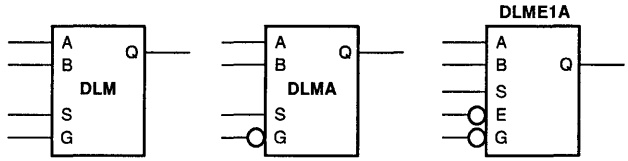
D-Latches with Clear (Module Count = 1)



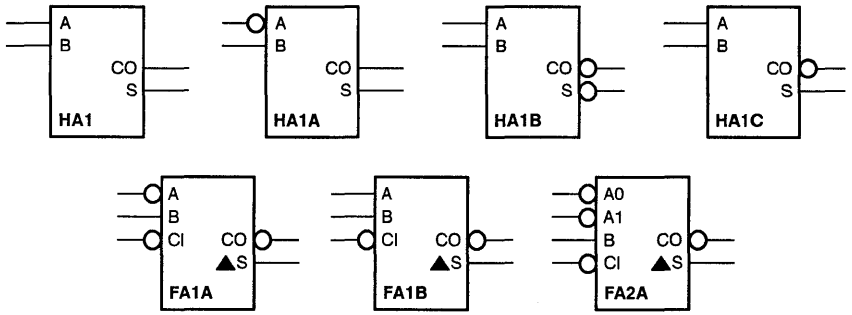
D-Latches with Enable (Module Count = 1)



Mux Latches (Module Count = 1)



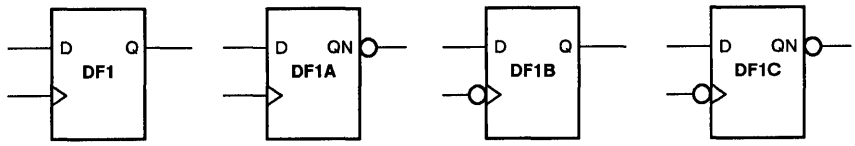
Adders (Module Count = 2)



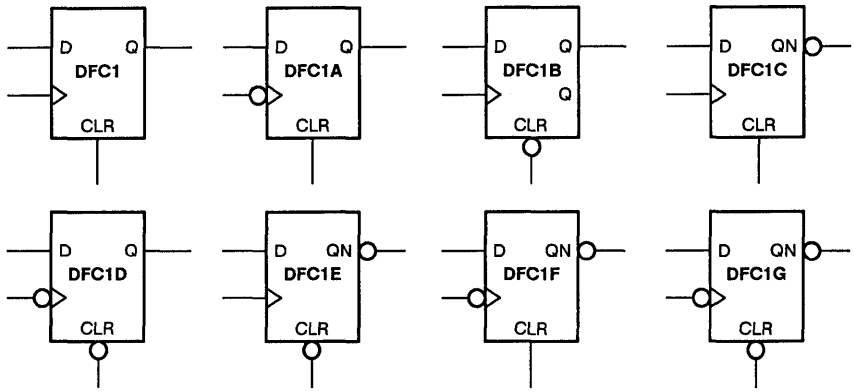
Macros FA1A, FA1B, and FA2A have two level delays from the inputs to the S outputs, as indicated by the▲

ACT 1 Macro Library

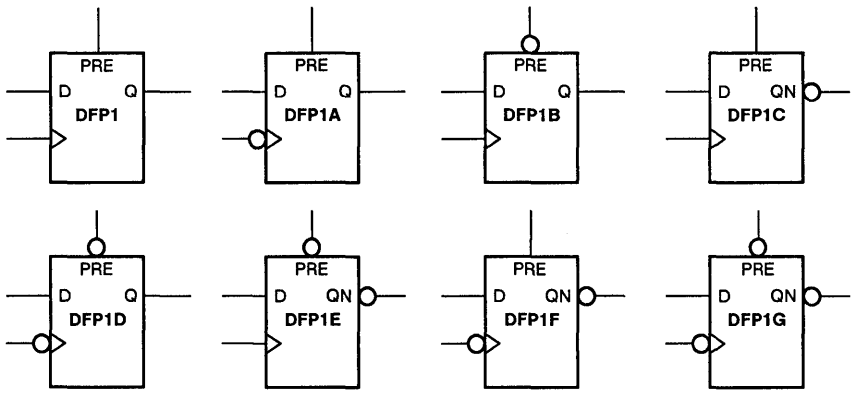
D-Flip-Flops (Module Count = 2)



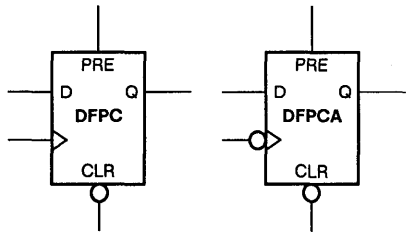
D-Flip-Flops with Clear



D-Flip-Flops with Preset

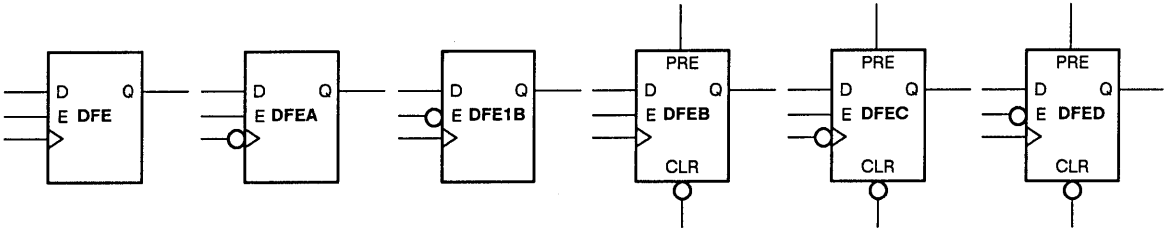


D-Flip-Flops with Preset and Clear

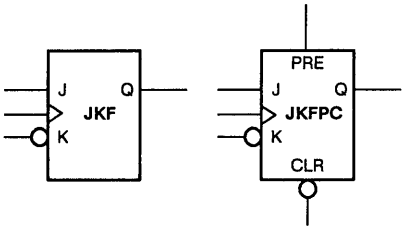


ACT 1 Macro Library

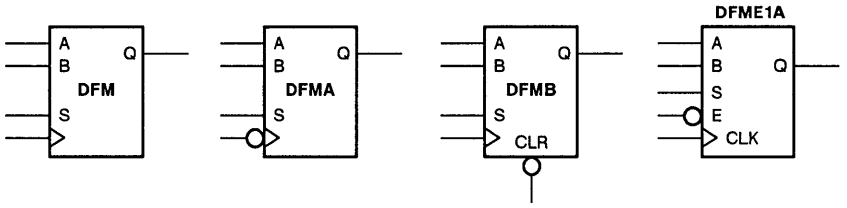
D-Flip-Flops with Enable (Module Count = 2)



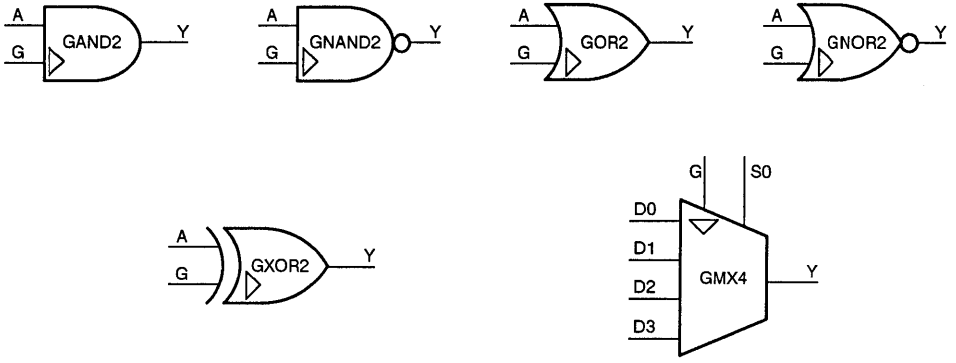
JK Flip-Flops (Module Count = 2)



Mux Flip-Flops (Module Count = 2)



CLKBUF Interface Macros (Module Count = 1)



ACT 2 Macro Library

Overview

The following tables describe ACT 2 macros, which are building blocks for designing FPGAs with the ALS and your CAE interface.

The macros are divided into four categories: I/O Macros, Hard Macros (Combinable and Non-Combinable), Soft Macros, and TTL Macros.

Equation Statement Elements

Combinatorial Elements

All equations for combinatorial logic elements use the following operators:

Operator	Symbol
AND	See Note 1
NOT	!
OR	+
XOR	^

Notes:

1. A space between the 'A' and 'B' in the equation Y = A B means **A AND B.**
2. Order of operators in decreasing precedence is: NOT, AND, XOR, and OR.
3. Signals expressed in bold have a dual module delay.

Sequential Elements

All equations for sequential logic elements use the following formula:

Q = <!> (<!> CLK or G, <data equation>, <!> CLR, <!> PRE)

<!>	Optional Inversion
CLK	Flip-Flop Clock Pin
G	Latch Gate Pin
CLR	Asynchronous Clear Pin
PRE	Asynchronous Preset Pin

ACT 2 Macro Selections

I/O Macros

Macro Name	No. of Modules		Description
	I/O	Clock	
INBUF	1		Input
IBDL	1		Input with Input Latch
BBDLHS	1		Bidirectional with Input Latch and Output Latch
BBHS	1		Bidirectional
BIBUF	1		Bidirectional
CLKBIBUF	1	1	Bidirectional with Input Dedicated to Clock Network
CLKBUF	1	1	Input for Dedicated Clock Network
OBDLHS	1		Output with Output Latch
OBHS	1		Output
OUTBUF	1		Output
TBDLHS	1		Three State Output with Latch
TBHS	1		Three State Output
TRIBUFF	1		Three State Output

Note:

The following are functionally identical:
OBHS and OUTBUF; TRIBUFF and TBHS; BBHS and BIBUF

ACT 2 Macro Library

TTL Macros

Macro Name	Description	Logic Levels	No. of Modules	
			Seq.	Comb.
TA00	2-input NAND	1		1
TA02	2-input NOR	1		1
TA04	Inverter	1		1
TA07	Buffer	1		1
TA08	2-input AND	1		1
TA10	3-input NAND	1		1
TA11	3-input AND	1		1
TA20	4-input NAND	1		2
TA21	4-input AND	1		1
TA27	3-input NOR	1		1
TA32	2-input OR	1		1
TA40	4-input NAND	1		2
TA42	4 to 10 decoder	1		10
TA51	AND-OR-Invert	1		2
TA54	4-wide AND-OR-Invert	2		5
TA55	2-wide 4-input AND-OR-Invert	2		3
TA86	2-input exclusive OR	1		1
TA138	3 to 8 decoder with enable and active low outputs	2		12
TA139	2 to 4 decoder with enable and active low outputs	1		4
TA150	16 to 1 multiplexor	3		6
TA151	8 to 1 multiplexor with enable and active low outputs	3		5
TA153	4 to 1 multiplexor	2		2
TA154	4 to 16 decoder	2		22
TA157	2 to 1 multiplexor	1		1
TA160	4-bit decode counter with clear	4	4	12
TA161	4-bit binary counter with clear	3	4	10
TA164	8-bit serial in, parallel out shift register	1	8	
TA169	4-bit up/down counter	6	4	14
TA174	Hex D-type flip-flop with clear	1	6	
TA175	Quadruple D-type flip-flop with clear	1	4	
TA190	4-bit up/down decode counter with up/down mode	7	4	31
TA191	4-bit up/down binary counter with up/down mode	7	4	30
TA194	4-bit shift register	1	4	4
TA195	4-bit shift register	1	4	1
TA269	8-bit up/down binary counter	8	8	28
TA273	Octal register with clear	1	8	
TA280	Parity generator and checker	4		9
TA377	Octal register with active low enable	1	8	
TA688	8-bit identity comparator	3		9

ACT 2 Macro Library

Soft Macros

Function	Description	Macro Name	Logic Levels	No. of Modules	
				Seq.	Comb.
Counters	4-bit binary counter with load, clear	CNT4A	4	4	8
	4-bit binary counter with load, clear, carry in, carry out	CNT4B	4	4	7
	4-bit up/down counter with load, carry in, and carry out	UDCNT4A	5	4	13
	very fast 16-bit down counter	VCNT16C	1	34	31
	2-bit down counter, prescaler	VCNT2CP	1	5	2
	2-bit down counter, most significant bit	VCNT2CU	1	2	3
	4-bit down counter, middle bits	VCNT4C	1	4	8
	4-bit down counter, low order bits	VCNT4CL	1	4	7
Decoders	2 to 4 decoder	DEC2X4	1		4
	2 to 4 decoder with active low outputs	DEC2X4A	1		4
	3 to 8 decoder	DEC3X8	1		8
	3 to 8 decoder with active low outputs	DEC3X8A	1		8
	4 to 16 decoder with active low outputs	DEC4X16A	2		20
	2 to 4 decoder with enable	DECE2X4	1		4
	2 to 4 decoder with enable and active low outputs	DECE2X4A	1		4
	3 to 8 decoder with enable	DECE3X8	2		11
	3 to 8 decoder with enable and active low outputs	DECE3X8A	2		11
Registers	octal latch with clear	DLC8A	1	8	
	octal latch with enable	DLE8	1	8	
	octal latch with multiplexed data	DLM8	1	8	
	4-bit shift register with clear	SREG4A	1	4	
	8-bit shift register with clear	SREG8A	1	8	
Adders	8-bit adder	FADD8	3		44
	9-bit adder	FADD9	3		49
	10-bit adder	FADD10	3		56
	12-bit adder	FADD12	4		69
	16-bit adder	FADD16	5		97
	2-bit sum generator	SUMX1A	2		5
	very fast 16-bit adder	VADD16C	3		97
Comparators	4-bit identity comparator	ICMP4	2		5
	8-bit identity comparator	ICMP8	3		5
	2-bit magnitude comparator with enable	MCMPC2	3		9
	4-bit magnitude comparator with enable	MCMPC4	4		18
	8-bit magnitude comparator with enable	MCMPC8	6		36
Multiplexors	8 to 1 multiplexor	MX8	2		3
	8 to 1 multiplexor with active low outputs	MX8A	2		3
	16 to 1 multiplexor	MX16	2		5

ACT 2 Macro Library

Combinable Hard Macros 1 (for DF1, DF1B, DFC1B, DFC1D, DL1, DL1B, DLC, and DLCA)

Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
AND	2-input	AND2	Y = A B		1
		AND2A	Y = !A B		1
		AND2B	Y = !A !B		1
		AND3B	Y = !A !B C		1
AND-OR		AO1A	Y = ((!A) B) + C		1
		AO1D	Y = (!A !B) + C		1
AND-OR Invert		AOI1D	Y = !((!A !B) + !C)		1
Buffers and Inverters		BUF	Y = A		1
		BUFA	Y = !(!A)		1
		INV	Y = !A		1
		INVA	Y = !A		1
Clock Net Interface		GAND2	Y = A G		1
		GNOR2	Y = !(A + G)		1
		GOR2	Y = A + G		1
Multiplexor	2:1	MX2	Y = (A !S) + (B S)		1
NAND	2-input	NAND2A	Y = !(!A B)		1
		NAND2B	Y = !(!A !B)		1
	3-input	NAND3C	Y = !(!A !B !C)		1
NOR	2-input	NOR2	Y = !(A + B)		1
		NOR2A	Y = !(!A + B)		1
		NOR2B	Y = !(!A + !B)		1
	3-input	NOR3A	Y = !(!A + B + C)		1
OR-AND		OA1	Y = (A + B) C		1
OR	2-input	OR2	Y = A + B		1
		OR2A	Y = !A + B		1
	3-input	OR3	Y = A + B + C		1

ACT 2 Macro Library

Combinable Hard Macros 2 (for DF1, DF1B, DFC1B, DFC1D, DL1, and DL1B)

Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
AND	3-input	AND3	Y = A B C		1
		AND3A	Y = !A B C		1
		AND3C	Y = !A !B !C		1
	4-input	AND4B	Y = !A !B C D		1
		AND4C	Y = !A !B !C D		1
AND-OR		AO1	Y = (A B) + C		1
		AO1B	Y = (A B) + (!C)		1
		AO1C	Y = ((!A) B) + (!C)		1
		AO1E	Y = (!A !B) + !C		1
		AO11	Y = A B + ((A + B) C)		1
		AO2	Y = ((A B) + C + D)		1
		AO2A	Y = ((!A B) + C + D)		1
		AO2B	Y = (!A !B) + C + D		1
		AO2C	Y = (!A B) + !C + D		1
		AO2D	Y = (!A !B) + !C + D		1
		AO3	Y = (!A B C) + D		1
		AO3B	Y = (!A !B C) + D		1
		AO3C	Y = (!A !B !C) + D		1
		A04A	Y = (!A B C) + (A C D)		1
		AO5A	Y = (!A B) + (A C) + D		1
AND-OR Invert		AOI1A	Y = !((!A B) + C)		1
		AOI1B	Y = !((A B) + !C)		1
		AOI1C	Y = !((!A !B) + C)		1
		AOI2A	Y = !((!A B) + C + D)		1
		AOI3A	Y = !((!A !B !C) + (!A !D)		1
Exclusive OR	XNOR, AND-XOR	AX1B	Y = (!A !B) ^ C		1
Boolean		CS2	Y = !((A + S) B) C + ((A + S) B) D		1
		CY2B	Y = A1 B1 + (A0 + B0) A1 + (A0 + B0) B1		1
Clock Net Interface		GMX4	Y = (D0 !S0 !G) + (D1 !G S0) + (D2 G !S0) + (D3 S0 G)		1
		GNAND2	Y = !(A G)		1
		GXOR2	Y = A ^ G		1
AND-OR		MAJ3	Y = (A B) + (B C) + (A C)		1
Multiplexor		MX2A	Y = (!A !S) + (B S)		1
		MX2C	Y = (!A !S) + (!B S)		1
	4:1	MX4	Y = (D0 !S0 !S1) + (D1 S0 !S1) + (D2 !S0 S1) + (D3 S0 S1)		1
NAND	2-input	NAND2	Y = !(A B)		1
	3-input	NAND3A	Y = !(!A B C)		1
		NAND3B	Y = !(!A !B C)		1
	4-input	NAND4C	Y = !(!A !B !C D)		1
		NAND4D	Y = !(!A !B !C !D)		1
NOR	3-input	NOR3	Y = !(A + B + C)		1
		NOR3B	Y = !(!A + !B + C)		1
		NOR3C	Y = !(!A + !B + !C)		1
	4-input	NOR4A	Y = !(!A + B + C + D)		1
		NOR4B	Y = !(!A + !B + C + D)		1

ACT 2 Macro Library

Combinable Hard Macros 2 (continued) (for DF1, DF1B, DFC1B, DFC1D, DL1, and DL1B)

Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
OR-AND		OA1A	Y = (!A + B) C		1
		OA1B	Y = (A + B) (!C)		1
		OA1C	Y = (!A + B) (!C)		1
		OA2	Y = (A + B) (C + D)		1
		OA2A	Y = (!A + B) (C+ D)		1
		OA3	Y = ((A + B) C D)		1
		OA3A	Y = ((A + B) !C D)		1
		OA4	Y = (A + B + C) D		1
		OA4A	Y = ((A + B + !C) D)		1
		OA5	Y = (A+B+C)(A+D)		1
OR-AND Invert		OAI1	Y = !((A + B) C)		1
		OAI2A	Y = !((A + B + C) !D)		1
		OAI3A	Y = !((A + B) !C !D)		1
OR	3-input	OR3A	Y = !A + B + C		1
		OR3B	Y = !A + !B + C		1
	4-input	OR4	Y = A + B + C + D		1
		OR4A	Y = !A + B + C + D		1
Exclusive OR	XOR	XOR	Y = A ^ B		1
		XO1	Y = (A ^ B) + C		1
		XO1A	Y = !(A ^ B) + C		1
	XNOR, AND-XOR	XNOR	Y = !(A ^ B)		1
		XA1	Y = (A ^ B) C		1
		XA1A	Y = !(A ^ B) C		1

ACT 2 Macro Library

Non-Combinable Hard Macros

Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
AND	4-input	AND4	Y = A B C D		1
		AND4A	Y = (!A B C D)		1
		AND4D	Y = !A !B !C !D		2
	5-input	AND5B	Y = !A !B C D E		1
OR	2-input	OR2B	Y = !A + !B		1
	3-input	OR3C	Y = !A + !B + !C		1
	4-input	OR4B	Y = !A + !B + C + D		1
		OR4C	Y = !A + !B + !C + D		1
		OR4D	Y = !A + !B + !C + !D		2
	5-input	OR5B	Y = !A + !B + C + D + E		1
NAND	3-input	NAND3	Y = !(A B C)		1
	4-input	NAND4	Y = !(A B C D)		2
		NAND4A	Y = !(!A B C D)		1
		NAND4B	Y = !(!A !B C D)		1
	5-input	NAND5C	Y = !(!A !B !C D E)		1
NOR	4-input	NOR4	X = !(A + B + C + D)		2
		NOR4C	Y = !(!A + !B + !C + D)		1
		NOR4D	Y = !(!A + !B + !C + !D)		1
	5-input	NOR5C	Y = !(!A + !B + !C + D +E)		1
Exclusive OR	XNOR, AND-XOR	AX1	Y = (!A B) ^ C		1
		AX1A	Y = !(!A B) ^ C		2
		AX1C	Y = (A B) ^ C		1
AND-OR		A02E	Y = (!A !B) + !C + !D		1
		AO3A	Y = (A B C) + D		1
		AO6	Y = A B + C D		1
		AO6A	Y = A B + C !D		1
		AO7	Y = A B C + D + E		1
		AO8	Y = (A B) + (!C !D) + E		1
		AO9	Y = (A B) + C + D + E		1
		AO10	Y = (A B + C) (D + E)		1
AND-OR Invert		AOI1	Y = !(A B + C)		1
		AOI2B	Y = !((!A B) + !C + D)		1
		AOI4	Y=!((A B) + (C D))		2
		AOI4A	Y = !(A B + !C D)		1
OR-AND		OA3B	Y = ((!A + B) !C D)		1
OR-AND Invert		OAI3	Y = !((A + B) C D)		1
Multiplexor	2:1	MX2B	Y = (A !S) + (!B S)		1

ACT 2 Macro Library

Non-Combinable Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
Adders	half	HA1	CO = A B S = A ^ B		2
		HA1A	CO = !A B S = !(A ^ B)		2
		HA1B	CO = !(A B) S = !(A ^ B)		2
		HA1C	CO = !(A B) S = (A ^ B)		2
	full	FA1A	CO = (CI !B !A) + (A !B) + (B CI A) S = (B !A !CI) + (CO !A CI) + (CO A !CI) + (B A CI)		2
		FA1B	CO = !A(!B + B CI) + A(!B CI) S = !A(!CI CO + CI B) + A(!CI B + CI CO)		2
		FA2A	CO = (CI !B !(A0+A1)) + (!B (A0+A1)) + (B CI (A0+A1)) S = (B !(A0+A1) !CI) + (CO !(A0+A1) CI) + (CO(A0+A1) !CI) + (B(A0+A1)CI)		2
Boolean		CS1	Y = !(A + S B) C + D (A + S B)		1
		CY2A	Y = A1 B1 + A0 B0 A1 + A0 BO B1		1
		MXT	Y = (!S1 (!S0A D0) + (S0A D1)) + (S1 (!S0B D2 + S0B D3))		2
		MXC1	Y = !(!S A + S B) C + (!S A + S B) D		2
D-type Flip-Flops		DF1	Q = (CLK, D, –, –)	1	
		DF1A	QN = !(CLK, D, –, –)	1	
		DF1B	Q = (!CLK, D, –, –)	1	
		DF1C	QN = !(!CLK, D,– ,–)	1	
	with clear	DFC1	Q = (CLK, D, CLR, –)	1	1
		DFC1A	Q = (!CLK, D, CLR, –)	1	1
		DFC1B	Q = (CLK, D, !CLR, –)	1	
		DFC1D	Q = (!CLK, D, !CLR, –)	1	
		DFC1E	QN = !(CLK, D, !CLR, –)	1	1
		DFC1G	QN = !(!CLK, D, !CLR, –)	1	1
	with enable	DFE	Q = (CLK, !E Q + E D, –, –)	1	
		DFE1B	Q = (CLK, !E D + E Q, –, –)	1	
		DFE1C	Q = (!CLK, D !E + Q E, –, –)	1	
		DFE3A	Q = (CLK, D E + Q !E, !CLR, –)	1	
		DFE3B	Q = (!CLK, D E + Q !E, !CLR, –)	1	
		DFE3C	Q = (CLK, D !E + Q E, !CLR, –)	1	
		DFE3D	Q = (!CLK, D !E + Q E, !CLR, –)	1	
		DFEA	Q = (!CLK, !E Q + E D, –, –)	1	1

ACT 2 Macro Library

Non-Combinable Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
D-type Flip-Flops (continued)	with multiplexed data	DFM	Q = (CLK, A !S + B S, –, –)	1	
		DFM1B	QN = !(CLK, A !S + B S, –, –)	1	
		DFM1C	QN = !(!CLK, A !S + B S, –, –)	1	
		DFM3	Q = (CLK, A !S + B S, CLR, –)	1	1
		DFM3B	Q = (!CLK, A !S + B S, !CLR, –)	1	
		DFM3E	Q = (!CLK, A !S + B S, CLR, –)	1	1
		DFM4C	QN = !(CLK, !A !S + !B S, –, !PRE)	1	
		DFM4D	QN = !(!CLK, A !S + B S, –, !PRE)	1	
		DFM6A	Q = (CLK, (D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1), !CLR, –)	1	
		DFM6B	Q = (!CLK, (D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1), !CLR, –)	1	
		DFM7A	Q = (CLK, !CLR, (D0 !S0 + D1 S0) !(S10 + S11) + (D2 !S0 + D3 S0) (S10 + S11))	1	
		DFM7B	Q = (!CLK, !CLR, (D0 !S0 + D1 S0) !(S10 + S11) + (D2 !S0 + D3 S0) (S10 + S11))	1	
		DFMA	Q = (!CLK, A !S + B S, –, –)	1	
		DFMB	Q = (CLK, A !S + B S, !CLR, –)	1	
		DFME1A	Q = (CLK, !E A !S + !E B S + E Q, –, –)	1	
	with preset	DFP1	Q = (CLK, D, –, PRE)		2
		DFP1A	Q = (!CLK, D, –, PRE)		2
		DFP1B	Q = (CLK, D, –, !PRE)		2
		DFP1C	QN = !(CLK, D, –, PRE)	1	1
		DFP1D	Q = (!CLK, D, –, !PRE)	2	
		DFP1E	QN = !(CLK, D, –, !PRE)	1	
		DFP1F	Q = (!CLK, D, –, PRE)	1	1
		DFP1G	QN = !(!CLK, D, –, !PRE)		1
	with clear and preset	DFPC	Q = (CLK, D, CLR, PRE)		2
		DFPCA	Q = (!CLK, D, !CLR, PRE)		2
JK Flip-Flops		JKF	Q = (CLK, !Q J + Q K, –, –)	1	
		JKF1B	Q = (!CLK, !Q J + Q K, –, –)	1	
		JKF2A	Q = (CLK, !Q J + Q K, !CLR, –)	1	
		JKF2B	Q = (!CLK, !Q J + Q K, !CLR, –)	1	
		JKF2C	Q = (CLK, !Q J + Q K, CLR, –)	1	1
		JKF2D	Q = (!CLK, !Q J + Q K, CLR, –)	1	1
T-type Flip-Flops		TF1A	Q = (CLK, T !Q + !T Q, !CLR, –)	1	
		TF1B	Q = (!CLK, T !Q + !T Q, !CLR, –)	1	
Data Latch		DL1	Q = (G, D, –, –)	1	
		DL1A	QN = !(G, D, –, –)	1	
		DL1B	Q = (!G, D, –, –)	1	
		DL1C	QN = !(!G, D, –, –)	1	
		DL2A	Q = (G, D, !CLR, PRE)		2
		DL2B	QN = !(!G, D, CLR, PRE)		2
		DL2C	Q = (!G, D, !CLR, PRE)		2
		DL2D	QN = !(G, D, CLR, !PRE)		2

ACT 2 Macro Library

Non-Combinable Hard Macros (continued)

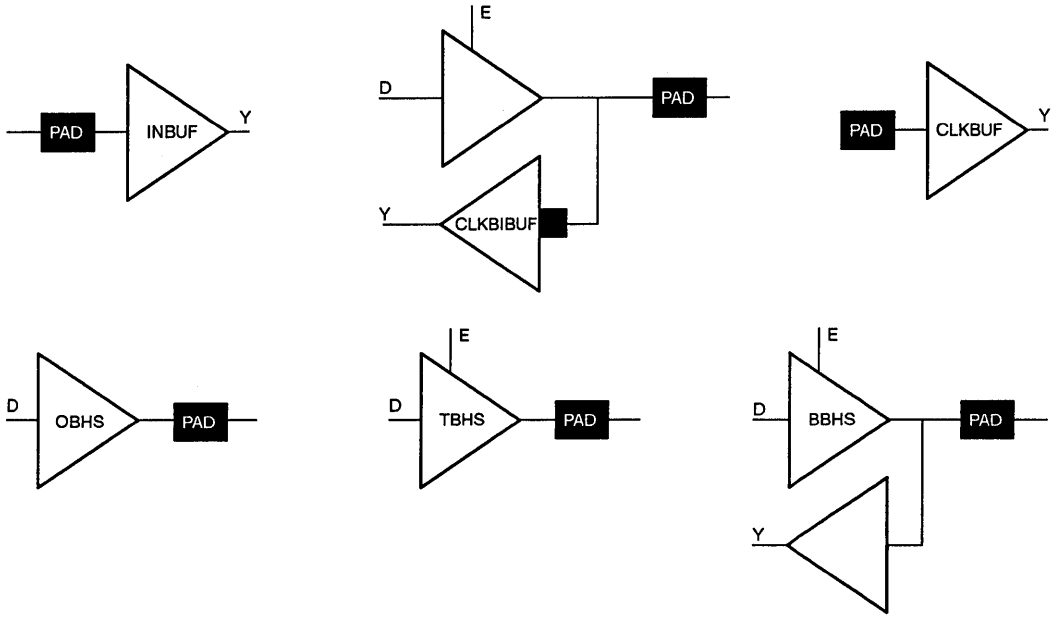
Function	Description	Macro Name	Equation(s)	No. of Modules	
				Seq.	Comb.
Data latch (continued)	with clear	DLC	Q = (G, D, !CLR, -)	1	
		DLC1	Q = (G, D, CLR, -)		1
		DLC1A	Q = (!G, D, CLR, -)		1
		DLC1F	QN = !(G, D, CLR, -)		1
		DLC1G	QN = !(!G, D, CLR, -)		1
		DLCA	Q = (!G, D, !CLR, -)	1	
	with enable	DLE	Q = (G, Q !E + D E, -, -)	1	
		DLE1D	QN = !(!G, !E !D + E QN, -, -)	1	
		DLE2A	Q = (!G, Q !E + D E, CLR, -)	1	1
		DLE2B	Q = (!G, D !E + Q E, !CLR, -)	1	
		DLE2C	Q = (!G, !E D + Q E, CLR, -)		1
		DLE3A	Q = (!G, E D + Q !E, -, PRE)		2
		DLE3B	Q = (!G, !E D + Q E, -, PRE)		1
		DLE3C	Q = (!G, !E D + Q E, -, !PRE)		1
		DLEA	Q = (G, Q E + D !E, -, -)	1	
		DLEB	Q = (!G, Q !E + D E, -, -)	1	
		DLEC	Q = (!G, Q E + D !E, -, -)	1	
	with multiplexed data	DLM	Q = (G, A !S + B S, -, -)	1	
		DLM2A	Q = (!G, A !S + B S, CLR, -)	1	1
		DLM3	Q = (G, D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1, -, -)	1	
		DLM3A	Q = (!G, D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1, -, -)	1	
		DLMA	Q = (!G, A !S + B S, -, -)	1	
	with multiplexed data and enable	DLME1A	Q = (!G, A !S !E + B S !E + E Q, -, -)	1	
	with preset	DLP1	Q = (G, D, -, PRE)		1
		DLP1A	Q = (!G, D, -, PRE)		1
		DLP1B	Q = (G, D, -, !PRE)		1
		DLP1C	Q = (!G, D, -, PRE)		1
		DLP1D	QN = !(G, D, -, !PRE)	1	
		DLP1E	QN = !(!G, D, -, !PRE)	1	
Clock Net Interface		CLKINT		clock modules = 1	
Tie-Off		VCC		modules = 0	
		GND		modules = 0	

ACT 2 Macro Library

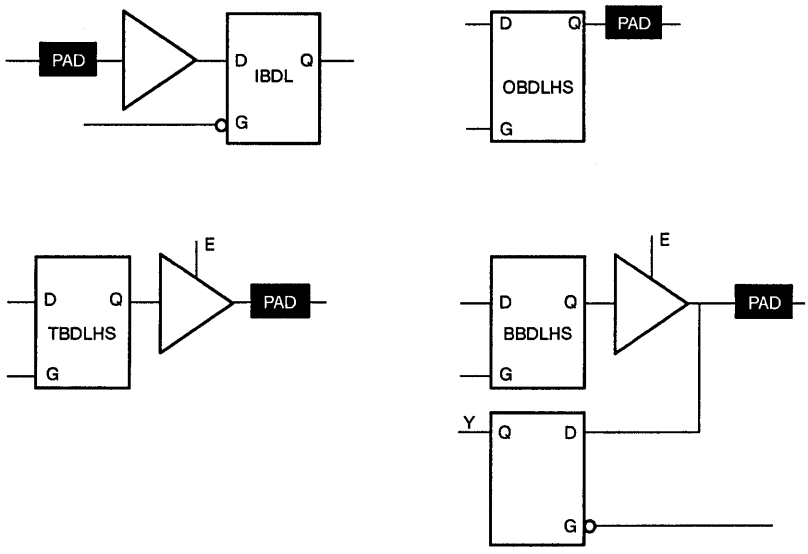
Hard Macro Symbols

I/O Buffers

(I/O Module Count = 1)



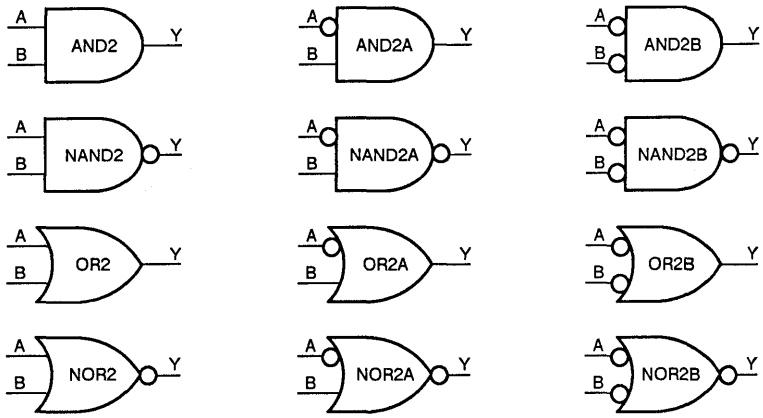
I/O Buffers with Latches



ACT 2 Macro Library

2-Input Gates

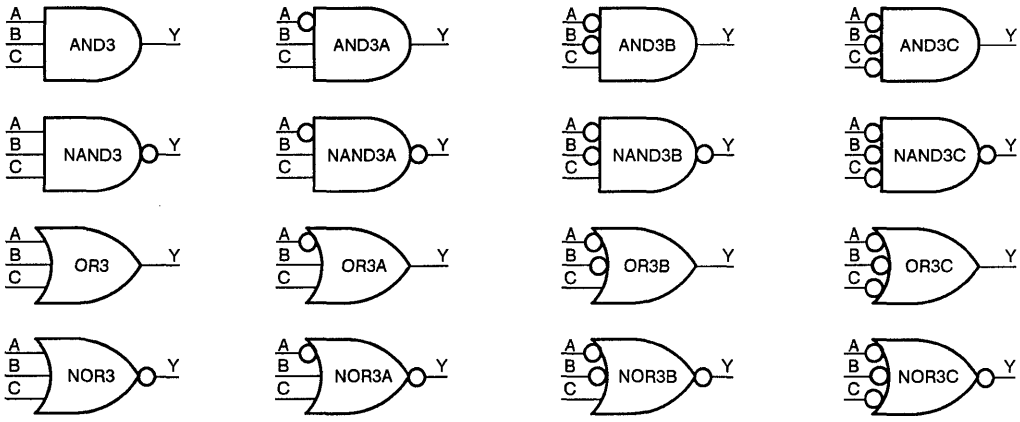
(Module Count = 1)



1

3-Input Gates

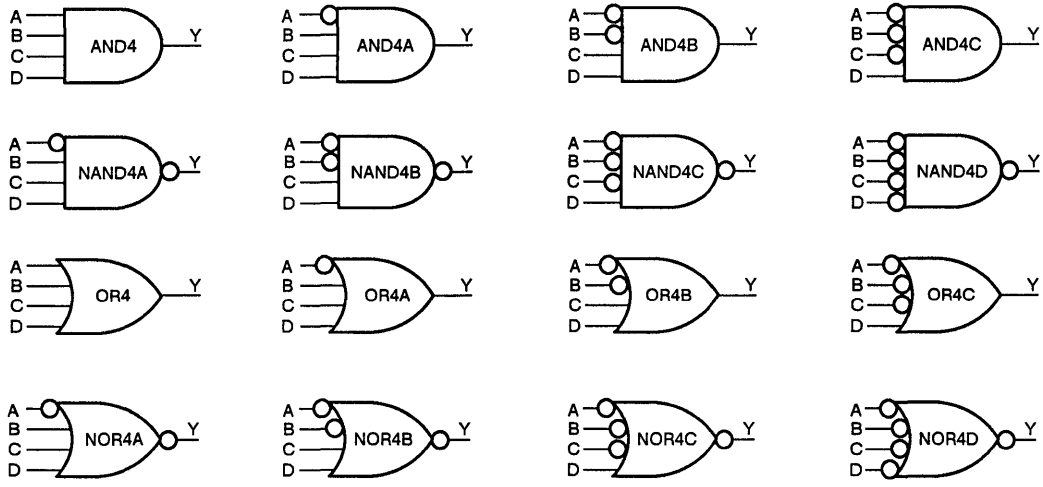
(Module Count = 1)



ACT 2 Macro Library

4-Input Gates

(Module Count = 1)

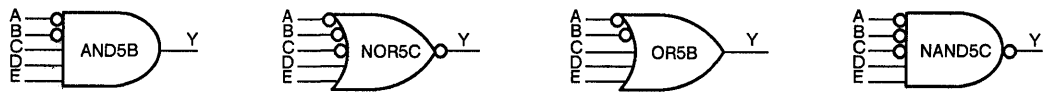


(Module Count = 2)

▲ Indicates extra delay input

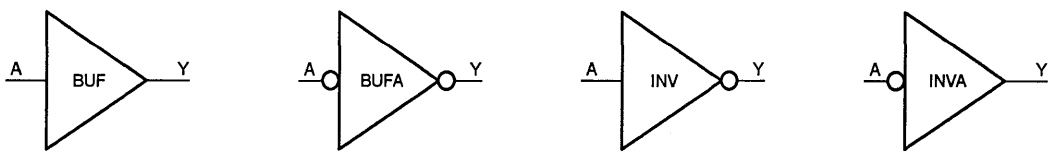
5-Input Gates

(Module Count = 1)



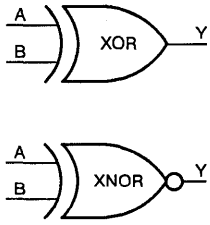
Buffers

(Module Count = 1)

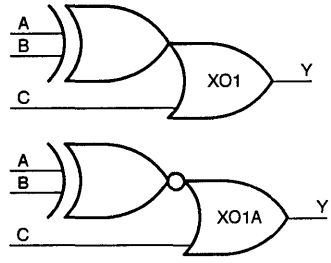


ACT 2 Macro Library

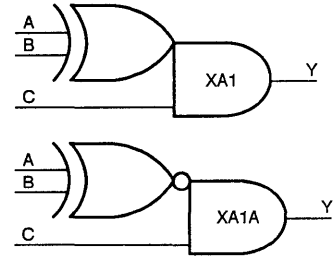
XOR Gates (Module Count = 1)



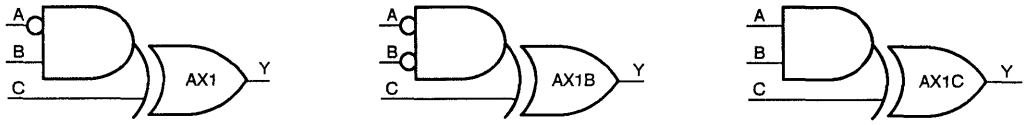
XOR-OR Gates (Module Count = 1)



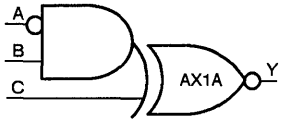
XOR-AND Gates (Module Count = 1)



AND-XOR Gates
(Module Count = 1)



(Module Count = 2)

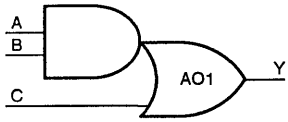


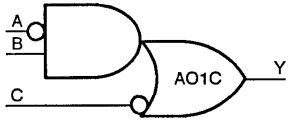
1

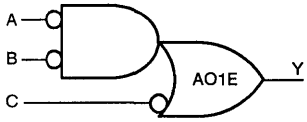
ACT 2 Macro Library

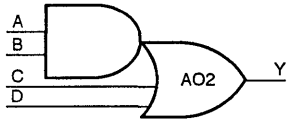
AND-OR Gates

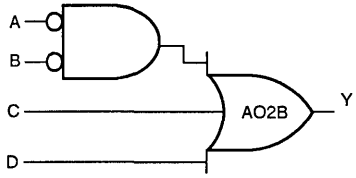
(Module Count = 1)

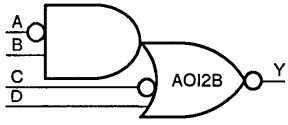


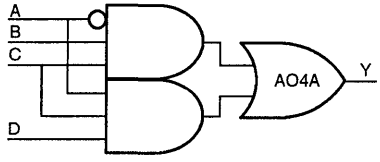


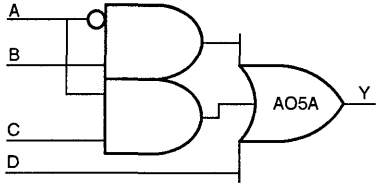


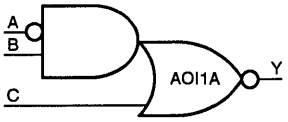


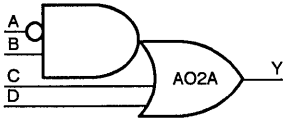


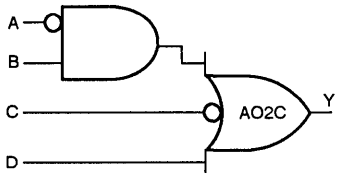


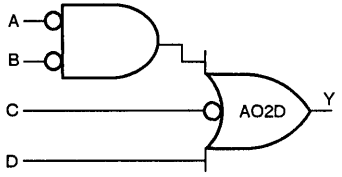


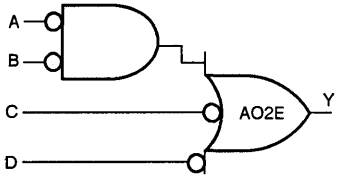


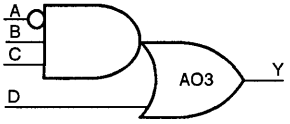


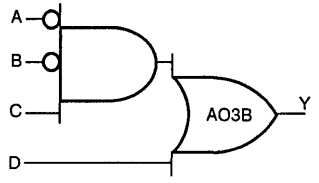


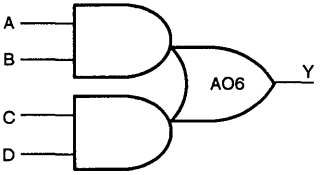


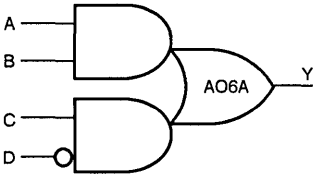


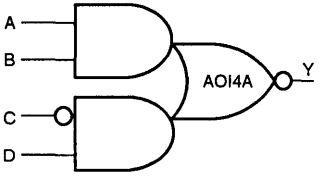


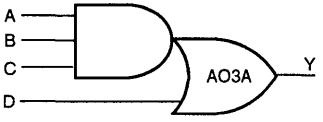


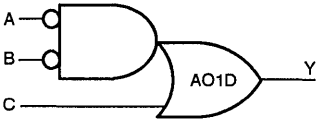


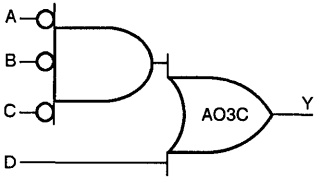






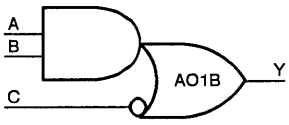


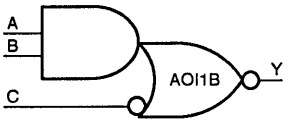


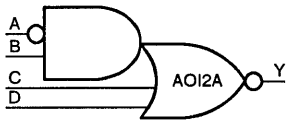


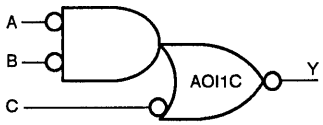
ACT 2 Macro Library

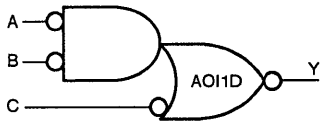
AND-OR Gates, continued
(Module Count = 1)

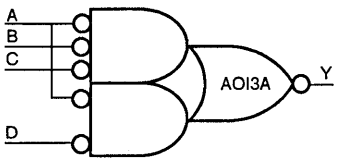


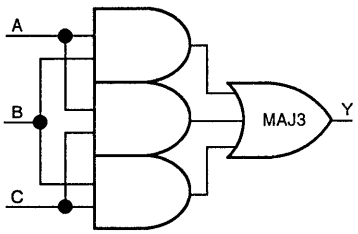


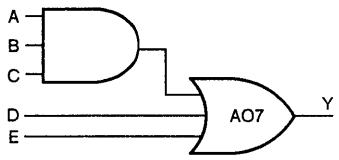


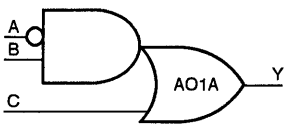


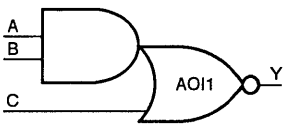




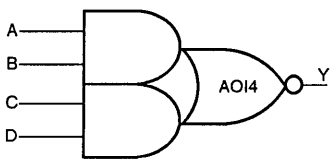


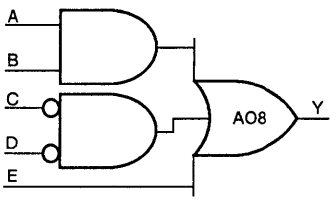


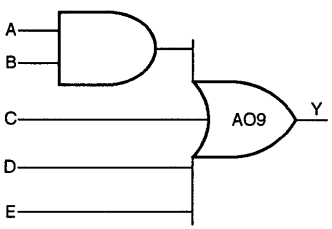


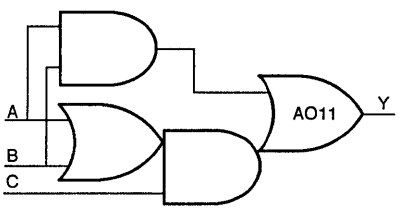


(Module Count = 2)









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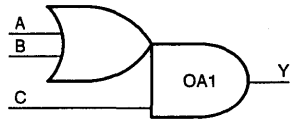
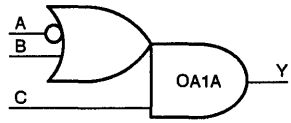
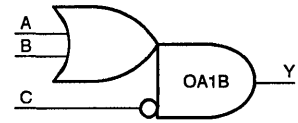
ACT 2 Macro Library

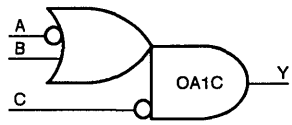
OR-AND Gates

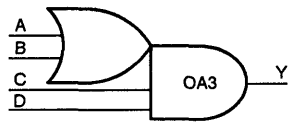
(Module Count = 1)

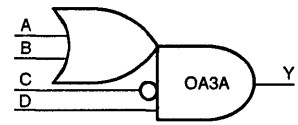


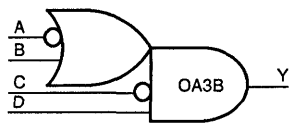


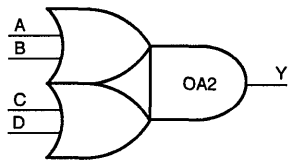


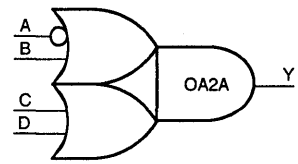


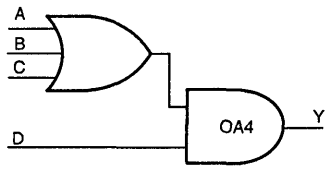


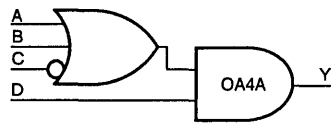


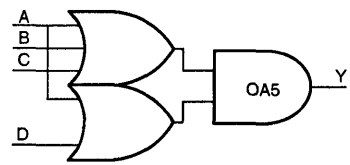


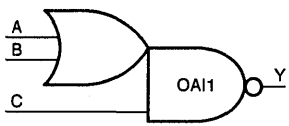


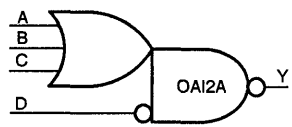


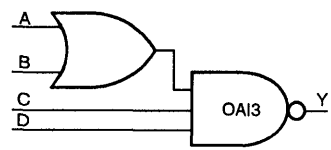


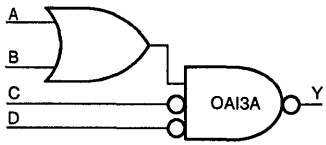


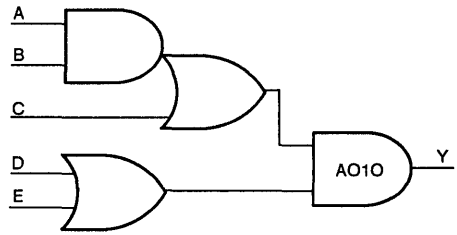








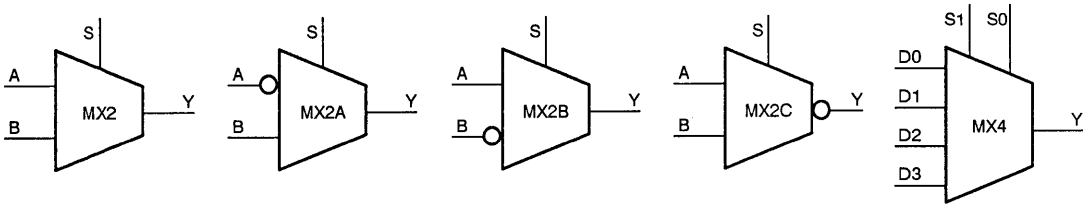




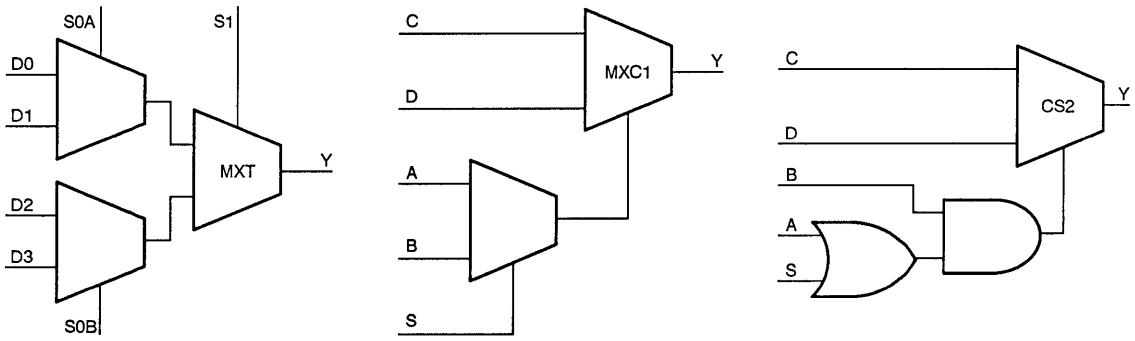
ACT 2 Macro Library

Multiplexors

Module Count = 1)

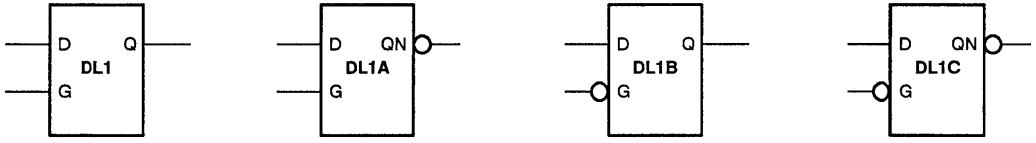


Module Count = 2)



Latches

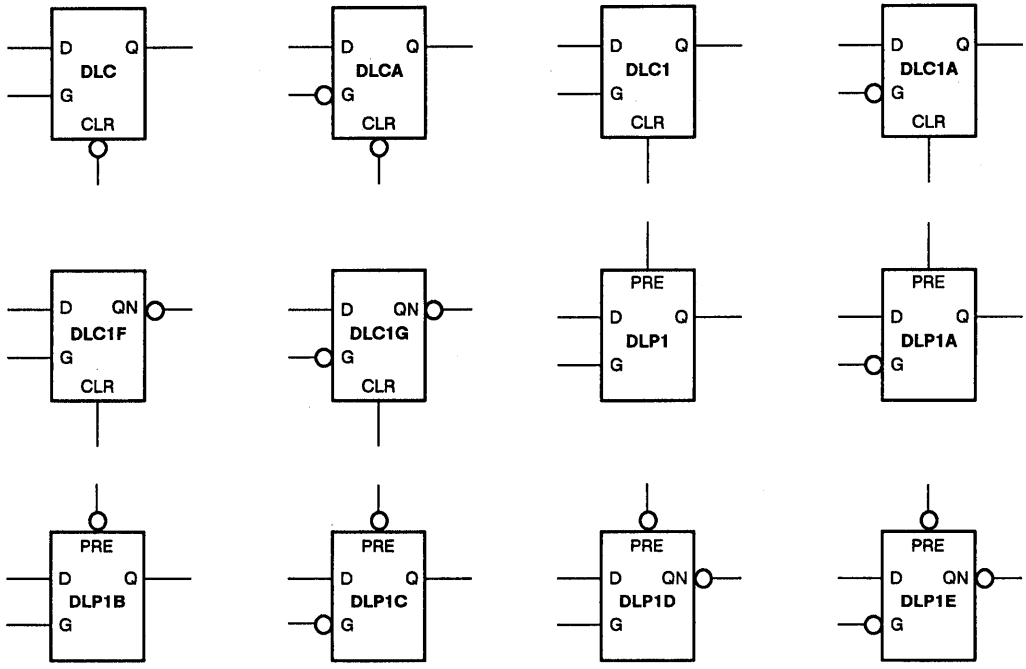
Module Count = 1)



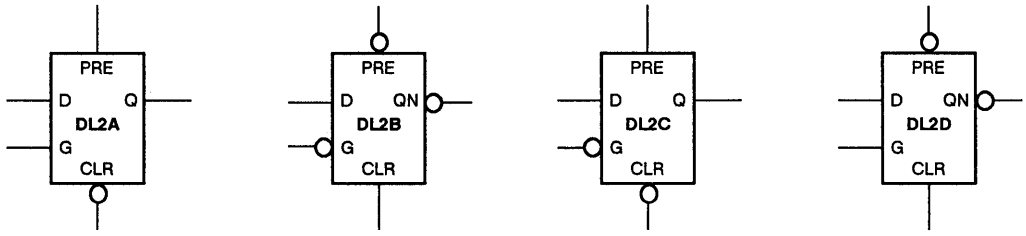
ACT 2 Macro Library

D-Latches with Clear

(Module Count = 1)



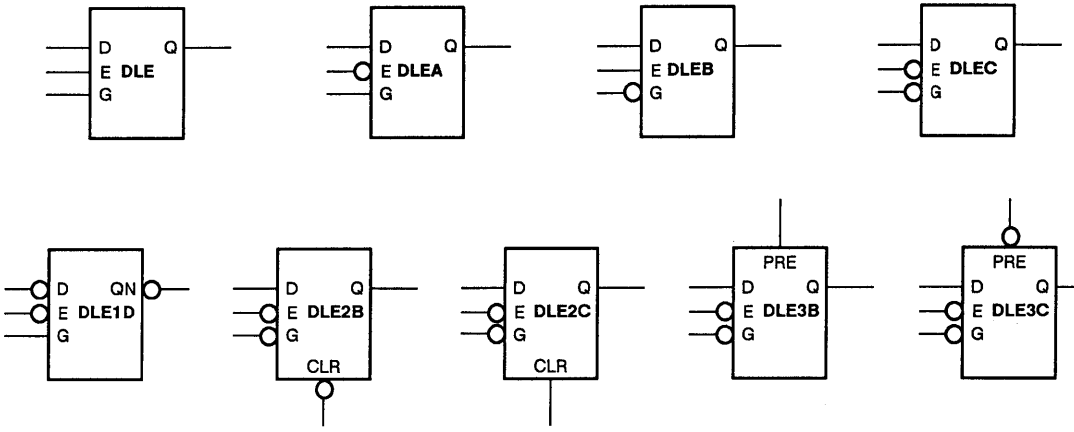
(Module Count = 2)



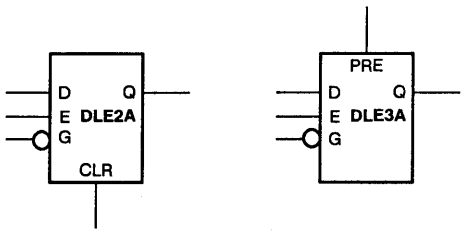
ACT 2 Macro Library

D-Latches with Enable

(Module Count = 1)

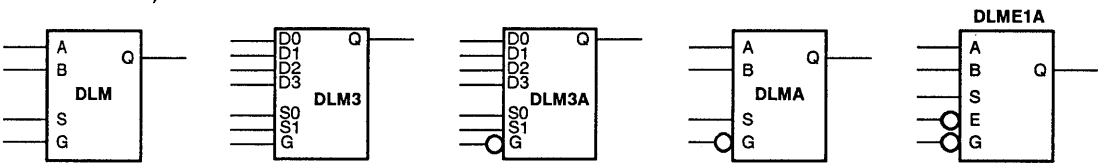


(Module Count = 2)

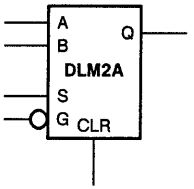


Mux Latches

(Module Count = 1)



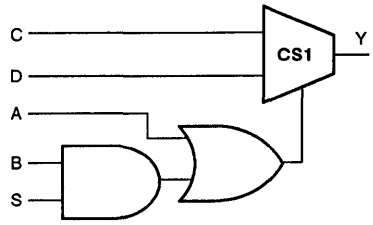
(Module Count = 2)

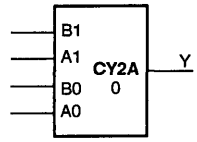


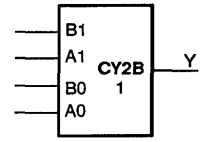
ACT 2 Macro Library

Adders

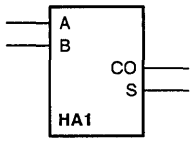
(Module Count = 1)

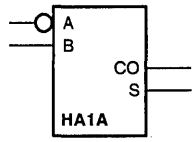


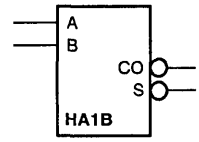


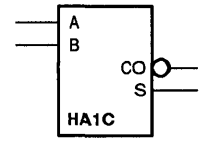


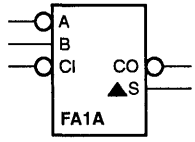
(Module Count = 2)

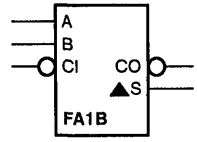


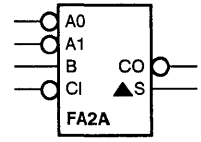








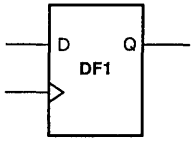


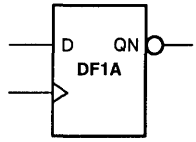


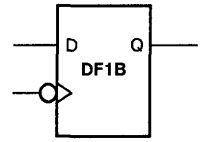
Macros FA1A, FA1B, and FA2A have two level delays from the inputs to the S outputs, as indicated by the▲

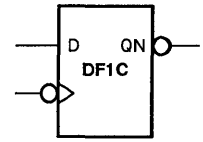
D-Type Flip-Flops

(Module Count = 1)





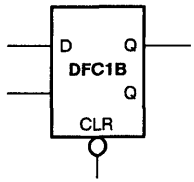


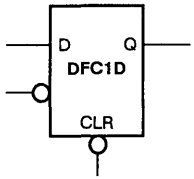


ACT 2 Macro Library

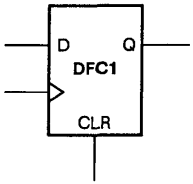
D-Type Flip-Flops with Clear

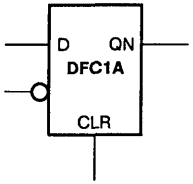
(Module Count = 1)

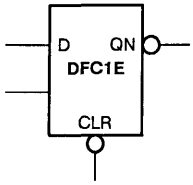


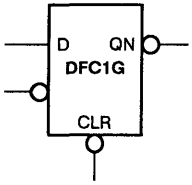


(Module Count = 2)



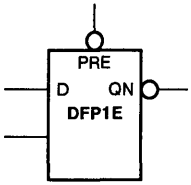


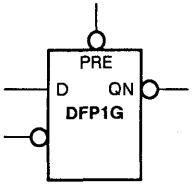




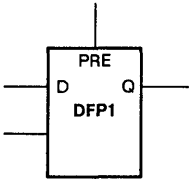
D-Type Flip-Flops with Preset

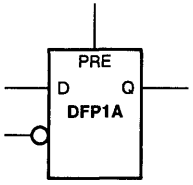
(Module Count = 1)

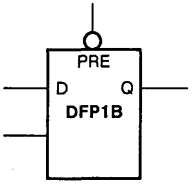


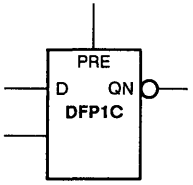


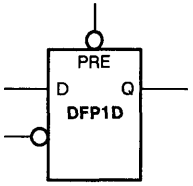
(Module Count = 2)

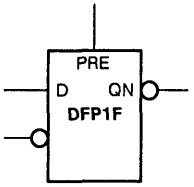






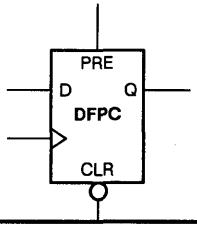


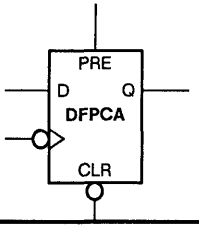




D-Type Flip-Flops with Preset and Clear

(Module Count = 2)

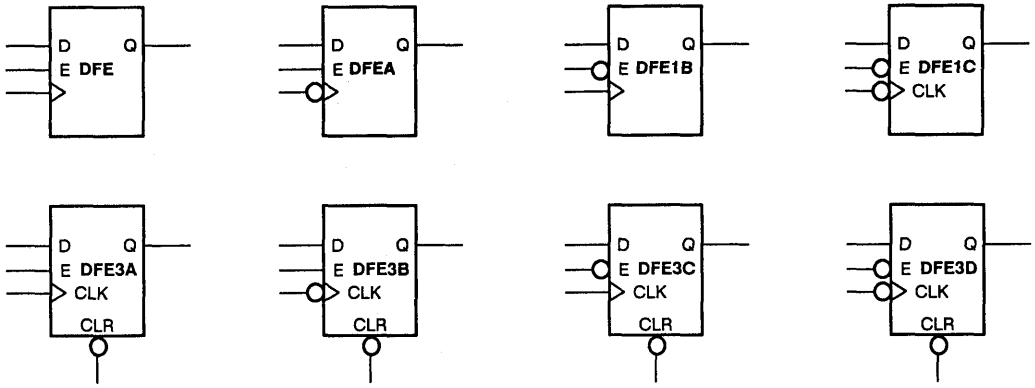




ACT 2 Macro Library

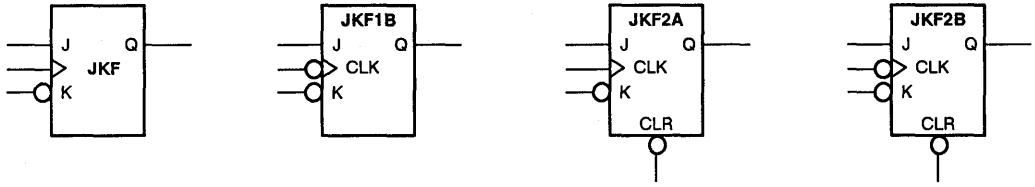
D-Type Flip-Flops with Enable

(Module Count = 1)

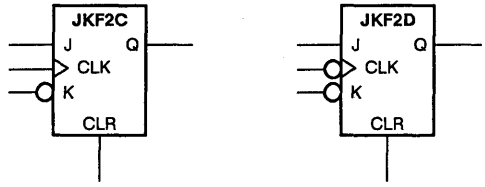


JK Flip-Flops

(Module Count = 1)

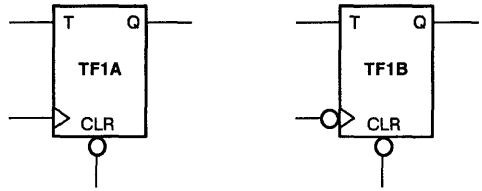


(Module Count = 2)



Toggle Flip-Flops

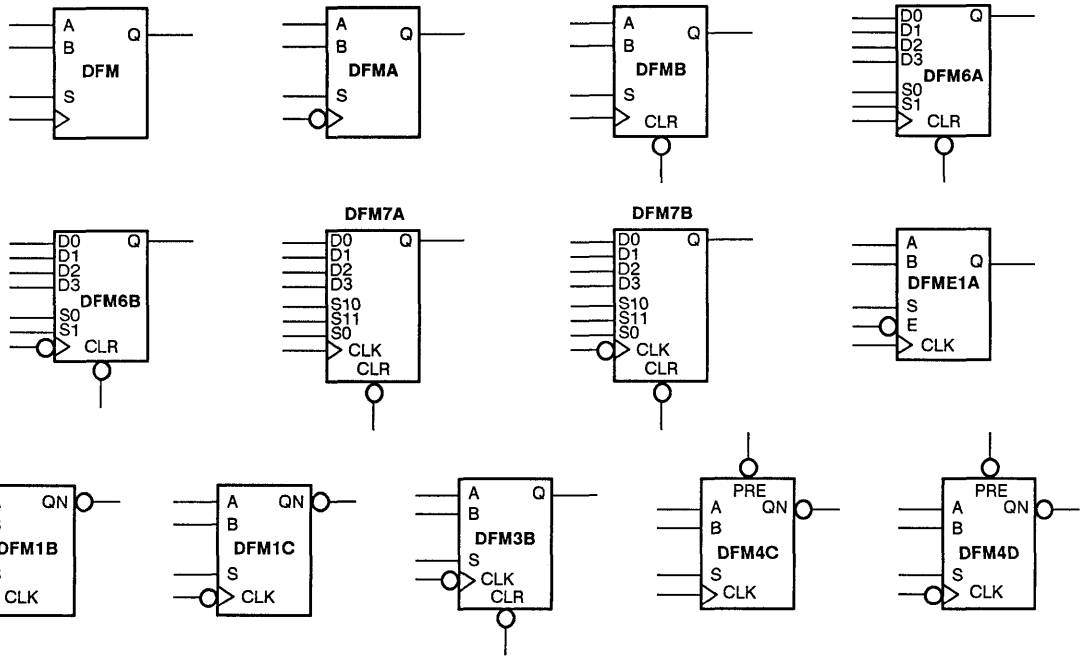
(Module Count = 1)



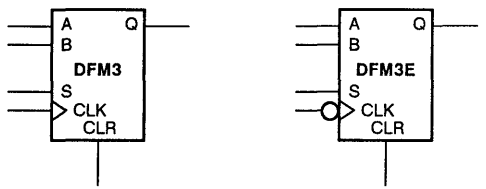
ACT 2 Macro Library

Mux Flip-Flops

(Module Count = 1)

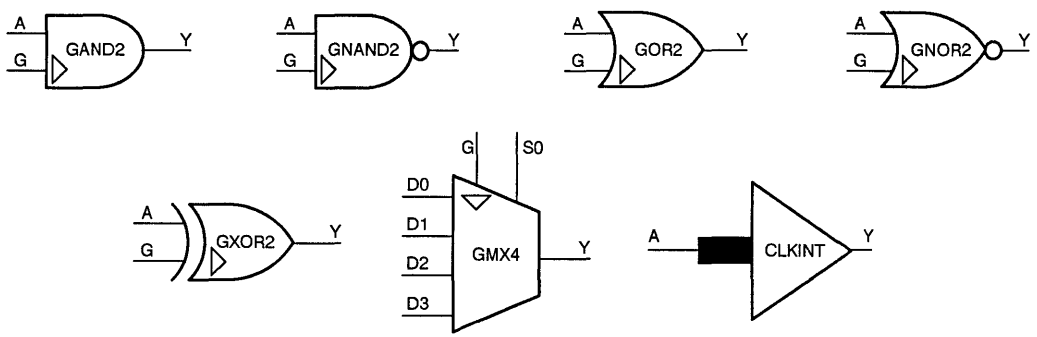


(Module Count = 2)



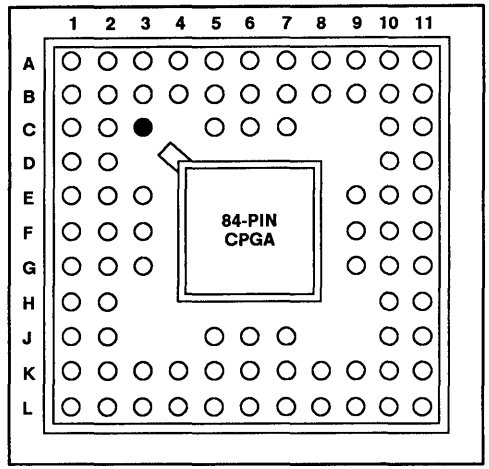
CLKBUF Interface Macros

(Module Count = 1)



▷ Indicates clock input for connection to the global clock networks.

Package Pin Assignments: 84-Pin CPGA (Top View)

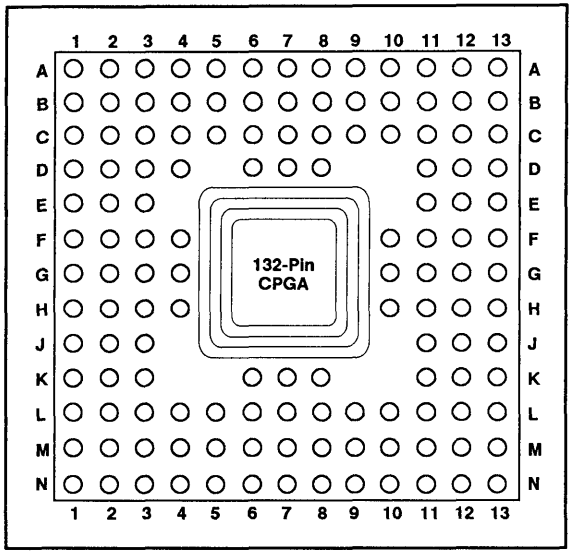


Signal	A1010-Series Devices	A1020-Series Devices
$\overline{PRA}$	A11	A11
$\overline{PRB}$	B10	B10
MODE	E11	E11
SDI	B11	B11
DCLK	C10	C10
V_{PP}	K2	K2
CLK or I/O	F9	F9
GND	B7, E2, E3, K5, F10, G10	B7, E2, E3, K5, F10, G10
V_{CC}	B5, F1, G2, K7, E9, E10	B5, F1, G2, K7, E9, E10
N/C (No Connection)	B1, B2, C1, C2, K1, J2, L1, J10, K10, K11, C11, D10, D11	B2

Notes:

1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

Package Pin Assignments: 132-Pin CPGA (Top View)

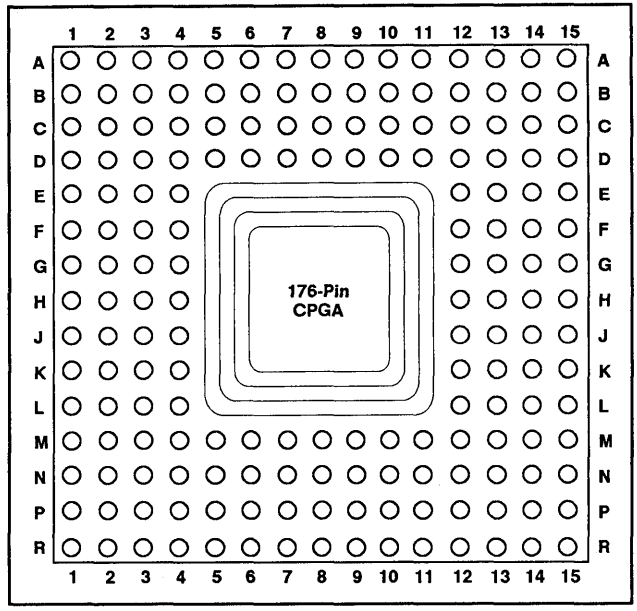


Signal	Pin No.	Location
PRA or I/O	113	B8
PRB or I/O	121	C6
MODE	2	A1
SDI or I/O	101	B12
SDO or I/O	65	N12
DCLK or I/O	132	C3
CLKA or I/O	115	B7
CLKB or I/O	119	B6
GND	9, 10, 26, 27, 41, 58, 59, 73, 74, 92, 93, 107, 108, 125, 126	E3, F4, J2, J3, L5, M9, L9, K12, J11, E12, E11, C9, B9, B5, C5
V_{CC}	18, 19, 49, 50, 83, 84, 116, 117	G3, G2, L7, K7, G10, G11, D7, C7
V_{PP}	82	G13
V_{SV}	17, 85	G4, G12
V_{KS}	81	H13

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

Package Pin Assignments: 176-Pin CPGA
(Top View)

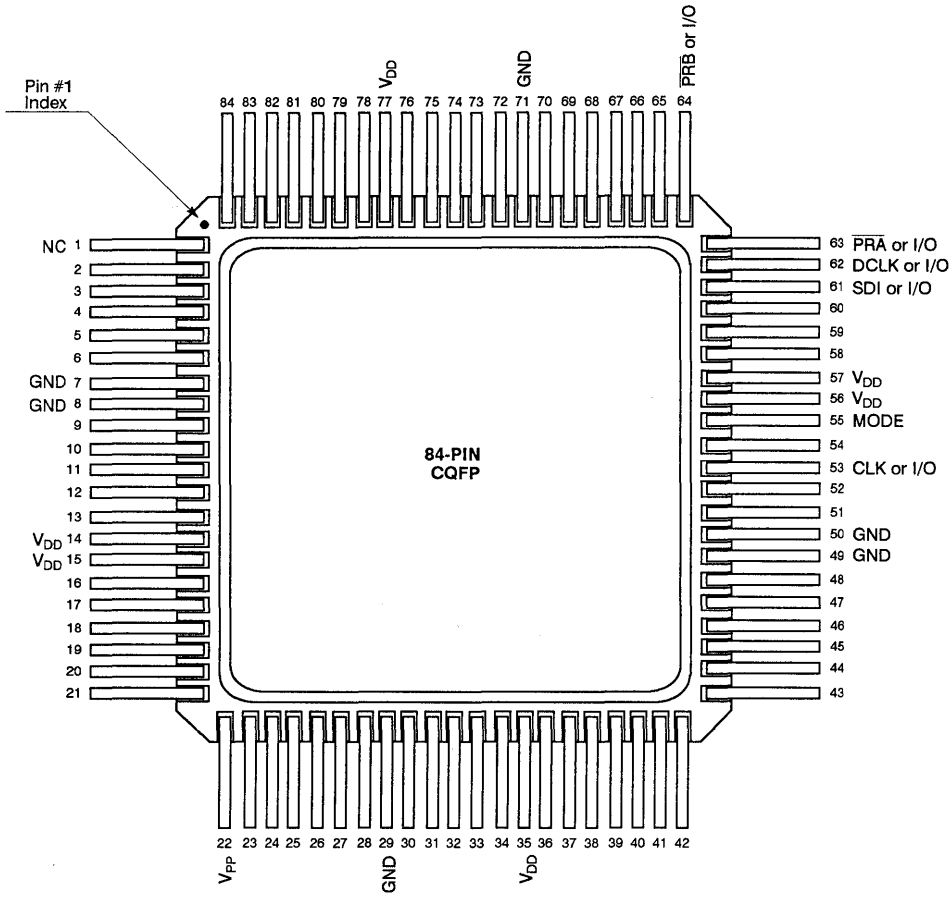


Signal	Pin No.	Location
PRA or I/O	152	C9
PRB or I/O	160	D7
MODE	2	C3
SDI or I/O	135	B14
SDO or I/O	87	P13
DCLK or I/O	175	B3
CLKA or I/O	154	A9
CLKB or I/O	158	B8
GND	1, 8, 18, 23, 33, 38, 45, 57, 67, 77, 89, 101, 106, 111, 121, 126, 133, 145, 156, 165	D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12, K12, J12, H12, F12, E12, D12, D10, C8, D6
V_{CC}	13, 24, 28, 52, 68, 82, 112, 116, 140, 155, 170	F4, H3, J4, M5, N8, M11, H13, G12, D11, D8, D5
V_{PP}	110	J14
V_{SV}	25, 113	H2, H14
V_{KS}	109	J13

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

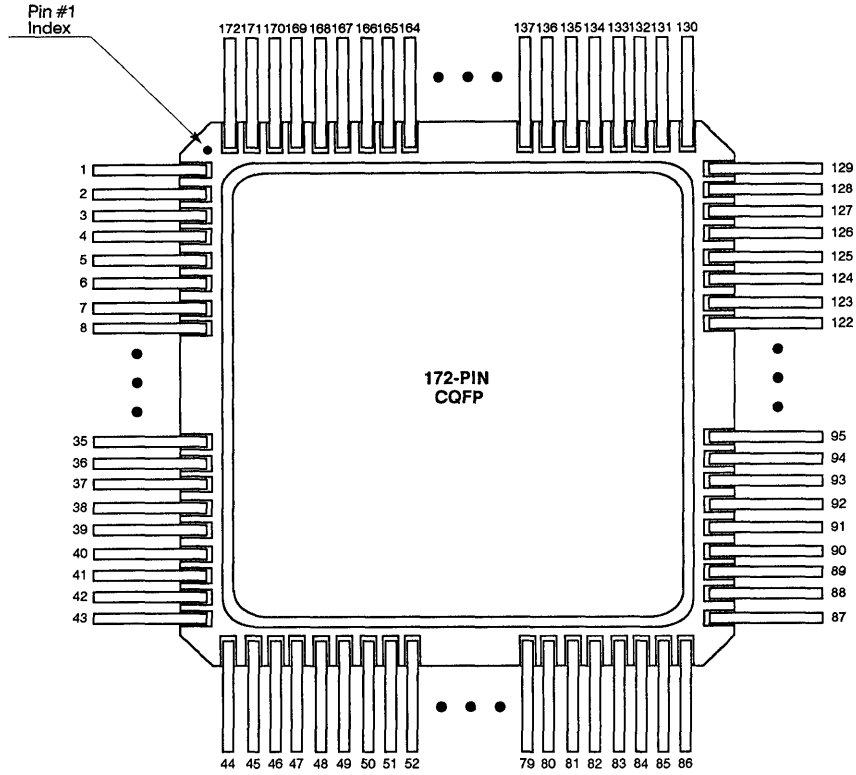
Package Pin Assignments: 84-Pin CQFP (Top View)



Notes:

1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

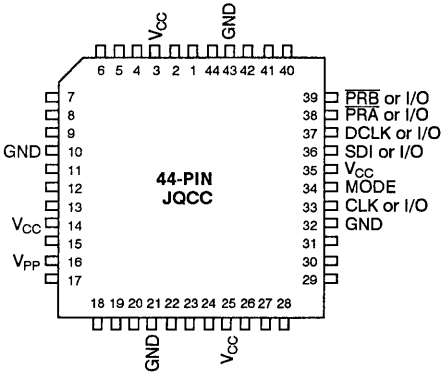
Package Pin Assignments: 172-Pin CQFP
(Top View)

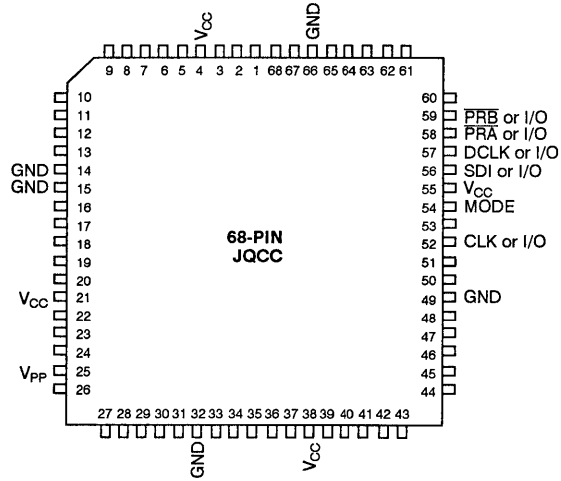


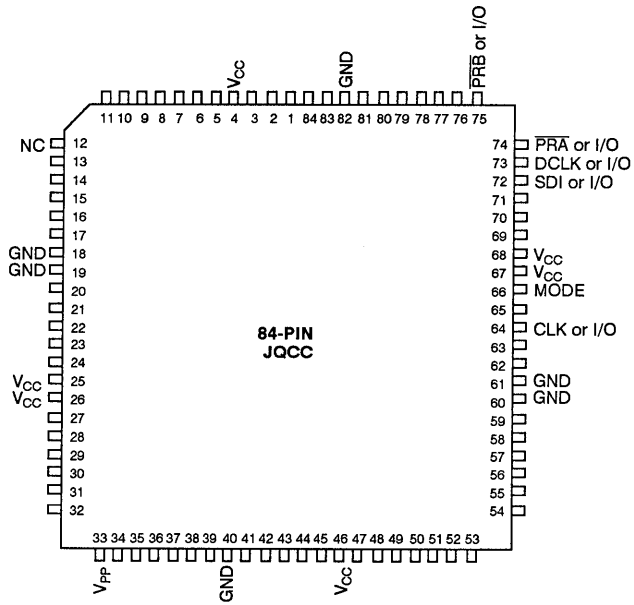
Signal	Pin Number
MODE	1
GND	7, 17, 22, 32, 37, 55, 65, 75, 98, 103, 108, 118, 123, 141, 152, 161
V_{CC}	12, 23 ,27, 50, 66, 80, 109, 113, 136, 151, 166
V_{SV}	24, 110
V_{KS}	106
V_{PP}	107
SDO or I/O	85
SDI or I/O	131
PRA or I/O	148
PRB or I/O	156
CLKA or I/O	150
CLKB or I/O	154
DCLK or I/O	171

Notes:
1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

Package Pin Assignments: 44-Pin, 68-Pin, 84-Pin JQCC



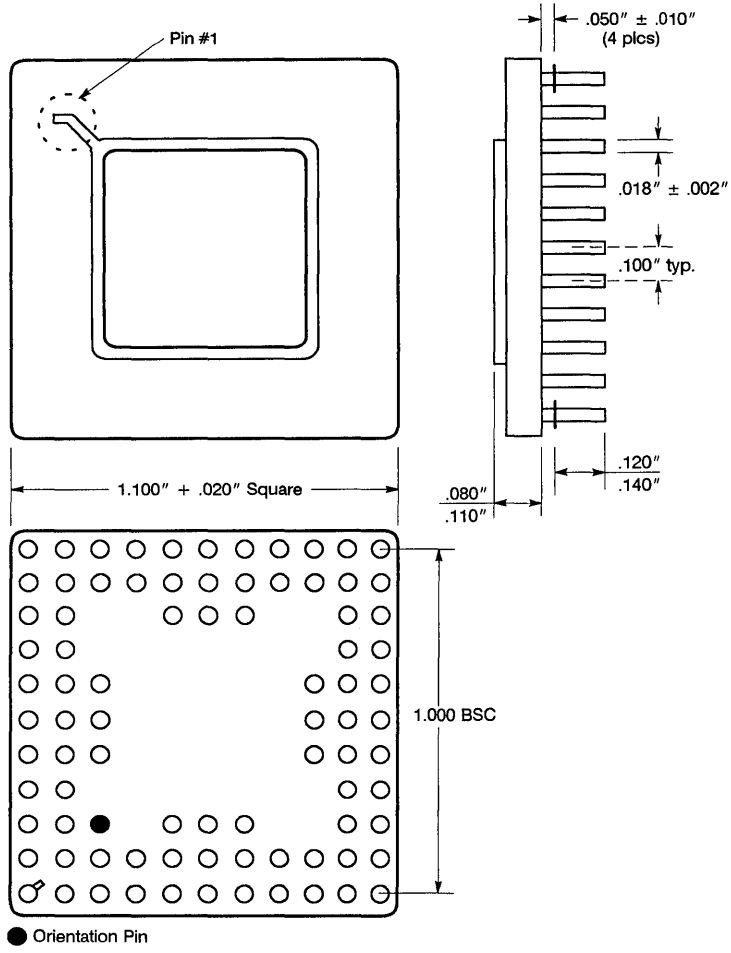




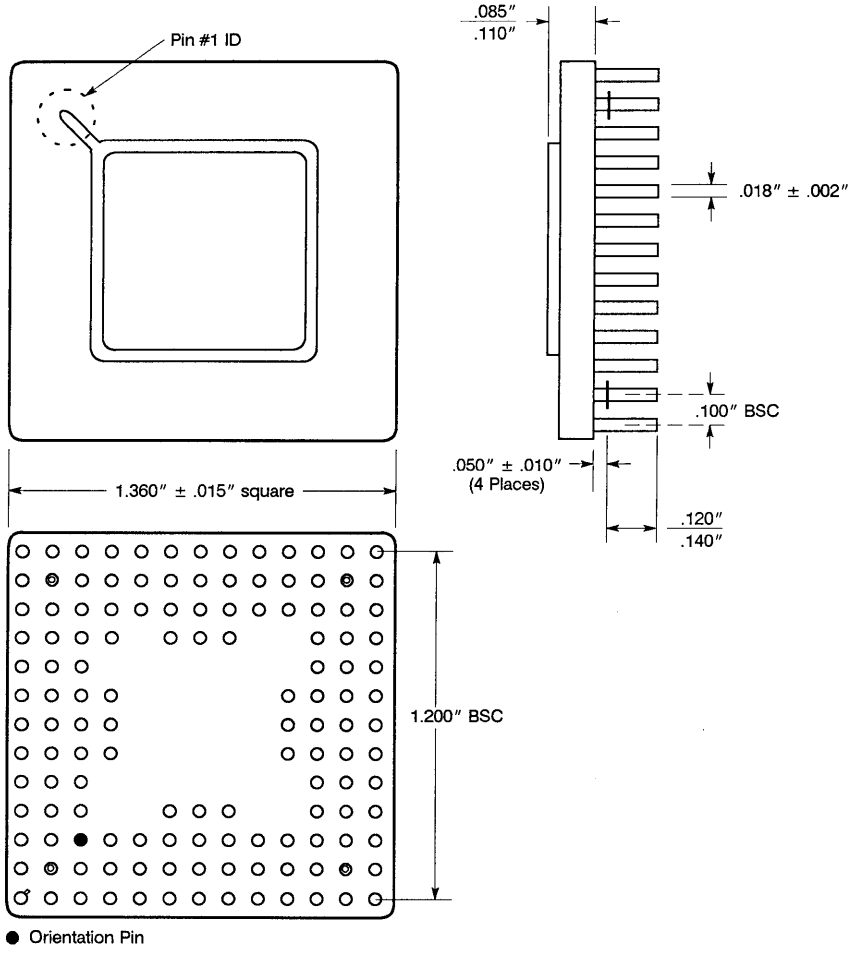
Notes:

1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

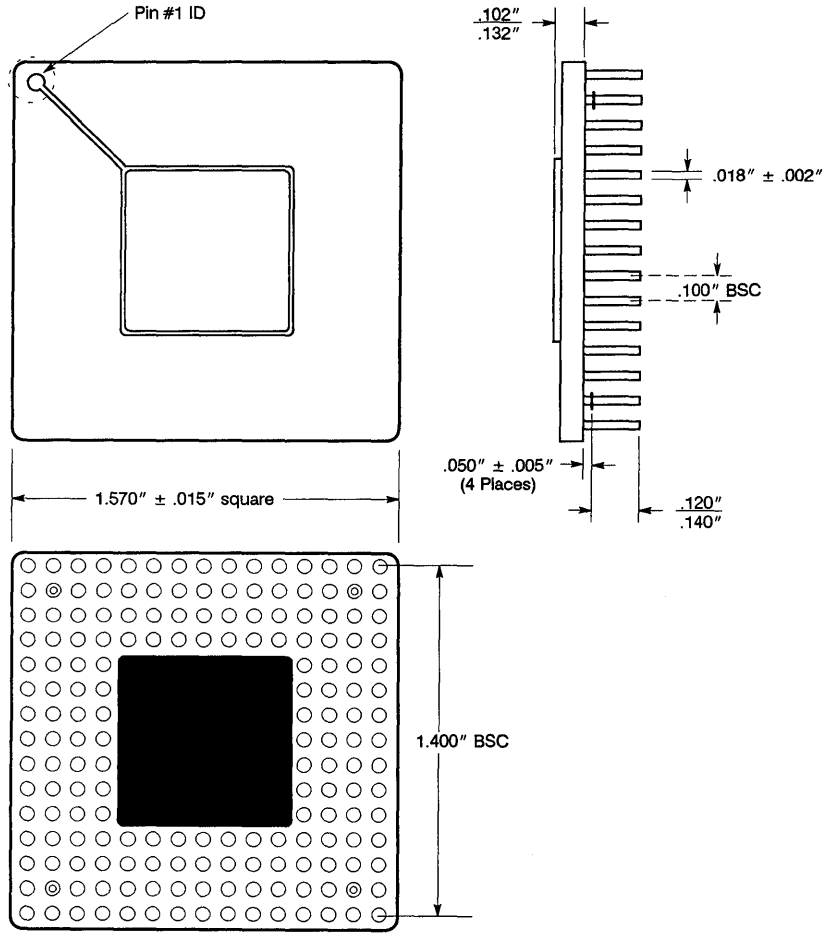
Package Mechanical Details: 84-Pin CPGA



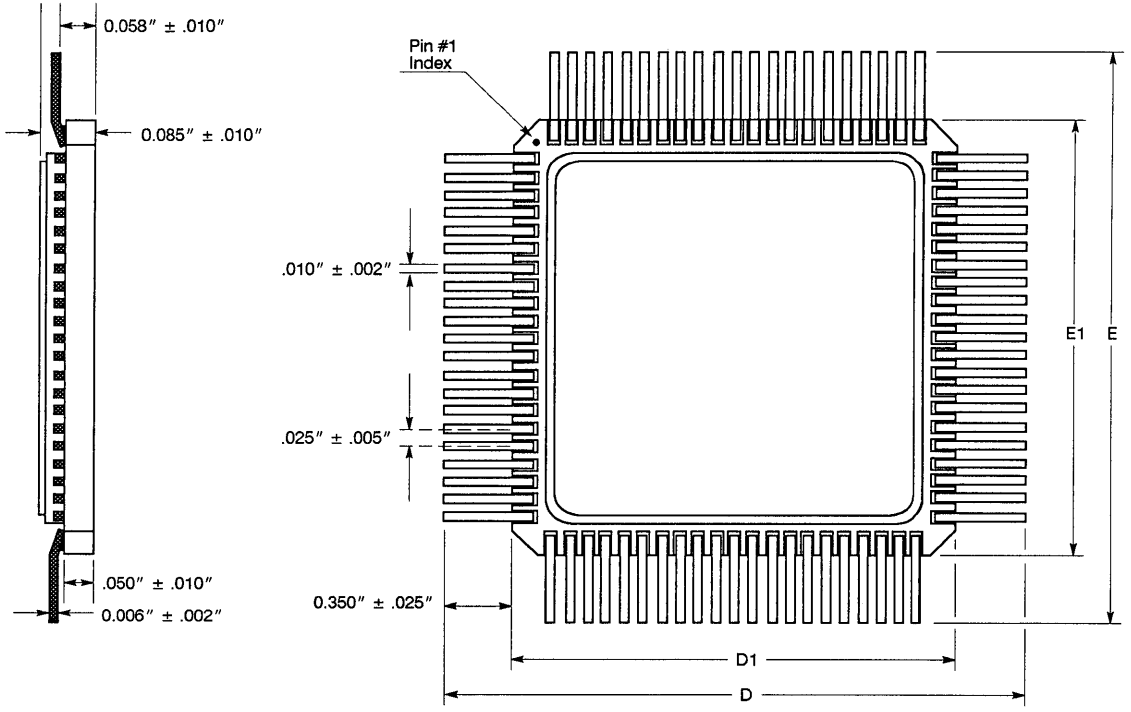
Package Mechanical Details: 132-Pin CPGA



Package Mechanical Details: 176-Pin CPGA

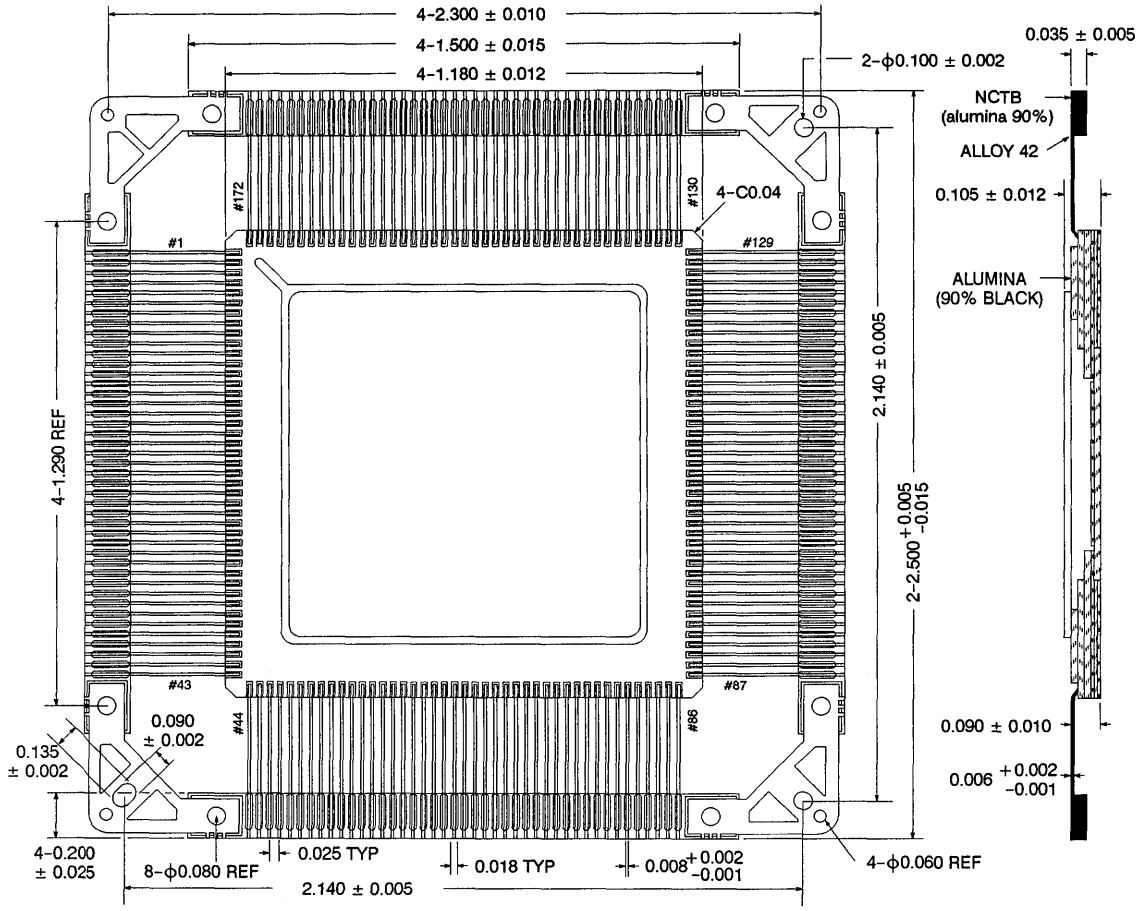


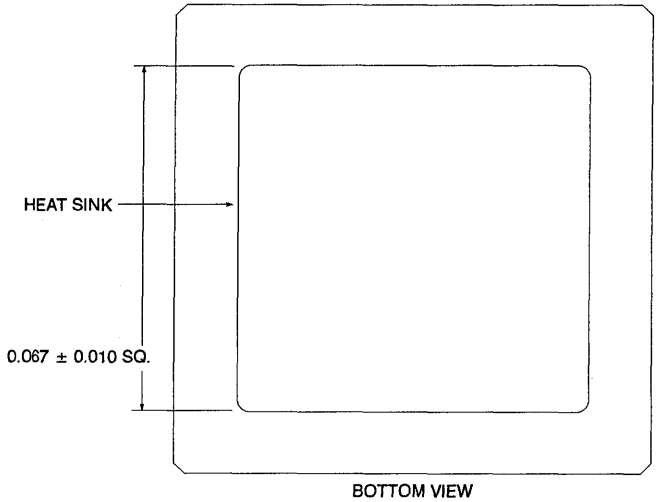
Package Mechanical Details: 84-Pin CQFP



Lead Count	D, E	D1, E1
84	1.350″ ± .030″	0.650″ ± .010″

Package Mechanical Details: 172-Pin CQFP

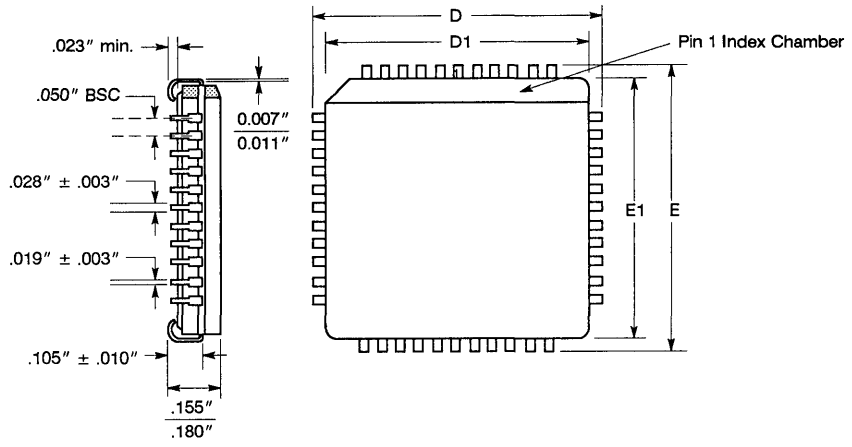




Notes:

1. All exposed metalized areas and leads are gold plated 100 microinches (2.5 μ mm) min. thickness over 80 to 350 microinches 2.0 to 8.9 μ mm) thickness of nickel.
2. Seal ring area is connected to GNDA.
3. Die attach pad is connected to GNDA.
4. GNDQ (4 PLS) is connected to GNDA.
5. Tolerances unless otherwise specified: ±1% N.L.T. ±0.005.

Package Mechanical Details: JQCC



Lead Count	D, E	D1, E1
44	.690″ ± .005″	.650″ ± .008″
68	.990″ ± .005″	.950″ ± .008″
84	1.190″ ± .005″	1.150″ ± .008″

A10M20A Mask Programmed Gate Array

Preliminary

Features

- High Gate Count: 2000 gate array gates (6000 PLD/LCA equivalent gates)
- Pin-for-Pin Compatible with Actel's A1020A FPGA at Lower Cost
- Easy Conversion From FPGA to Mask Programmed Gate Array (MPGA)
- Re-routing Not Required for FPGA to MPGA Conversion
- Automatic Test Generation (ATG) Eliminates Test Vector Generation
- ATG Vectors Provide 100% Test Coverage for all Detectable Faults
- 35–70% Faster than Programmable A1020A FPGA
- Gate Array Architecture Allows Completely Automatic Place and Route
- Short Lead Times to Prototypes and Production
- Low-Power CMOS Technology
- System Level Performance to 50 MHz
- Toggle Rates to 120 MHz
- I/O Drive to 8 mA
- Nonvolatile, Permanent Programming
- Built-In Clock Distribution Network

Product Profile

Device	A10M20A
Capacity	
Gate Array Equivalent Gates	2,000
PLD/LCA Equivalent Gates	6,000
TTL Equivalent Packages	50
20-Pin PAL Equivalent Packages	15
Logic Modules	547
Flip-Flops (maximum)	273
Routing Resources	
Horizontal Tracks/Channel	25
Vertical Tracks/Column	13
User I/Os (maximum)	69
Packages	68-pin PLCC 84-pin PLCC 100-pin PQFP
CMOS Process	1.2 µm

Description

The Actel A10M20A Mask Programmed Gate Array (MPGA) offers a lower cost, faster alternative to the A1020A Field Programmable Gate Array (FPGA). These A10M20A MPGAs are pin-for-pin compatible with the A1020A FPGAs. The devices are manufactured in 1.2 micron, two-level metal CMOS and the Actel PLICE® antifuse is replaced by a metal connection via. Actel's unique architecture offers gate array flexibility and high performance.

Actel's MPGA provides automatic test vector generation and 100% test coverage for all detectable faults. This procedure is automatic. Additional features include an on-chip clock driver with a hard-wired distribution network. The on-chip clock driver provides efficient clock distribution with minimum skew.

The user-definable I/Os can drive TTL and CMOS levels.

The Action Logic System

The MPGA is supported by Actel's Action Logic™ System, which allows logic design to be implemented with minimum effort. The Action Logic System (ALS) interfaces with the resident CAE platform to provide a complete gate array design environment for the ACT 1 MPGA. It allows schematic capture, simulation, fully automatic place and route, timing verification, and device programming. The Action Logic System also provides timing and simulation information for the MPGA device. The Action Logic System is supported on the following platforms: 386/486 PC, and Sun®, HP® and Apollo® workstations. It provides CAE interfaces to the following design environments: Valid™, Viewlogic®, Mentor Graphics™, HP DCS and OrCad™.

The MPGA offers the user the ability to move into volume production much faster than with conventional masked gate arrays. Actel produces prototype devices directly from customer generated design files. The user can employ the Action Logic System to perform all schematic capture, pre-route simulation, place and route, and post-route back-annotated simulation. Since there are no additional routes or simulations needed at the vendor's site, there are no extra CPU charges. This gives the user the opportunity to fully determine the functionality of the device prior to paying any NRE development charges.

Device Structure

The A10M20A MPGA's basic structure is similar to the A1020A FPGA. Logic modules are arranged in horizontal rows separated by horizontal interconnect tracks, with vertical interconnect tracks running over the logic modules. The FPGA has PLICE antifuses, located at the intersection of the horizontal and vertical tracks, which connect its logic module inputs and outputs. During the programming cycle, the software addresses and programs the connections required by the circuit application. The MPGA is designed so that all programmable antifuses are removed.

Antifuses are replaced by low-impedance metal vias. Metal via connections are made according to specific customer designs.

The Actel Logic Module

The Actel Logic Module is an eight-input, one-output logic circuit chosen for its wide range of functions and its efficient use of interconnect routing resources. All of the functions available in the ACT 1 FPGA family are available for the A10M20A device.

The logic module implements the four basic logic functions (NAND, AND, OR, and NOR) in gates of two, three, or four inputs. Each function has many versions, due to different combinations of active-low inputs. The logic module also implements a variety of D-latches, an exclusivity function, AND-ORs and OR-AND relationships. Dedicated hard-wired latches or flip-flops are not required, since latches and flip-flops may be constructed from logic modules, wherever needed in the application.

I/O Buffers

Each I/O pin can be configured as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications.

Device Organization

The MPGA consists of a matrix of logic modules arranged in rows separated by wiring channels. The number of logic modules and routing resources is identical for the A1020A FPGA and the A10M20A MPGA (14 rows by 44 columns, 547 logic modules and 69 I/O modules). The MPGA has ATG peripheral circuits for generating test vectors. Routing channels, which contain 22 horizontal segmented metal tracks, are between the rows of logic modules. Vertical routing is provided by 13 vertical tracks per logic module column. Metal via connections are made between the routing tracks to implement a customer's design.

Automatic Test Generation

ATG test vectors are generated automatically to verify user design and interconnect wiring, with 100% fault coverage. Testing is facilitated by testability structures incorporated in the MPGA logic module.

Greater details concerning the methods used to generate the ATG test vectors can be found in the technical paper entitled "Array Architecture for ATG with 100% Fault Coverage," included in this datasheet.

Device Performance

Temperature, Voltage and Processing Effects

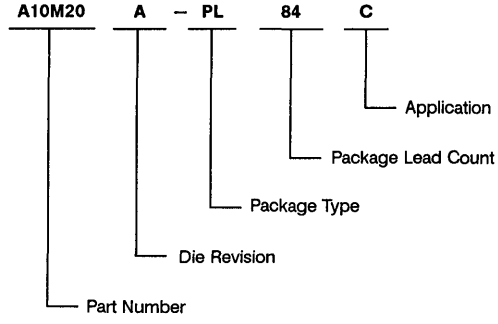
Worst-case delays for the A1020A FPGA device and the A10M20A MPGA device are calculated in the same manner as for conventional masked gate arrays. A typical delay parameter is multiplied by a derating factor to account for temperature, voltage, and processing effects.

The total derating factor from typical to worst-case for the A10M20A MPGA is 1.54 to 1.

Logic Module Size

The logic module size also affects performance. A conventional masked gate array cell with four transistors usually implements only one logic level. In more complex logic modules (similar to the complexity of a gate array macro), of both the A1020A FPGA, and the A10M20A MPGA, it is possible to implement multiple logic levels within a single module. This eliminates inter-level wiring and associated RC delays.

Ordering Information



Product Plan

Package Type	Lead Count	Application
PL	68	C
PL	84	C
PQ	100	C

PL = Plastic Leaded Chip Carrier
PQ = Plastic Quad Flatpack
C = Commercial

Device Resources

Device Series	Logic Modules	Gates	User I/Os		
			68-Pin	84-Pin	100-Pin
A10M20A	547	2000	57	69	69

Absolute Maximum Ratings

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	-0.5 to +7.0	Volts
V_I	Input Voltage	-0.5 to V_{CC} +0.5	Volts
V_O	Output Voltage	-0.5 to V_{CC} +0.5	Volts
I_{IK}	Input Clamp Current	±20	mA
I_{OK}	Output Clamp Current	±20	mA
I_{OK}	Continuous Output Current	±25	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.

Recommended Operating Conditions

Parameter	Commercial	Units
Temperature Range[1]	0 to +70	°C
Power Supply Tolerance	±5	%V_{CC}

Note:

1. Ambient temperature (T_A).

Power Dissipation

The following formula is used to calculate total device dissipation.

Total Device Power (mW) = (0.067 x N x F1) + (0.028 x M x F2) + (0.80 x P x F3)

Where:

F1 = Average logic module switching rate in MHz.

F2 = CLKBUF macro switching rate in MHz.

F3 = Average I/O module switching rate in MHz.

M = Number of logic modules connected to the CLKBUF macro.

N = Total number of logic modules used in the design (including M).

P = Number of outputs loaded with 50 pF.

The average switching rate of logic modules and I/O modules is some fraction of the device operating frequency (usually CLKBUF). Logic modules and I/O modules switch states (from low-to-high or from high-to-low) only if the input data changes when the module is enabled. A conservative estimate for average logic module and I/O module switching rates (variables F1 and F3, respectively) is 10% of device clock driver frequency.

If the CLKBUF macro is not used in the design, eliminate the second term (including F2 and M variables) from the formula.

Sample A10M20A Power Dissipation Calculation

This sample design uses 85% of available logic modules on the A10M20A-series device (.85 x 547 = 465 logic modules). The design contains 104 flip-flops (208 logic modules). The design's operating frequency is 16 MHz. The CLKBUF macro drives the clock network. Logic modules and I/O modules switch states at approximately 10% of the clock frequency rate (.10 x 16 MHz = 1.6 MHz). Sixteen outputs are loaded with 50 pF.

To summarize the design described above: N = 465; M = 208; F2 = 16; F1 = 1.6; F3 = 1.6; P = 16. Total device power can be calculated by substituting these values for variables in the device dissipation formula.

Total device power for this example =

(0.067 x 465 x 1.6) + (0.028 x 208 x 16) + (0.80 x 16 x 1.6) = 164 mW

Electrical Specifications

Parameter		Min.	Max.	Units
V_{OH}[1]	(I_{OH} = -8 mA)	2.4		V
	(I_{OH} = -4 mA)	3.84		V
V_{OH}[1]	(I_{OL} = 8 mA)		0.5	V
	(I_{OL} = 4 mA)		0.33	V
V_{IL}		-0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500	ns
C_{IO} I/O Capacitance[2, 3]			10	pF
Standby Current, I_{CC}[4]			1	mA
Leakage Current[5]		-10	10	µA
I_{OS} Output Short Circuit Current[6]	(V_O = V_{CC})	20	140	mA
	(V_O = GND)	-10	-100	mA

Notes:
1. Only one output tested at a time. V_{CC} = min.
2. Not tested, for information only.
3. Includes worst-case 84-pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.
4. Typical standby current = 300 µA. All outputs unloaded. All inputs = V_{CC} or GND.
5. V_O, V_{IN} = V_{CC} or GND.
6. Only one output tested at a time. Min. at V_{CC} = 4.5 V; Max. at V_{CC} = 5.5 V.

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown in the following table, with two different air flow rates.

Package Type	Pin Count	θjc	θja Still air	θja 300 ft/min.	Units
Plastic J-leaded Chip Carrier	68	13	45	35	°C/W
	84	12	44	33	°C/W
Plastic Flatpack	100	13	55	50	°C/W

Timing Characteristics

Timing is design dependent; actual delay values are determined after place and route of the design using the ALS Timer utility. The following delay values use statistical estimates for wiring delays based on 85% to 90% module utilization. Device utilization above 95% will result in performance degradation.

The A10M20A MPGA is 35–70% faster than the A1020A FPGA because the antifuse is replaced by a metal via connection. The designer needs to be aware of these timing differences when converting from an A1020A FPGA to the A10M20A MPGA. These differences can be quickly analyzed at the customer's facility using ALS.

Logic Module Timing

V_{CC} = 5.0 V; T_A = 25°C; Process = Typical

Single Logic Module Macros (e.g., most gates, latches, multiplexors)[1]

Parameter	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD}	Typical	4.3	4.4	4.5	4.6	4.8	ns

Dual Logic Module Macros (e.g., adders, wide input gates)[1]

Parameter	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD}	Typical	6.9	7.0	7.1	7.3	7.6	ns

Sequential Element Timing Characteristics

Parameter		Fan-Out					Units
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{SU}	Set Up Time, Data Latches	2.7	2.8	3.0	3.3	3.8	ns
t_{SU}	Set Up Time, Flip-Flops	2.8	2.8	2.8	2.8	2.8	ns
t_H	Hold Time	0	0	0	0	0	ns
t_W	Pulse Width, Minimum[2]	6.0	6.3	6.5	7.0	8.0	ns
t_{CQ}	Delay, Typical Net	3.7	3.8	3.9	4.0	4.2	ns
t_{PRE}	Asynchronous Preset to Q	4.3	4.4	4.5	4.6	4.8	ns
t_{CLR}	Asynchronous Clear to Q	4.3	4.4	4.5	4.6	4.8	ns

Notes:

1. Most flip-flops exhibit single module delays.
2. Minimum pulse width, t_W, applies to CLK, PRE, and CLR inputs.

I/O Buffer Timing

PRELIMINARY DATA

V_{CC} = 5.0 V; T_A = 25°C; Process = Typical

INBUF Macros

Parameter	From - To	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PHL}	Pad to Y	2.2	2.3	2.3	2.4	2.6	ns
t_{PLH}	Pad to Y	2.1	2.1	2.2	2.2	2.4	ns

CLKBUF (High Fan-Out Clock Buffer) Macros

Parameter	FO = 40	FO = 160	FO = 320	Units
t_{PLH}	4.1	4.1	4.1	ns
t_{PHL}	4.3	4.3	4.3	ns

Notes:

1. A clock balancing feature is provided to minimize clock skew.
2. There is no limit to the number of loads that may be connected to the CLKBUF macro.

OUTBUF, TRIBUFF & BIBUF Macros

C_L = 50 pF

Parameter	From - To	CMOS	TTL	Units
t_{PHL}	D to Pad	7.0	8.2	ns
t_{PLH}	D to Pad	7.9	6.1	ns
t_{PHZ}	E to Pad	9.1	9.1	ns
t_{PZH}	E to Pad	8.6	6.6	ns
t_{PLZ}	E to Pad	8.9	8.9	ns
t_{PZL}	E to Pad	8.2	9.4	ns

Change in Propagation Delay with Load Capacitance

Parameter	From - To	CMOS	TTL	Units
t_{PHL}	D to Pad	0.05	0.05	ns/pF
t_{PLH}	D to Pad	0.08	0.07	ns/pF
t_{PHZ}	E to Pad	0.11	0.11	ns/pF
t_{PZH}	E to Pad	0.09	0.05	ns/pF
t_{PLZ}	E to Pad	0.11	0.11	ns/pF
t_{PZL}	E to Pad	0.05	0.07	ns/pF

Notes:

1. The BIBUF macro input section exhibits the same delays as the INBUF macro.
2. Load capacitance delay delta can be extrapolated down to 15 pF minimum.

   Example:

   Delay for OUTBUF driving a 100-pF TTL load:

   t_{PHL} = 8.2 + (0.05 x (100–50)) = 10.7 ns

   t_{PLH} = 6.1 + (0.07 x (100–50)) = 9.6 ns

Timing Derating

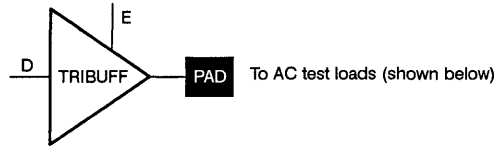
Operating temperature and voltage and device processing condition account for variations in array timing characteristics. These variations are summarized into a derating factor for the A10M20A MPGA typical timing specifications. Derating factors are shown below.

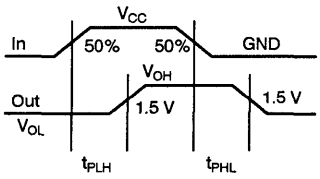
Timing Derating Factor (x typical)

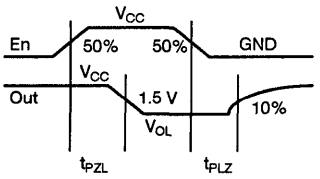
	Commercial	
Device	**Best Case**	**Worst Case**
A10M20A	0.50	1.64

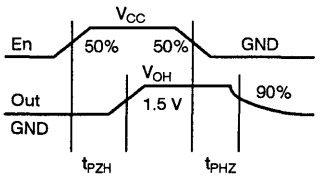
Note:
Best case reflects maximum operating voltage, minimum operating temperature, and best case processing. Worst case reflects minimum operating voltage, maximum operating temperature, and worst case processing. Best case derating is based on sample data only and is not guaranteed.

Output Buffer Delays



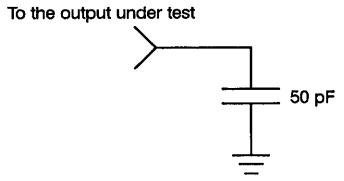




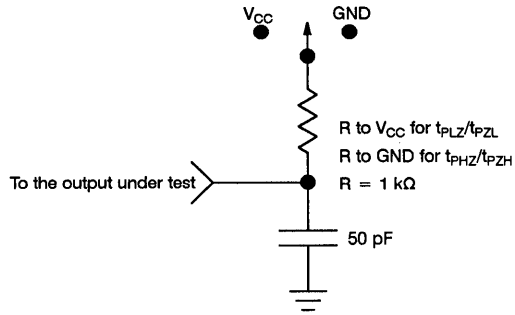


AC Test Loads

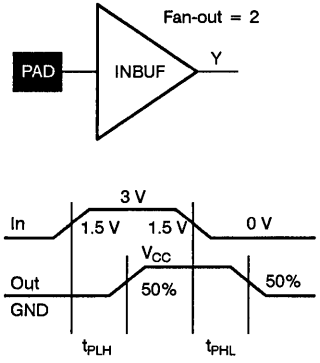
Load 1
(Used to measure propagation delay)



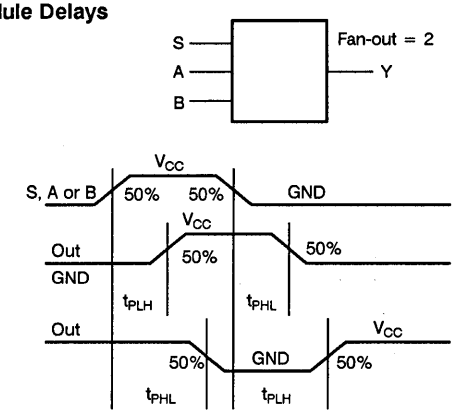
Load 2
(Used to measure propagation delay only for t_{PLZ}/t_{PZL}, t_{PHZ}/t_{PZH})



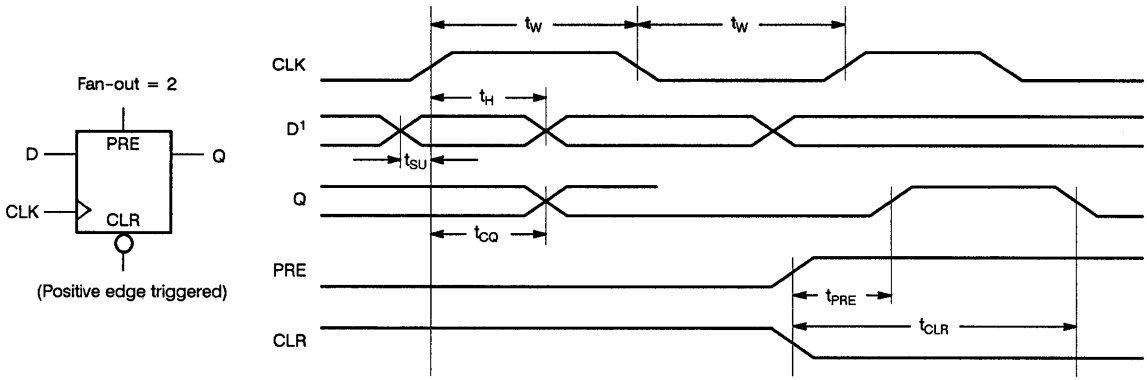
Input Buffer Delays



Module Delays



D-Type Flip-Flop and Clock Delays



Note:

1. For flip-flops with multiplexed inputs, D represents all data functions involving A, B, or S.

Macro Library

Overview

This selection guide describes ACT 1 macros, which are the same for both FPGA and MPGA devices. These macros are building blocks for designing programmable gate arrays with the Action Logic System (ALS) and your CAE interface.

The macros are divided into four categories: I/O Macros, Hard Macros, Soft Macros and TTL Macros.

Equation Statement Elements

Combinatorial Elements

All equations for combinatorial logic elements use the following operators:

Operator	Symbol
AND	See Note 1
NOT	!
OR	+
XOR	^

Notes:

1. A space between the 'A' and 'B' in the equation Y = A B means **A AND B.**
2. Order of operators in decreasing precedence is: NOT, AND, XOR and OR.
3. Signals expressed in bold have a dual module delay.

Sequential Elements

All equations for sequential logic elements use the following formula:

Q = <!> (<!> CLK or G, <data equation>, <!> CLR, <!> PRE)

<!>	Optional Inversion
CLK	Flip-Flop Clock Pin
G	Latch Gate Pin
CLR	Asynchronous Clear Pin
PRE	Asynchronous Preset Pin

MPGA Macro Selections

I/O Macros

Macro Name	No. of Modules I/O	No. of Modules Clock	Description
INBUF	1		Input
BIBUF	1		Bidirectional
CLKBUF	1	1	Input for Dedicated Clock Network
TRIBUF	1		Three State Output
OUTBUF	1		Output

TTL Macros

Macro Name	Description	Logic Levels	Modules Required
TA138	3 to 8 decoder with enable and active low outputs	2	12
TA139	2 to 4 decoder with enable and active low outputs	1	4
TA151	8 to 1 multiplexor with enable and active low outputs	3	5
TA153	4 to 1 multiplexor Equations: X = (C0 !B !A) + (C1 !B A) + (C2 B !A) + (C3 B A) Y = (!EN X)	2	2
TA157	2 to 1 multiplexor Equation: Y = (!EN !S A) + (!EN S B)	1	1
TA161	4-bit binary counter with clear	3	22
TA164	8-bit shift register with serial in/parallel out	1	18
TA169	4-bit up/down counter	6	25
TA194	4-bit shift register	1	14
TA195	4-bit shift register	1	11
TA269	8-bit up/down binary counter	8	50
TA273	Octal register with clear	1	18
TA280	Parity generator and checker	4	9
TA377	Octel register with enable	1	16

Soft Macros

Function	Description	Macro Name	Logic Levels	Modules Required
Adders	1-bit adder	FA1	3	3
	8-bit adder	FADD8	4	37
	12-bit adder	FADD12	5	58
	16-bit adder	FADD16	5	79
	24-bit adder	FADD24	6	120
	32-bit adder	FADD32	7	160
Comparators	4-bit identity comparator	ICMP4	2	5
	8-bit identity comparator	ICMP8	3	9
	2-bit magnitude comparator with enable	MCMPC2	3	9
	4-bit magnitude comparator with enable	MCMPC4	4	18
	8-bit magnitude comparator with enable	MCMPC8	6	36
	16-bit magnitude comparator	MCMP16	5	93
Counters	4-bit binary counter with load, clear	CNT4A	4	18
	4-bit binary counter with load, clear, carry in, and carry out	CNT4B	4	15
	4-bit up/down counter with load, carry in, and carry out	UDCNT4A	6	24
Decoders	2 to 4 decoder	DEC2X4	1	4
	2 to 4 decoder with active low outputs	DEC2X4A	1	4
	2 to 4 decoder with enable	DECE2X4	1	4
	2 to 4 decoder with enable and active low outputs	DECE2X4A	1	5
	3 to 8 decoder	DEC3X8	1	8
	3 to 8 decoder with active low outputs	DEC3X8A	1	9
	3 to 8 decoder with enable	DECE3X8	2	11
	3 to 8 decoder with enable and active low outputs	DECE3X8A	2	11
	4 to 16 decoder with active low outputs	DEC4X16A	2	20
Multiplexors	8 to 1 multiplexor	MX8	2	3
	8 to 1 multiplexor with active low output	MX8A	2	3
	16 to 1 multiplexor	MX16	2	5
Multipliers	8 x 8 multiplier	SMULT8		241
Registers	Octal latch with clear	DLC8A	1	8
	Octal latch with enable	DLE8	1	8
	Octal latch with multiplexed data	DLM8	1	8
	Octal with preset, clear, and enable	REGE8A	2	20
	Octal with preset, clear, enable, and active low clock	REGE8B	2	20
	4-bit shift register with clear	SREG4A	2	8
	8-bit shift register with clear	SREG8A	2	18

Hard Macros

Function	Description	Macro Name	Equation(s)	Modules Required
AND	2-Input	AND2	Y = A B	1
		AND2A	Y = !A B	1
		AND2B	Y = !A !B	1
	3-Input	AND3	Y = A B C	1
		AND3A	Y = !A B C	1
		AND3B	Y = !A !B C	1
		AND3C	Y = !A !B !C	1
	4-Input	AND4	Y = (A B C D)	2
		AND4A	Y = (!A B C D)	2
		AND4B	Y = !A !B C D	1
		AND4C	Y = !A !B !C D	1
		AND4D	Y = (!A !B !C !D)	2
OR	2-Input	OR2	Y = A + B	1
		OR2A	Y = !A + B	1
		OR2B	Y = !A + !B	1
	3-Input	OR3	Y = A + B + C	1
		OR3A	Y = !A + B + C	1
		OR3B	Y = !A + !B + C	1
		OR3C	Y = !(A B C)	2
	4-Input	OR4	Y = A + B + C + D	1
		OR4A	Y = !A + B + C + D	1
		OR4B	Y = !A + !B + C + D	2
		OR4C	Y = !A + !B + !C + D	2
		OR4D	Y = !A + !B + !C + !D	2
NAND	2-Input	NAND	Y = !(A B)	1
		NAND2A	Y = !(A B)	1
		NAND2B	Y = !(!A !B)	1
	3-Input	NAND3	Y = !(A B C)	2
		NAND3A	Y = !(!A B C)	1
		NAND3B	Y = !(!A !B C)	1
		NAND3C	Y = !(!A !B !C)	1
	4-Input	NAND4	Y = !(A B C D)	2
		NAND4A	Y = !(!A B C D)	2
		NAND4B	Y = !(!A !B C D)	2
		NAND4C	Y = !(!A !B !C D)	1
		NAND4D	Y = !(!A !B !C !D)	1
NOR	2-Input	NOR2	Y = !(A + B)	1
		NOR2A	Y = !(!A + B)	1
		NOR2B	Y = !(!A + !B)	1
	3-Input	NOR3	Y = !(A + B + C)	1
		NOR3A	Y = !(!A + B + C)	1
		NOR3B	Y = !(!A + !B + C)	1
		NOR3C	Y = !(!A + !B + !C)	1
	4-Input	NOR4	Y = !(A + B + C + D)	2
		NOR4A	Y = !(!A + B + C + D)	1
		NOR4B	Y = !(!A + !B + C + D)	1
		NOR4C	Y = !(!A + !B + !C + D)	2
		NOR4D	Y = !(!A + !B + !C + !D)	2

Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	Modules Required
Exclusive OR	XOR	XOR	Y = A ^ B	1
		XO1	Y = (A ^ B) + C	1
		XO1A	Y = !(A ^ B) + C	1
	XNOR	XNOR	Y = !(A ^ B)	1
	XOR-AND	XA1	Y = (A ^ B) C	1
		XA1A	Y = !(A ^ B) C	1
	AND-XOR	AX1	Y = (!A B) ^ C	1
		AX1A	Y = !((!A B) ^ C)	1
		AX1B	Y = (!A !B) ^ C	1
AND-OR		AO1	Y = (A B) + C	1
		AO1A	Y = (!A B) + C	1
		AO1B	Y = (A B) + (!C)	1
		AO1C	Y = (!A B) + (!C)	1
		AO2	Y = ((A B) + C + D)	1
		AO2A	Y = ((!A B) + C + D)	1
		AO3	Y = (!A B C) + D	1
		AO4A	Y = (!A B C) + (A C D)	1
		AO5A	Y = (!A B) + (A C) + D	1
		MAJ3	Y = (A B) + (B C) + (A C)	1
AND-OR Invert		AOI1	Y = !(**A B** + C)	2
		AOI1A	Y = !((!A B) + C)	1
		AOI1B	Y = !((A B) + !C)	1
		AOI2A	Y = !((!A B) + C + D)	1
		AOI2B	Y = !((!A B) + !C + D)	1
		AOI3A	Y = !((!A !B !C) + (!A !D))	1
		AOI4	Y = !(A B + **C D**)	2
OR-AND		OA1	Y = (A + B) C	1
		OA1A	Y = (!A + B) C	1
		OA1B	Y = (A+ B) (!C)	1
		OA1C	Y = (!A + B) (!C)	1
		OA2	Y = (C + D) (A + B)	1
		OA2A	Y = ((C + D) (!A + B))	1
		OA3	Y = ((A + B) C D)	1
		OA3A	Y = ((A + B) !C D)	1
		OA3B	Y = ((!A + B) !C D)	1
		OA4A	Y = ((A + B + !C) D)	1
		OA5	Y = (A + B + C) (A + D)	1
OR-AND Invert		OAI1	Y = !((A + B) & C)	1
		OAI2A	Y = !((A + B + C) !D)	1
		OAI3	Y = !((**A + B**) C D)	2
		OAI3A	Y = !((A + B) !C !D)	1
Buffers and Inverters		BUF	Y = A	1
		BUFA	Y = !(!A)	1
		INV	Y = !A	1
		INVA	Y = !A	1

Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	Modules Required
Multiplexors	2:1	MX2	Y = (A !S) + (B S)	1
		MX2A	Y = (!A !S) + (B S)	1
		MX2B	Y = (A !S) + (!B S)	1
		MX2C	Y= (!A !S) + (!B S)	1
	4:1	MX4	Y = (D0 !S0 !S1) + (D1 S0 !S1) + (D2 !S0 S1) + (D3 S0 S1)	1
Adders	Half	HA1	CO =A B S =A ^ B	2
		HA1A	CO = !A B S = !(A ^ B)	2
		HA1B	CO = !(A B) S = !(A ^ B)	2
		HA1C	CO = !(A B) S = (A ^ B)	
	Full	FA1A	CO = (CI !B !A) + (A !B) + (B CI A) **S** = (B !A !CI) + (CO !A CI) + (CO A !CI) + (B A CI)	2
		FA1B	CO = !A(!B + B CI) + A(!B CI) **S** = !A(!CI CO + CI B) + A(!CI B + CI CO)	2
		FA2A	CO = (CI !B !(A0+A1)) + (!B (A0+A1)) + (B CI (A0+A1)) **S** = (B !(A0+A1) !CI) + (CO !(A0+A1) CI) + (CO (A0+A1) !CI) + (B (A0+A1)CI)	2
		FA3A	CO = (B0 !(A0+A1)!B1)+(!(A0 + A1) B1)+ ((A0 + A1) !B1) +((A0 + A1) B1) **S** = (B0 !(A0 + A1) !B2) + (!(A0 + A1) B2) + (B0 (A0 + A1) !B1)	2
Boolean		MXCI	Y = (!((!S A) + (S B)) C) + (((!S A) + (S B)) D)	1
		MXT	Y = (!S1 !S0A D0) + (!S1 S0A D1)+ (S1 !S0B D2) + (S1 S0B D3)	1
D-type Flip-Flops	with clear	DF1	Q = (CLK, D, -, -)	2
		DF1A	QN = !(CLK, D, -, -)	2
		DF1B	Q = (!CLK, D, -, -)	2
		DF1C	QN = !(!CLK, D, -, -)	2
		DFC1	Q = (CLK, D, CLR, -)	2
		DFC1A	Q = (!CLK, D, CLR, -)	2
		DFC1B	Q = (CLK, D, !CLR, -)	2
		DFC1C	QN = !(CLK, D, CLR, -)	2
		DFC1D	Q = (!CLK, D, !CLR, -)	2
		DFC1E	QN = !(CLK, D, !CLR, -)	2
		DFC1F	QN = !(!CLK, D, CLR, -)	2
		DFC1G	QN = !(!CLK, D, !CLR, -)	2

Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	Modules Required
D-type Flip-Flops (continued)	with enable	DFE	Q = (CLK, E D + !E Q, –, –)	2
		DFE1B	Q = (CLK, !E D + E Q, –, –)	2
		DFE1C	Q = (!CLK, !E D + E Q, –, –)	2
		DFE2D	Q = (!CLK, !E D + E Q, !CLR, PRE)	2
		DFE3A	Q = (!CLK, E D + !E Q, !CLR, –)	2
		DFE3B	Q = (!CLK, E D + !E Q, !CLR, –)	2
		DFE3C	Q = (CLK, !E D + E Q, !CLR, –)	2
		DFE3D	Q = (!CLK, !E D + E Q, !CLR, –)	2
		DFE4	Q = (CLK, E D + !E Q, –, PRE)	2
		DFE4A	Q = (!CLK, E D + !E Q, –, PRE)	2
		DFE4B	Q = (CLK, !E D + E Q, –, PRE)	2
		DFE4C	Q = (!CLK, !E D + E Q, –, PRE)	2
		DFEA	Q = (!CLK, E D + !E Q, –, –)	2
		DFEB	Q = (CLK, E D + !E Q, !CLR,PRE)	2
		DFEC	Q = (!CLK, E D + !E Q, !CLR, PRE)	2
		DFED	Q = (CLK, !E D + E Q, !CLR, PRE)	2
	with multiplexed data	DFM	Q = (CLK, !S A + S B, –, –)	
		DFM1B	QN = !(CLK, !S A + S B, –, –)	2
		DFM1C	QN = !(!CLK, !S A + S B, –, –)	2
		DFM3	Q = (CLK, !S A + S B, CLR, –)	2
		DFM3B	Q = (!CLK, !S A + S B, !CLR, –)	2
		DFM3E	Q = (!CLK, !S A + S B, CLR, –)	2
		DFM3F	QN = !(CLK, !S A + S B, CLR, –)	2
		DFM3G	QN = !(!CLK, !S A + S B, CLR, –)	2
		DFM4	Q = (CLK, !S A + S B, –, PRE)	2
		DFM4A	Q = (CLK, !S A + S B, –, !PRE)	2
		DFM4B	Q = (!CLK, !S A + S B, –, !PRE)	2
		DFM4C	QN = !(CLK, !S A + S B, –, !PRE)	2
		DFM4D	QN = !(!CLK, !S A + S B, –, !PRE)	2
		DFM4E	Q = (!CLK, !S A + S B, –, PRE)	2
		DFM5A	Q = (CLK, !S A + S B, !CLR, PRE)	2
		DFM5B	Q = (!CLK, !S A + S B, !CLR, PRE)	2
		DFMA	Q = (!CLK, !S A + S B, –, –)	2
		DFMB	Q = (CLK, !S A + S B, !CLR, –)	2
	with multiplexed data and enable	DFME1A	Q = (CLK, !E (!S A + S B) + E Q, –, –)	2
	with preset	DFP1	Q = (CLK, D, –, PRE)	2
		DFP1A	Q = (!CLK, D, –, PRE)	2
		DFP1B	Q = (CLK, D, –, !PRE)	2
		DFP1C	QN = !(CLK, D, –, PRE)	2
		DFP1D	Q = (!CLK, D, –, !PRE)	2
		DFPIE	QN = !(CLK, D, –, !PRE)	2
		DFP1F	QN= !(!CLK, D, –, PRE)	2
		DFP1G	QN = !(!CLK, D, –, !PRE)	2
	with clear and preset	DFPC	Q = (CLK, D, !CLR, PRE)	2
		DFPCA	Q = (!CLK, D, !CLR, PRE)	2

Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	Modules Required
JK Flip-Flops		JKF	Q = (CLK, (!Q J + Q K)), –, –)	2
		JKF1B	Q = (!CLK, (!Q J + Q K), –, –)	2
		JKF2A	Q = (CLK, (!Q J + Q K), !CLR, –)	2
		JKF2B	Q = (!CLK, (!Q J + Q K), !CLR, –)	2
		JKF2C	Q = (CLK, (!Q J + Q K), CLR, –)	2
		JKF2D	Q = (!CLK, (!Q J + Q K), CLR, –)	2
		JKF3A	Q = (CLK, (!Q J + Q K), – !PRE)	2
		JKF3B	Q = (!CLK, (!Q J + Q K), –, !PRE)	2
		JKF3C	Q = (CLK, (!Q J + Q K), –, PRE)	2
		JKF3D	Q = (!CLK, (!Q J + Q K), –, PRE)	2
		JKF4B	Q = (!CLK, (!Q J + Q K), !CLR, PRE)	2
		JKFPC	Q = (CLK, (!Q J + Q K), !CLR, PRE)	2
Data Latches	with clear	DL1	Q = (G, D, –, –)	1
		DL1A	QN = !(G, D, –, –)	1
		DL1B	Q = (!G, D, –, –)	1
		DL1C	QN = !(!G, D, –, –)	1
		DLC	Q = (G, D, !CLR, –)	1
		DLC1	Q = (G, D, CLR, –)	1
		DLC1A	Q = (!G, D, CLR, –)	1
		DLC1F	QN = !(G, D, CLR, –)	1
		DLC1G	QN = !(!G, D, CLR, –)	1
		DLCA	Q = (!G, D, !CLR, –)	1
	with enable	DLE	Q = (G, (E D + !E Q), –, –)	1
		DLE1D	QN = !(!G, (!E D + E Q), –, –)	1
		DLE2A	Q = (!G, (E D + !E Q), CLR, –)	1
		DLE2B	Q = (!G, (!E D + E Q), !CLR, –)	1
		DLE2C	Q = (!G, (!E D + E Q), CLR, –)	1
		DLE3A	Q = (!G, (E D + !E Q), –, PRE)	1
		DLE3B	Q = (!G, (!E D + E Q), –, PRE)	1
		DLE3C	Q = (!G, (!E D + E Q), –, !PRE)	1
		DLEA	Q = (G, (!E D + E Q), –, –)	1
		DLEB	Q = (!G, (E D + !E Q), –, –)	1
		DLEC	Q = (!G, (!E D + E Q), –, –)	1
	with multiplexed data	DLM	Q = (G, (A !S + B S), –, –)	1
		DLM2A	Q = (!G, (A !S + B S), CLR, –)	1
		DLMA	Q = (!G, (A !S + B S), –, –)	1
	with multiplexed data and enable	DLME1A	Q = (!G, !E (A !S + B S) + E Q, –, –)	1
	with preset	DLP1	Q = (G, D, –, PRE)	1
		DLP1A	Q = (!G, D, –, PRE)	1
		DLP1B	Q = (G, D, –, !PRE)	1
		DLP1C	Q = (!G, D, –, !PRE)	1
		DLP1D	QN = !(G, D, –, !PRE)	1
		DLP1E	QN = !(!G, D, –, !PRE)	1
	with preset and clear	DL2A	Q = (G, D, !CLR, PRE)	1
		DL2B	QN = !(!G, D, CLR, !PRE)	1
		DL2C	Q = (!G, D, !CLR, PRE)	1
		DL2D	QN = !(G, D, CLR, !PRE)	1

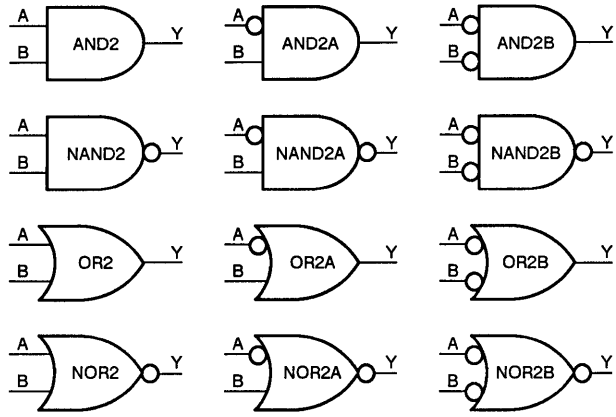
Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	Modules Required
Clock Net Interface Macros		GAND2	Y = A G	1
		GMX4	Y = (D0 !S0 !G) + (D1 !G S0) + (D2 G !S0) + (D3 S0 G)	1
		GNAND2	Y = !(A G)	1
		GNOR2	Y = !(A + G)	
		GOR2	Y = A + G	1
		GXOR	Y = A ^ G	1
Logical Tieoff Macros		GND		
		VCC		

Hard Macro Library Overview

The following illustrations show all the available Hard Macros.

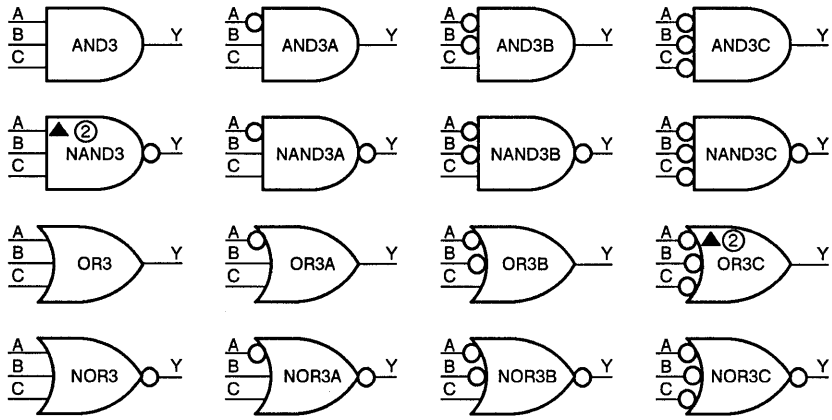
2-Input Gates (Module Count = 1)



3-Input Gates (Module Count = 1, unless indicated otherwise)

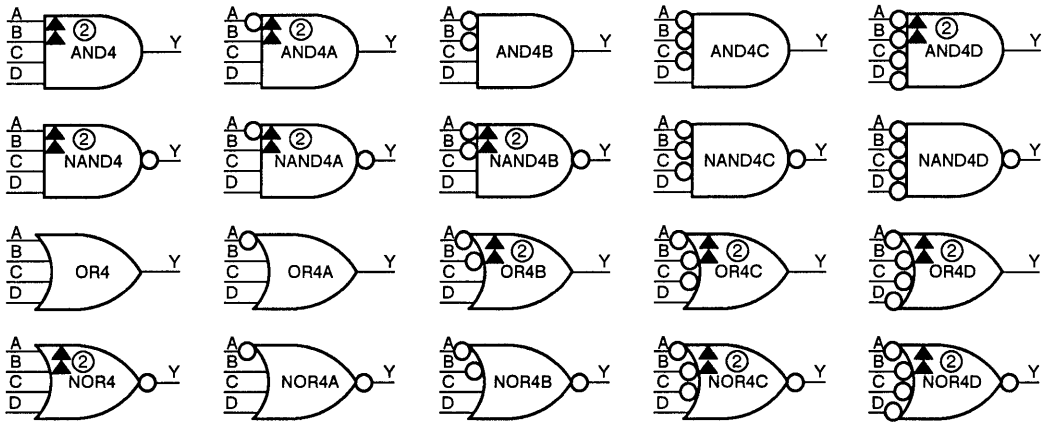
② Indicates 2-module macro

▲ Indicates extra delay input



4-Input Gates (Module Count = 1, unless indicated otherwise)

② Indicates 2-module macro
▲ Indicates extra delay input



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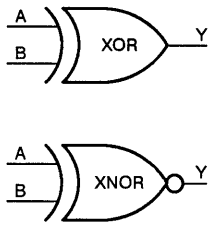
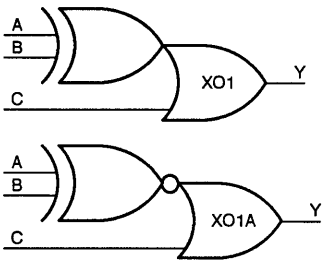
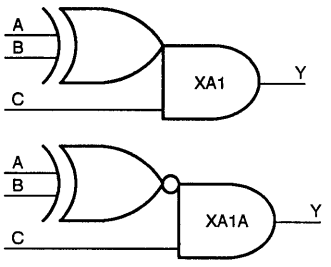
XOR Gates
(Module Count = 1)



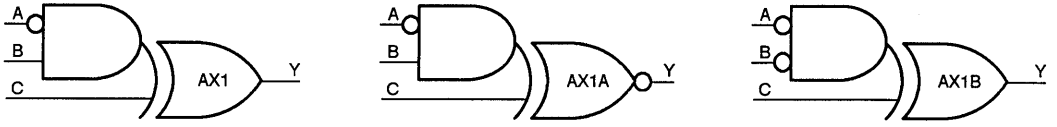
XOR OR Gates
(Module Count = 1)



XOR AND Gates
(Module Count = 1)

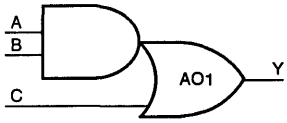


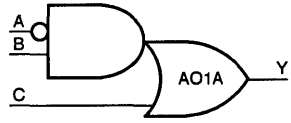
AND XOR Gates
(Module Count = 1)

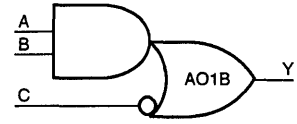


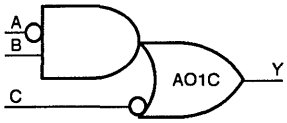
AND OR Gates (Module Count = 1)

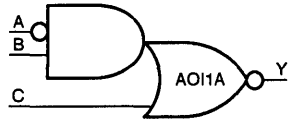
② Indicates 2-module macro
▲ Indicates extra delay input

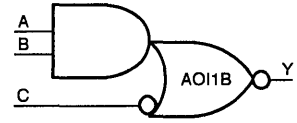


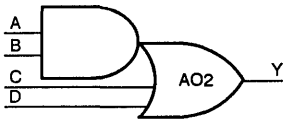


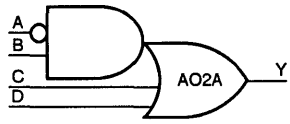


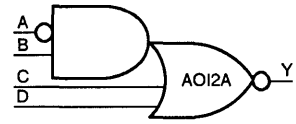


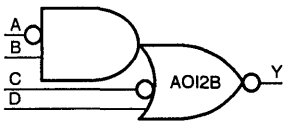


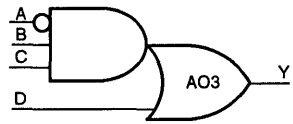


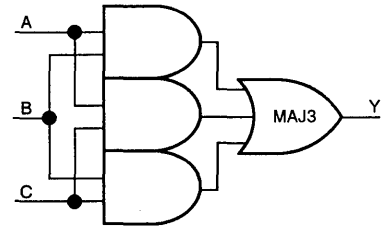


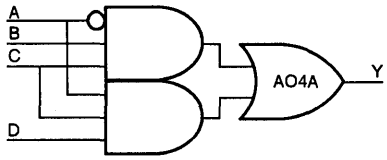


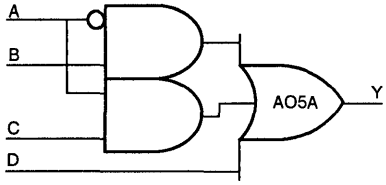


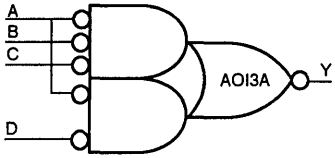


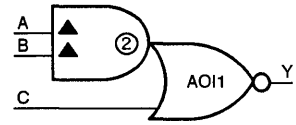


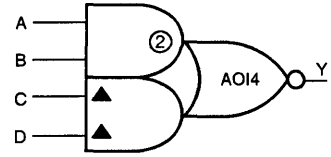






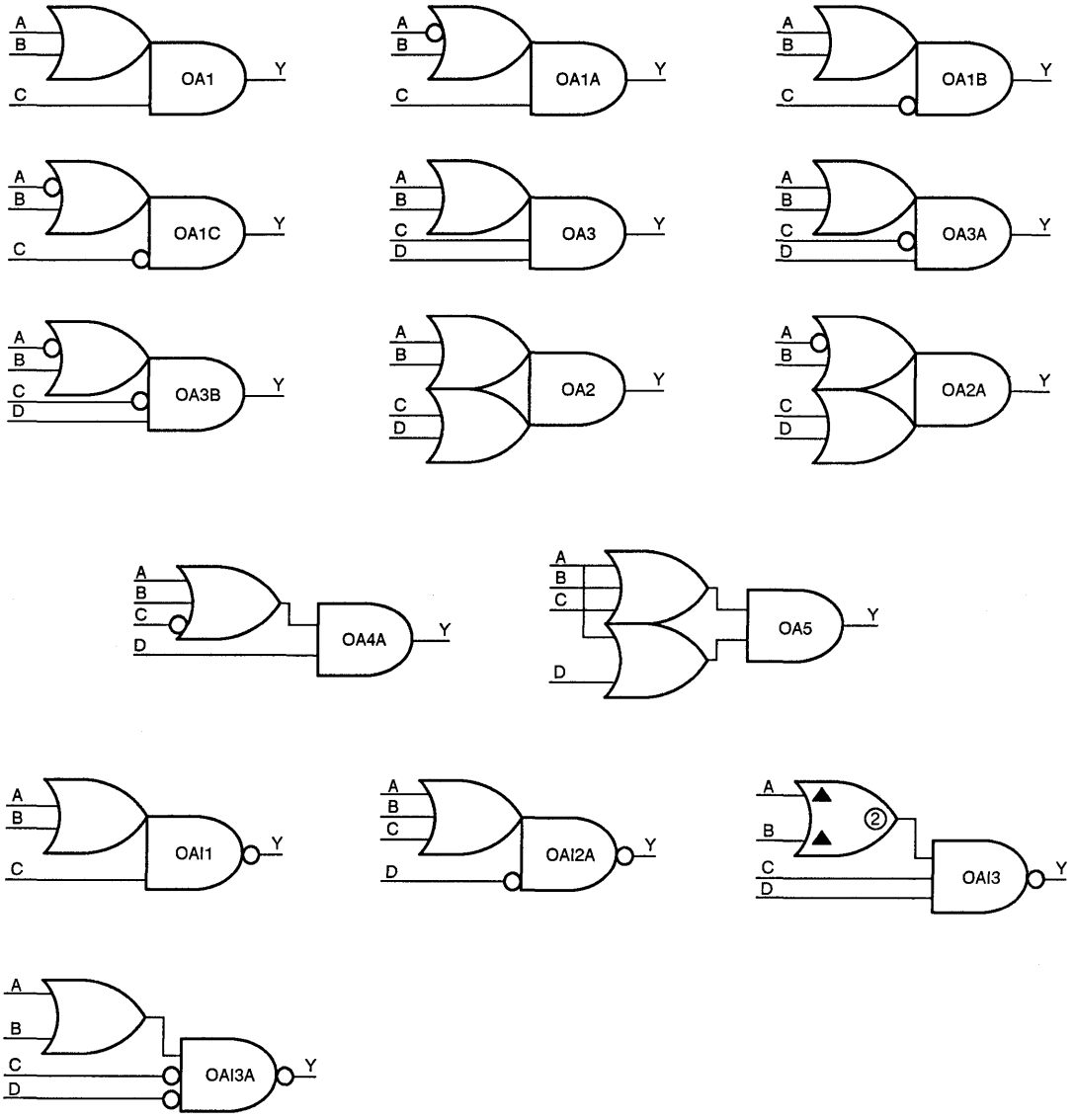




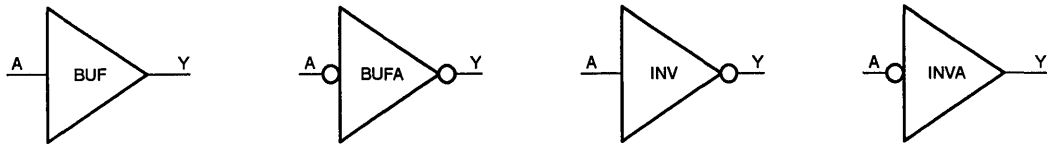


OR AND Gates (Module Count = 1)

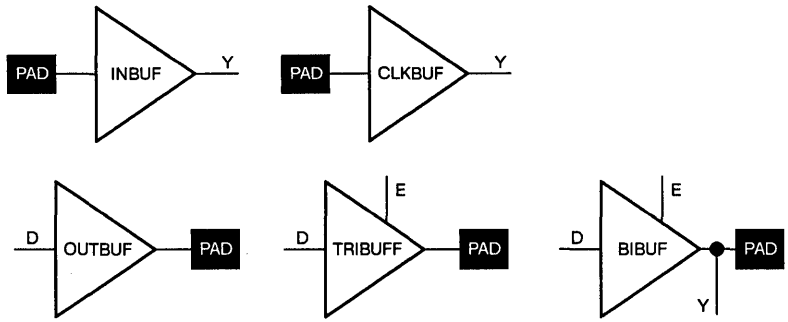
② Indicates 2-module macro
▲ Indicates extra delay input



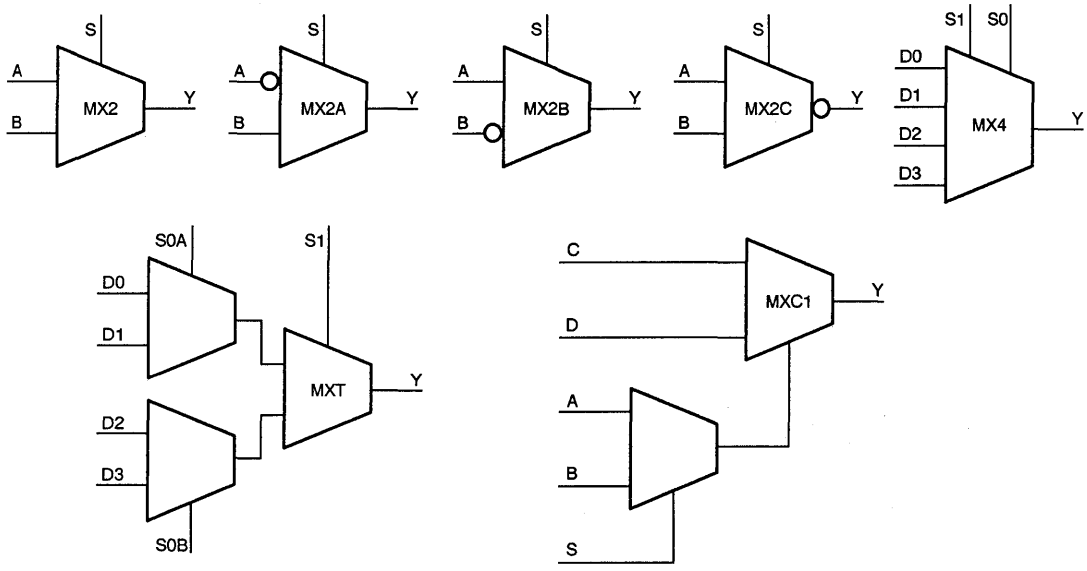
Buffers (Module Count = 1)



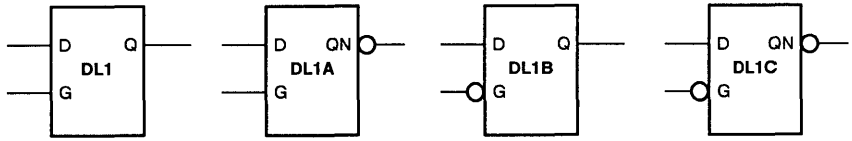
I/O Buffers (I/O Module Count = 1)



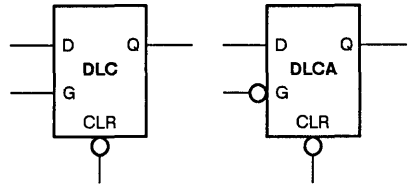
Multiplexors (Module Count = 1)



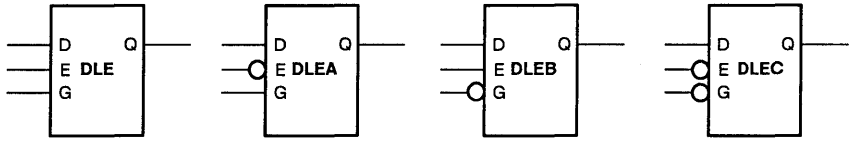
Latches (Module Count = 1)



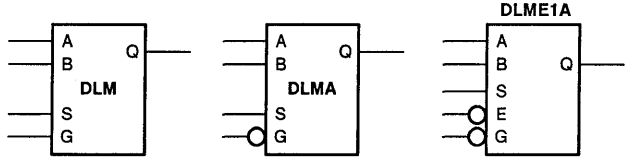
D Latches with Clear (Module Count = 1)



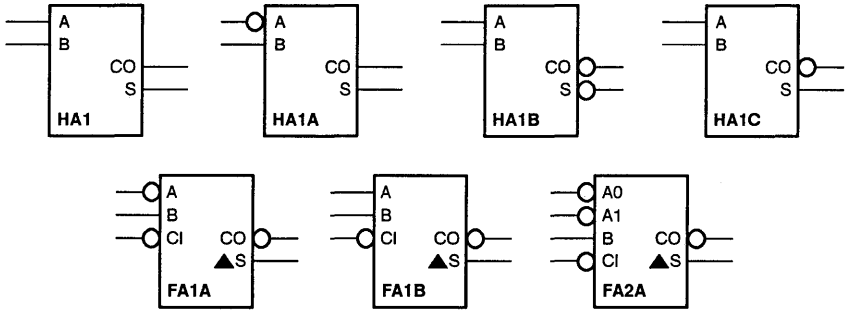
D Latches with Enable (Module Count = 1)



Mux Latches (Module Count = 1)

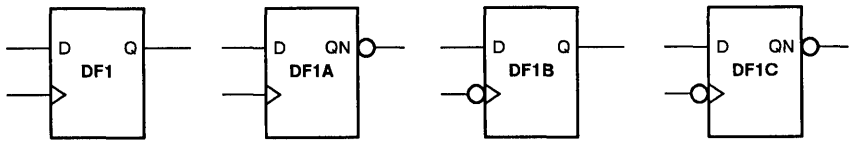


Adders (Module Count = 2)

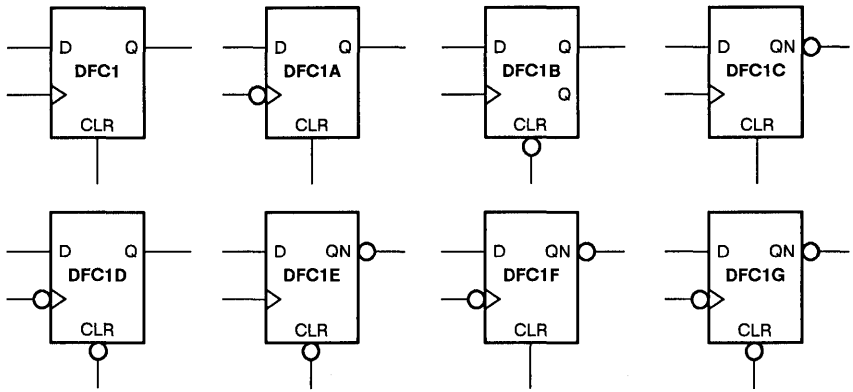


Macros FA1A, FA1B, and FA2A have two level delays from the inputs to the S outputs, as indicated by the▲

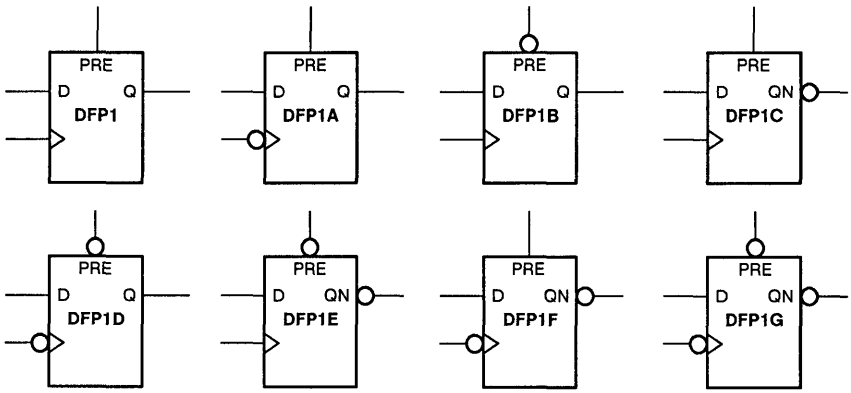
D-type Flip-Flops (Module Count = 2)



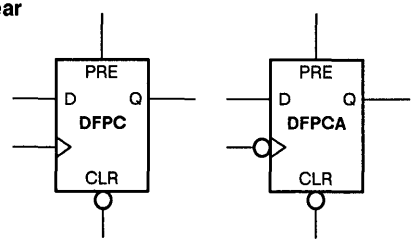
D-type Flip-Flops with Clear



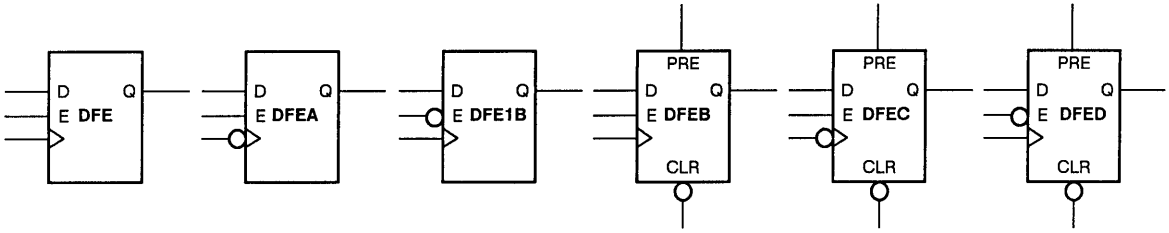
D-type Flip-Flops with Preset



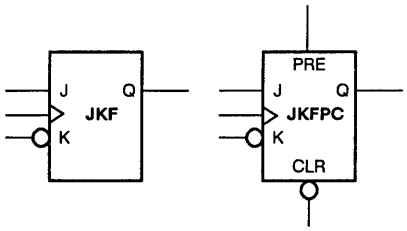
D-type Flip-Flops with Preset and Clear



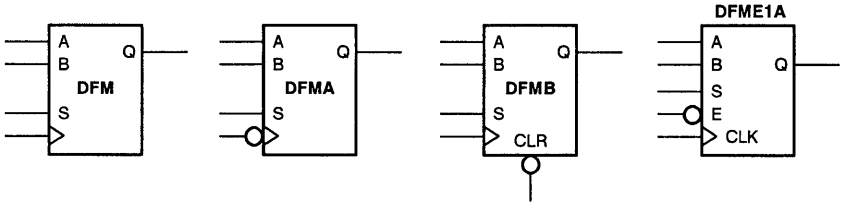
D-type Flip-Flops with Enable (Module Count = 2)



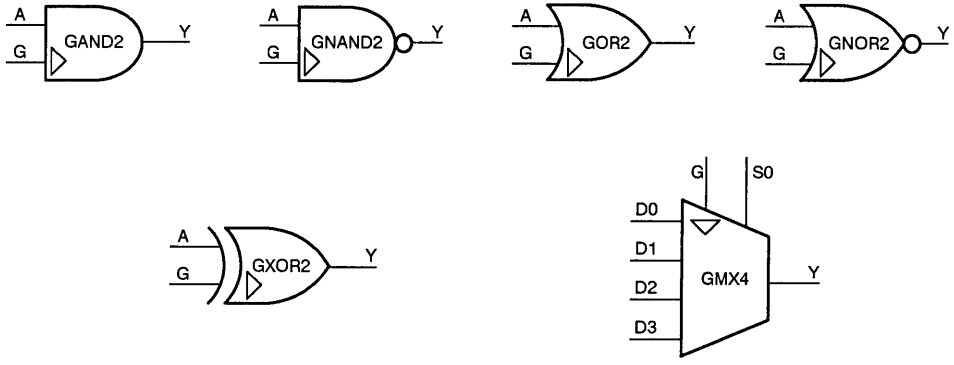
JK Flip-Flops (Module Count = 2)



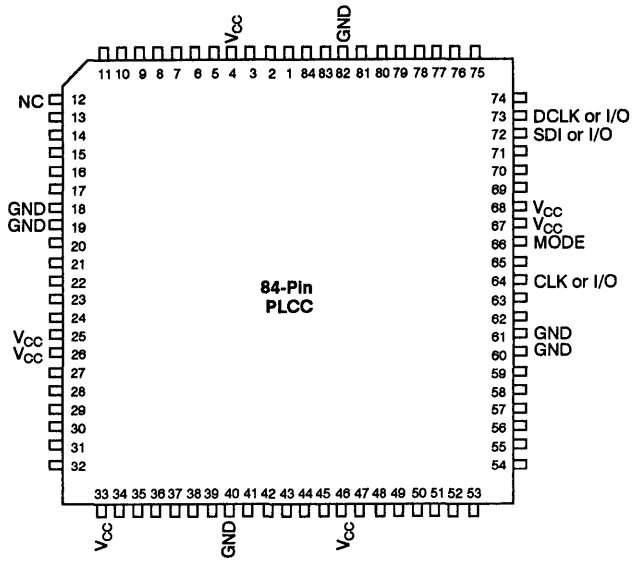
MUX Flip-Flops (Module Count = 2)



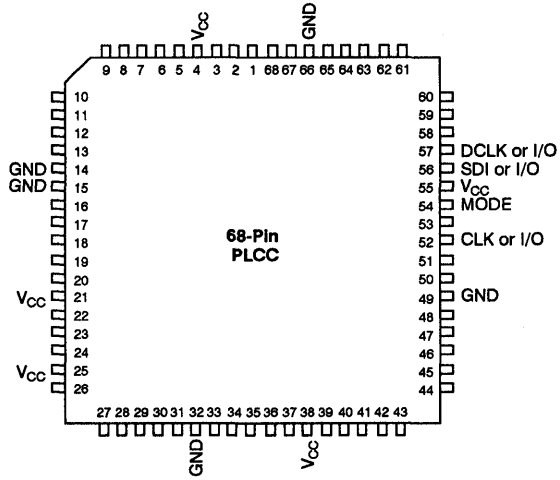
CLKBUF Interface Macros (Module Count = 1)



Package Pin Assignments: 84-Pin PLCC (Top View)

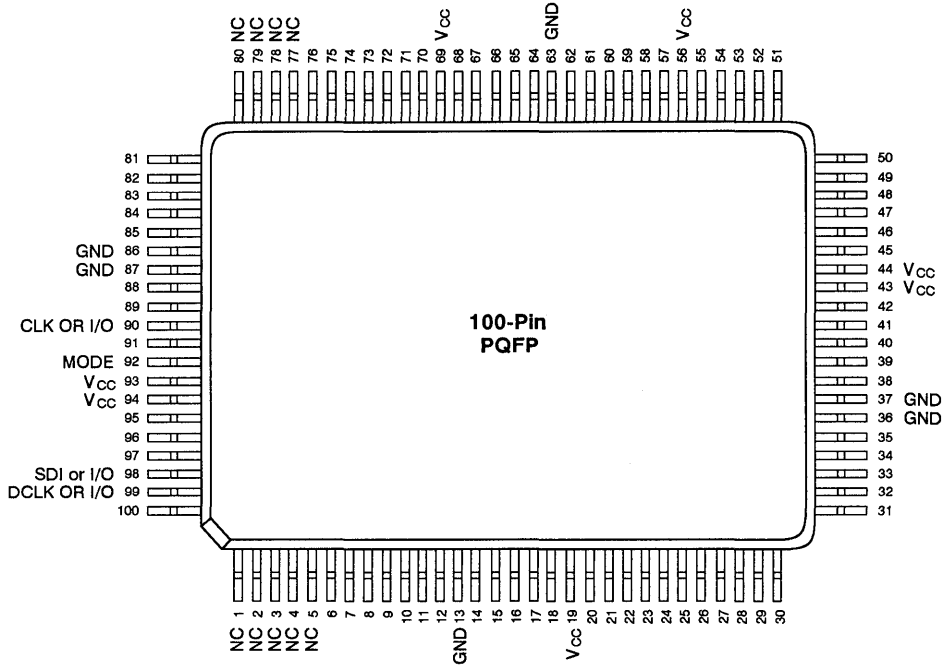


Package Pin Assignments: 68-Pin PLCC (Top View)



Notes:
1. MODE must be terminated to circuit ground.
2. All unassigned pins are available for use as I/Os.

Package Pin Assignments: 100-Pin PQFP (Top View)

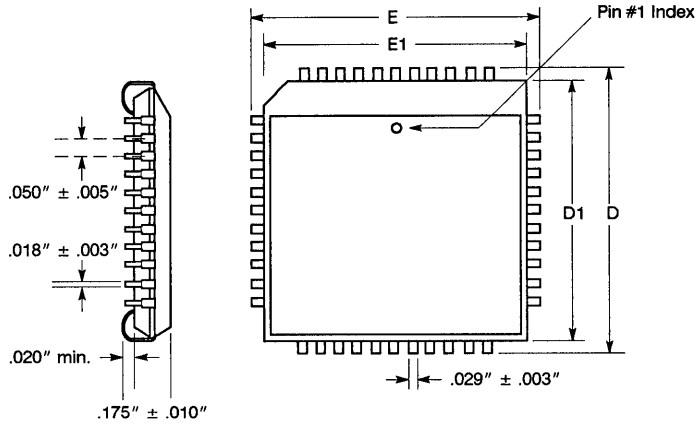


Notes:

1. MODE must be terminated to circuit ground.
2. All unassigned pins are available for use as I/Os.

Package Mechanical Details

Plastic J-Leaded Chip Carrier

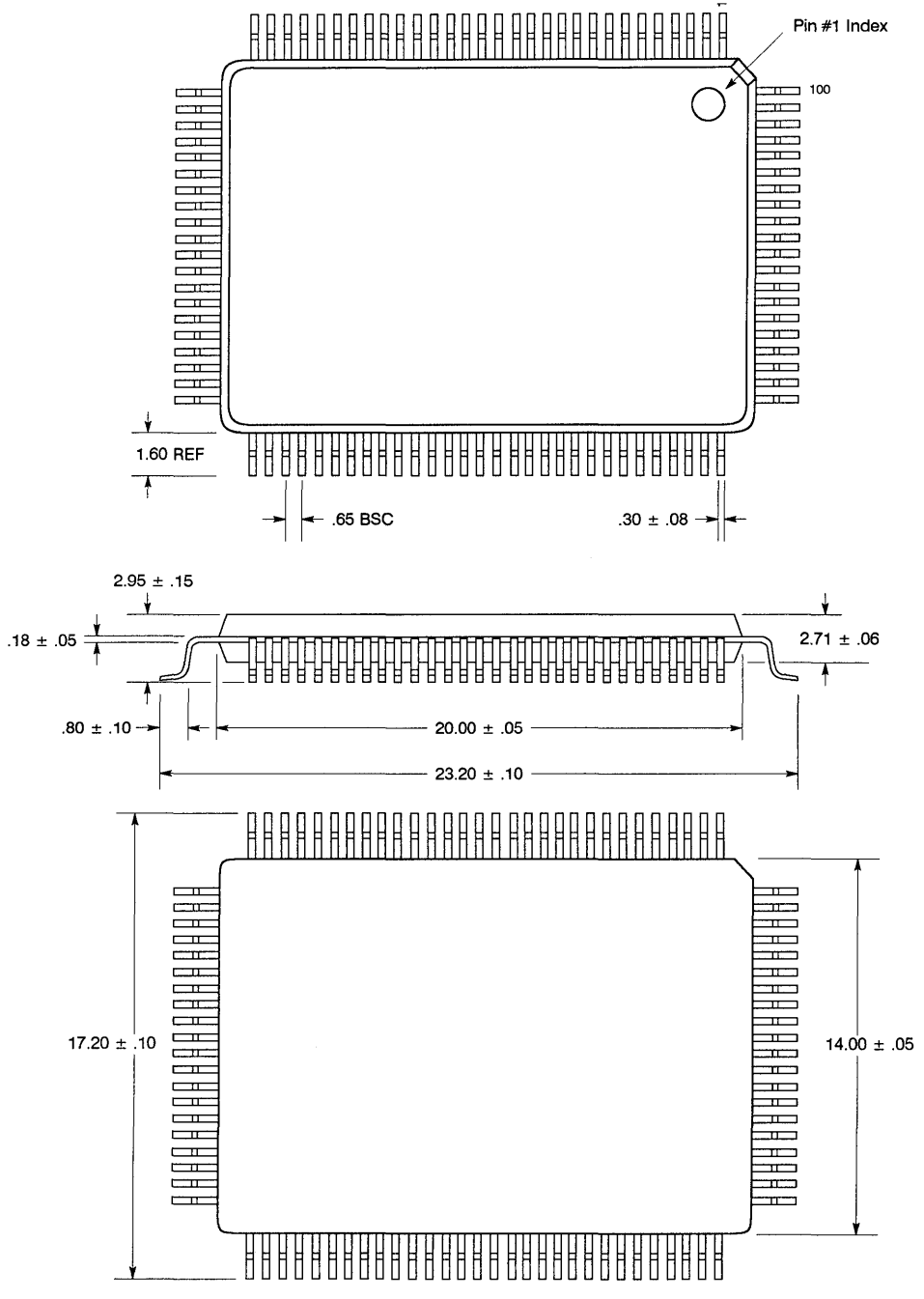


Lead Count	D, E	D1, E1
68	.990" ± .005"	.955" ± .005"
84	1.190" ± .005"	1.155" ± .005"

Package Mechanical Details (continued)

Plastic Quad Flatpack

Dimensions in millimeters



Array Architecture for ATG with 100% Fault Coverage

Technical Paper

Abstract

This paper discusses array architecture, circuitry and methodology for the automatic generation of test vectors. The architecture is implemented in a mask programmed version of an antifuse based FPGA. The architecture allows the designer to 100% control and observe each node in the circuit. This allows the automatic generation of test vectors with 100% fault coverage independent of the design implemented in the array circuit. In addition to architecture and circuit implementation details, this paper discusses the ATG generation methodology and algorithms, circuit overhead for the test features as well as test times and results.

Overview

To the ASIC user, Field Programmable Gate Arrays (FPGAs) [1] offer many advantages over conventional mask programmable gate arrays. A primary advantage of the FPGA is that it speeds up the "time to market" of the new system by removing the ASIC design from the critical path of the system design cycle. However, once the new system goes into high volume production, the user will often convert his FPGA design into a conventional gate array to reduce the cost of the system. Though the conversion to a gate array may ultimately reduce manufacturing costs, significant engineering time is expended translating FPGA design netlists to a gate array and, especially, developing test vectors to test the gate array.

An ideal ASIC solution should (a) provide fast time to market, (b) reduce high volume manufacturing costs and (c) eliminate the need for further design engineering involvement in translating netlists and generating test vectors. A masked programmable gate array, which is a one-mask version of an antifuse-based FPGA has been developed to satisfy the above requirements. The architecture of the antifuse based FPGA shown in Figure 1 is essentially that of a channelled gate array with rows of functional logic modules alternating with channels of horizontal routing tracks [1]. Antifuses are programmed to connect the logic module inputs and outputs to the routing tracks. In the mask programmable version of the FPGA, the antifuses programmed for a given design are simply replaced with vias connecting two metal layers, thus preserving the original netlist. This is accomplished with the aid of software which automatically converts a fuse design netlist into a via mask layer for that design. All other mask layers are common between designs. The MPGA has a much smaller die than the FPGA version because the antifuses and, more significantly, the associated programming circuitry have been eliminated, thus providing substantial cost savings.

A significant advantage of the MPGA over a conventional gate array, is that the MPGA's architecture includes built-in testability. This architecture, which is the focus of this paper, reduces the problem of generating test vectors for an entire design into a set of predetermined tests of the individual logic modules. Test vectors are generated automatically to test the user design and interconnect wiring with 100% fault coverage. It is important to note that while this built-in testability has been implemented in a mask-programmable version of an FPGA, it could easily be included in the design of FPGAs and conventional gate arrays.

Architecture and Circuitry

The MPGA architecture, which is similar to the A1020 FPGA consists of 14 rows and 44 columns of logic modules with routing channels between the module rows as shown in Figure 1. The user's logic design is created by interconnecting logic module inputs and outputs to routing tracks. Logic modules implement the required logic functions while I/O modules connect logic modules to I/O buffers and to package pins.

The ATG control operation works as follows. Each logic module (Figure 2) is divided into an input section LM' and an output section LM". Each has its own latching capability. The two sections may be isolated from one another or connected by the operating modes of the circuit. Since inputs and outputs of all modules are interconnected together by routing tracks, separating LM' and LM" of all logic modules essentially breaks the entire design up into combinational pieces where each LM' of a logic module is driven by LM" of other modules or its own LM". Using this feature, complex testing situations such as feedback loops, reconvergent connections, and sequential circuits are converted into simple combinational circuits that can be readily tested. Any LM" can be randomly addressed and controlled with desired logic values which serve as the stimuli for the LM' sections. Each LM' is tested by controlling the corresponding LM"s connected to its inputs.

Then, the LM' logic function is computed and latched into the LM' latch. Subsequently, the latched result is transferred from LM' latch to LM" for "ATG observe". In this mode, any LM" can be randomly addressed and its contents read out to the periphery circuits [2]. Periphery and control circuits provide all the necessary timing and mode control operations needed to implement the above functions.

Logic Module

The MPGA Logic Module with testability capability is shown in Figure 2. The logic module has eight data inputs (S0, S1, SA, A1, A0, B0, B1, SB), 1 output (OUT), 5 control signals (Yi, Xi, TDI, C2, C1) and a sense output signal (SEN_Xi). Control signals determine logic module operations in the various operating modes.

As explained above, the logic module is divided into two sections LM' and LM". Signals C1 and C2 control sections LM' and LM". When C1 = 0, mux3 is enabled and latch1 is transparent. When C1 = 1, mux3 is disabled with a three-state output and latch1 is in a latching mode. C2 = 0 turns Q1 "ON" and makes latch2 transparent. C2 = 1 turns Q1 "OFF" and configures latch2 as a latch. When Q1 is "OFF", LM" is disconnected from LM'. By controlling C1 and C2, the following operations are possible: (a) data can be stored in latch1 and/or latch2, (b) LM" can be connected or disconnected from LM', and (c) data can be transferred from LM' to LM".

In the ATG Control phase, Xi, Yi, and TDI (Test Data Input) are used to control LM". In this phase LM" is separated from LM' by maintaining C2 at "1" and C1 at "0". The ATG Observe phase works as follows. The controlled LM" outputs drive LM' of other logic modules (or its own LM') and subsequently causes logic computation in the driven LM'. Using C1 and C2 control signals the computed data is first latched into LM' and then transferred to LM". The final result is then read out via the micro-probe sensing circuits and the SEN_Xi line. In normal logic module operation, C1, C2, and Xi are at "0", latch1 and latch2 become transparent, LM' is connected to LM", and LM" is isolated from the TDI input.

I/O Module

Figure 3 shows the schematic for the I/O Module. P_EN, P_OUT, and P_IN are direct input and output interconnects to the I/O Buffer; EN, IN are I/O Module inputs. Xi, Yi, TDI, and SEN_Xi perform identical functions as the Logic Module. C3, which is similar to C1 and C2, is for ATG control operation. When C3 = 0, the I/O module is normally operating where P_EN is controlled by EN input. When C3 = 1, P_EN is controlled by TDI. Thus, the I/O Buffer can be set as an "input pin" or an "output pin" by storing the appropriate TDI data bit into latch1 of I/O module in ATG testing.

Array Test Example

A "5 X 5 Logic Module Array example" with interconnect is shown in Figure 4. For simplicity, each logic module will be denoted as LM(Xi,Yi), and each I/O module will be denoted as I/OM(Xi,Yi). The bottom row address will be X0 and the left-most column will be Y0. All LM(Xi,Yi) and I/OM(Xi,Yi) are controlled by C1, C2, C3, and TDI global control signals. In a normal chip operation, C1, C2, C3, Xi, and Yi are "0" and the array functions are the desired user design.

Assume LM(2,1) is to be "ATG-tested". Inputs LM'(2,1) are connected to LM"(2,1), I/OM(3,0), LM"(1,1), and LM"(1,2). When C2 is placed in "high" state, all LM"(Xi,Yi) are disconnected from their LM'(Xi,Yi). Also, all logic module data are preserved at the LM" latches. By addressing and controlling LM"(2,1), LM"(1,1), and LM"(1,2), inputs of LM'(2,1) can be set to a specific test vector for ATG testing. Since IOM(3,0) is one of the inputs to LM'(2,1) also, its associated I/O buffer needs to be converted to an input pin so that test vectors can be applied to the pin directly. This is achieved by ATG control of IOM(3,0) with a data value "1".

After the ATG control is completed for the inputs of LM'(2,1), C1 is placed in "high" state to latch new data in all LM'(Xi,Yi). Then, C2 is placed in "low" state to connect and enable data transfer from LM' to LM". New data can be read from the corresponding SEN_Xi line for verification. As for LM(2,1), new data is read from SEN_X2 line and this completes the ATG testing for this particular logic module and its input interconnects to the other modules.

Automatic Test Generation (ATG)

An example of a basic test flow is illustrated as follows. One of the greatest difficulties in ATG is testing circuits that contain sequential elements, feedback loops and reconvergent fan-outs. Instead of generating ATG vectors for the complete circuit, vectors are generated only for the logic module whose simplified ATG model is shown in Figure 5. The only variable in this "logic module ATG" is the connectivity of the circuit. Feedback connections used to implement sequential circuits are broken by virtue of the split module sections described above. Sequential testing is thus replaced by combinational testing.

The module shown in Figure 5 has no reconvergent fan-out. The module is composed of a few primitive gates. The small size of the module and the fact that it is free of feedback and reconvergent fan-outs means it is practical to exhaustively scan the complete search space for a test solution. This implies the fact that if a fault is detectable, the logic module ATG will always find a test vector in a reasonable amount of time. Thus, the module is guaranteed a 100% fault coverage (single stuck-at-0, stuck-at-1 fault model).

Compared to other test approaches, without any built-in testability, feedback, reconvergent fan-outs or just circuit complexity make ATG systems CPU or memory bound, possibly yielding poor fault coverage. Scan design and built-in probing provide some form of built in testability, but sub-circuits partitioned by scan cells, may still contain reconvergent fan-outs, and are thus difficult for ATG testing. In general, scan based ATG systems give very good fault coverage, but 100% fault coverage is still rarely achievable.

Unlike scan based ATG systems, the MPGA architecture provides design independent ATG. Built-in testability shields testing details from the designer and more importantly, simplifies the ATG problem.

ATG Strategy

The ATG strategy is to generate a test vector which completely tests each module based on its input net configuration. Vector sets of each module are grouped together to form a single set of vectors which are translated to different tester formats.

In order to generate a compact vector set, a traditional ATG approach is used. The ATG uses simple D-algorithm for vector generation and a fault simulator for compaction. A single fault is picked from a list of all possible faults. A D-algorithm is performed to see if the fault is detectable. If an undetectable fault (redundant fault, which has no effect on the circuit) is found, the fault will be removed from the fault list. If the fault is detectable, the vector is fault simulated to see if more faults can be detected. All detected faults are removed from the fault list until the list is exhausted.

The fault model is based on single stuck-at-zero and stuck-at-one faults on input pins of primitive gates. Output pin and interconnect stuck-at faults are tested by verifying their equivalent stuck-at faults at input pins.

Multiplexor Fault Modeling

The MPGA module is based on 2 input multiplexors. General gate array fault modeling approaches usually treat the Multiplexor as a primitive gate as shown in Figure 6 and model the multiplexor as a combination of AND, OR gates. This is not an accurate fault representation. In our ATG module, a more detailed representation is shown in Figure 7. The advantage of modelling at such low level, is that we can examine one of the multiplexor problems [6] traditionally ignored by ATG systems. If the select line S is at fault, we can detect its fault. But if the gate of the transistor is stuck at 0 (Figure 8), a correct result should be the value of B. But for a faulty device, both transistors are turned off and thus the output node is at high impedance state. This is the same as a stuck open fault on the output pin, a vector pair fault, which can be detected by transition.

To handle such a special case, the D-algorithm is extended to support vector pair generation. Whenever the fault under test is the stuck-at-0 fault on the gate of the multiplexor, the D-algorithm switches into transition vector pairs mode. The fault simulator also extends its capability to fault simulate transition vector pairs.

Design Independent Testing

To complete the testing of the array, there are several tests which are independent of the implemented design. The tests include (a) DC Input Levels (V_{IH}, V_{IL}), (b) DC Output Levels (V_{IH}, V_{IL}, V_{OH}, V_{OL}, I_{OL}), (c) Net Shorts test, (d) Three-state Output Leakage, and (e) Static IDD.

Net Shorts Testing

The algorithms used for the module test ATG, and probably all ATG algorithms, use the circuit schematic as input for vector generation. The actual layout of the schematic in silicon is not considered in the ATG process. Therefore, as shown in Figure 8, test vectors generated to exercise Net A, do not consider the potential for a short between Net A and Net B, which cross each other in the layout. However, the built-in testability of the MPGA allows net shorts testing to be performed.

Net shorts testing is accomplished by first latching logic 1s into the outputs of a set of modules and logic 0s into the outputs of the remaining logic modules. Then, the static current of the power supply is measured. If the current is increased over a previously measured baseline value, there must be a short between at least two of the nets driven to opposite states.

The vector set for net shorts testing is surprisingly compact, with only 10 vectors/current measurements required. A vector set is used to test for shorts between nets driven from modules in different rows of the array. Similarly, another vector set is used to test for shorts between nets driven from modules in a different column of the array. When the two vector sets are combined, they exhaustively check for every short. (Note that the vector set for a particular row or column is a binary expansion of the row or column number.) Furthermore, the vector set is completely design independent and depends only on the number of columns and rows of logic modules in the base array.

DC/Parametric Testing

The MPGA's testing architecture allows for all DC and parametric testing to be design independent. The control and observe features of the I/O modules provide much of this capability. For example, to test input levels (V_{IH}, V_{IL}), the I/O module is first set as an "input pin" using the ATG control feature to three-state its associated output. The switching levels of an input signal are applied to the I/O module so that it can be monitored with the addressable microprobe. This three-state mode is also used to measure leakage current in the disabled output buffer and to measure static IDD.

Conclusion

A logic array architecture and circuit implementation for the automatic generation of test vectors has been presented. A masked programmed gate array, which is just one version of an antifuse based FPGA has been developed to satisfy the above requirements. A key feature of the architecture is the ability to control and observe 100% of every node in the design. The test algorithms and methodology used to achieve 100% fault coverage is presented. Three user designs have been implemented. The designs required an average of 4.8 vectors per module for a total of 2600 vectors per design. Test time was well below 1 second.

Acknowledgements

The authors gratefully acknowledge contributions from Jon Greene, Paul Jasmine, Kurt Kolkind, Sifuei Ku, Ken Joyner, Telle Whitney and Kitty Shaw.

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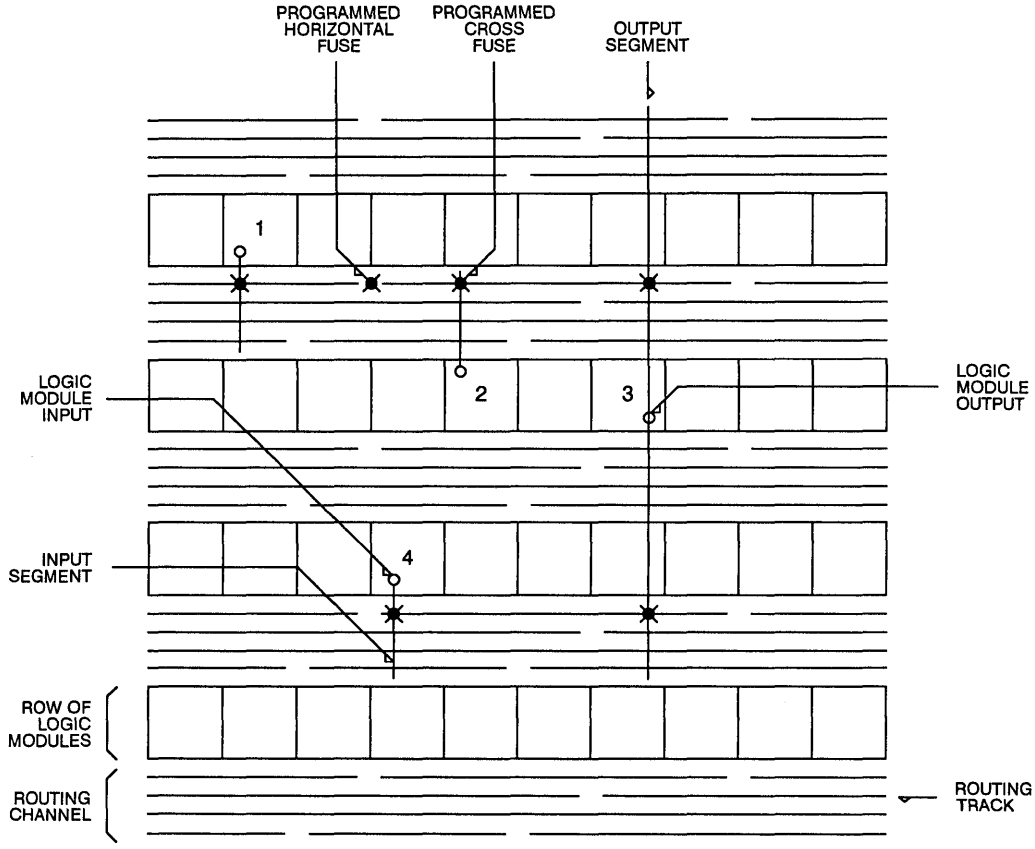


Figure 1. Channelled Gate Array Architecture of Antifuse Based FPGA

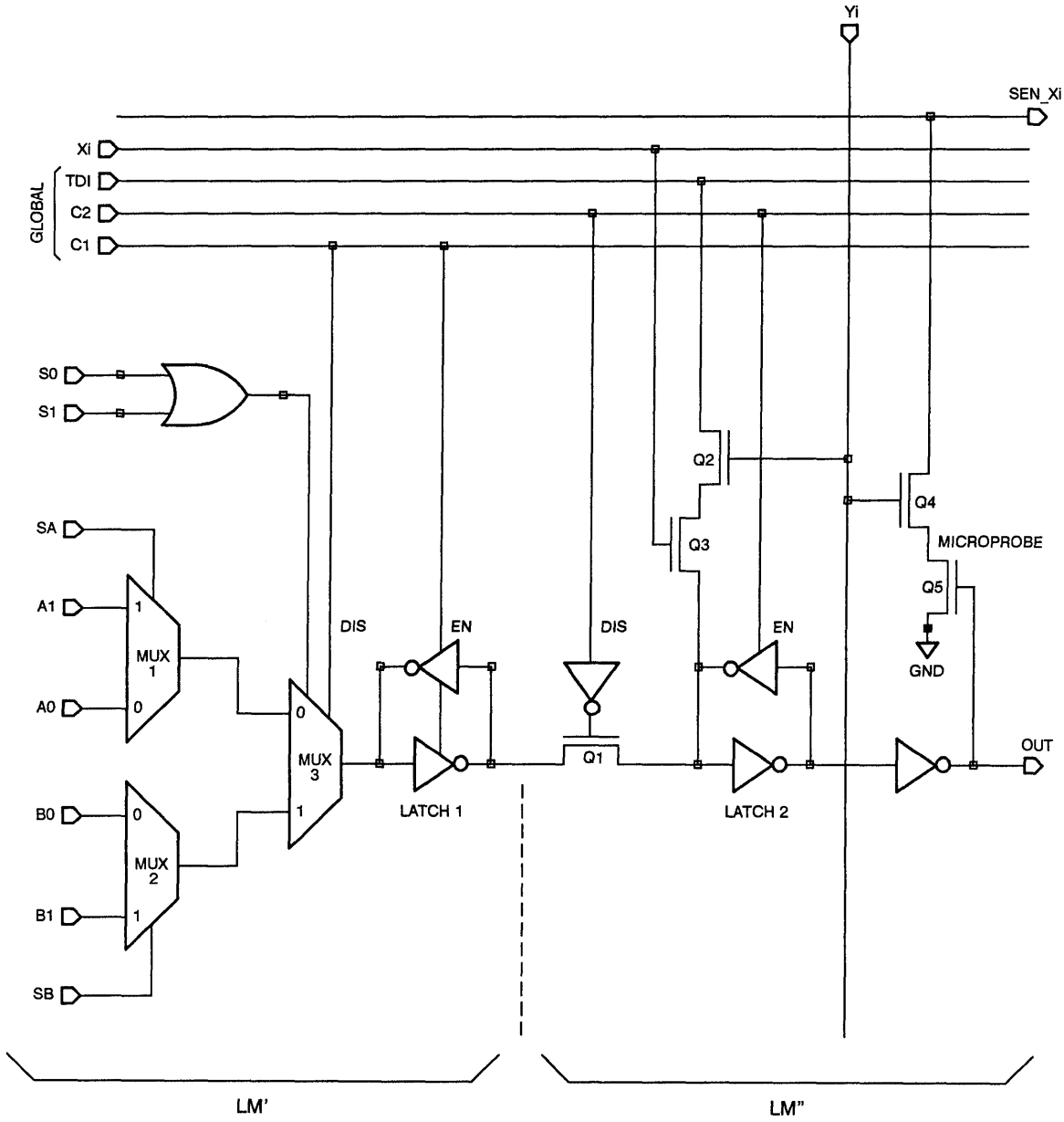


Figure 2. I/O Module

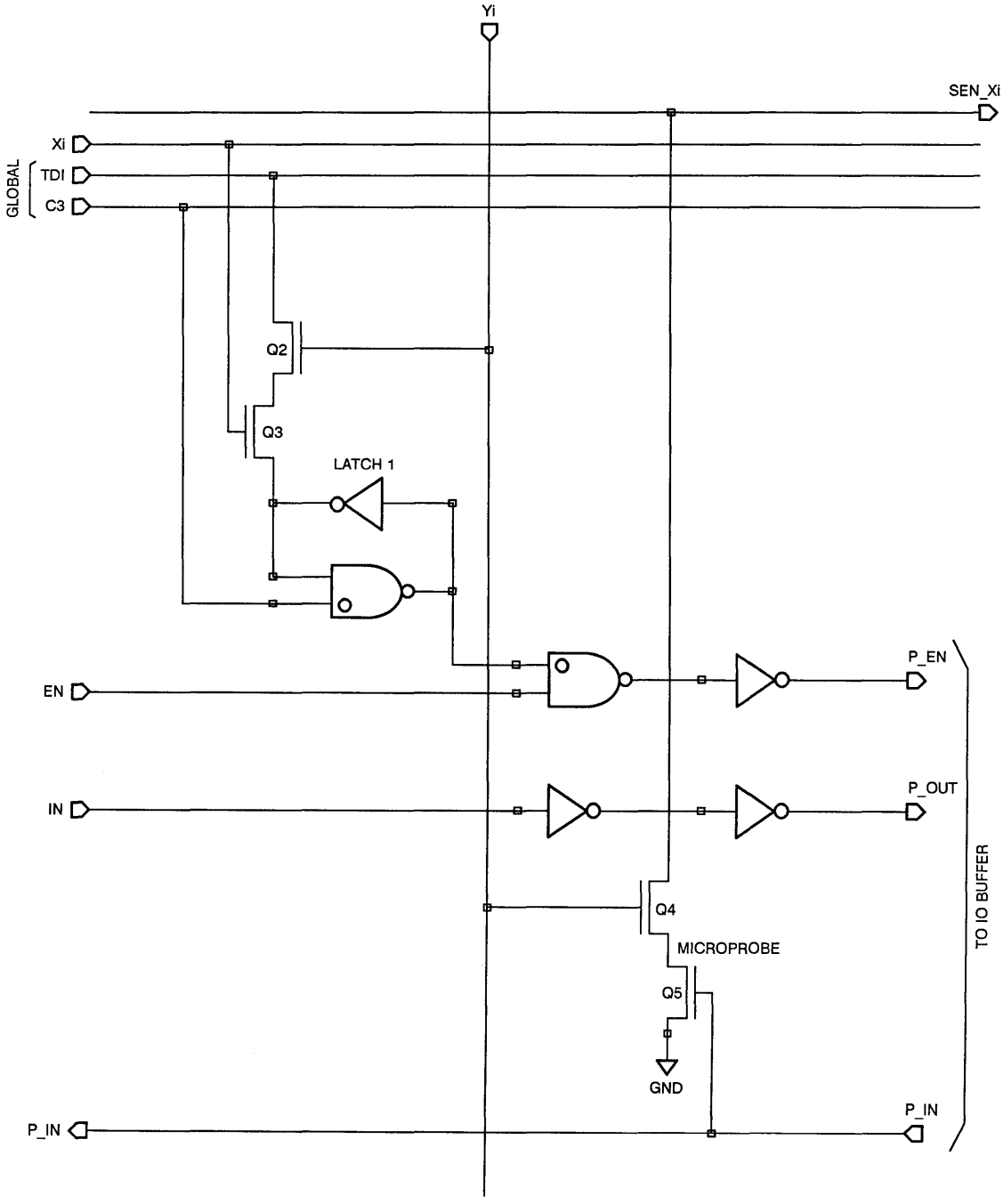


Figure 3. I/O Module

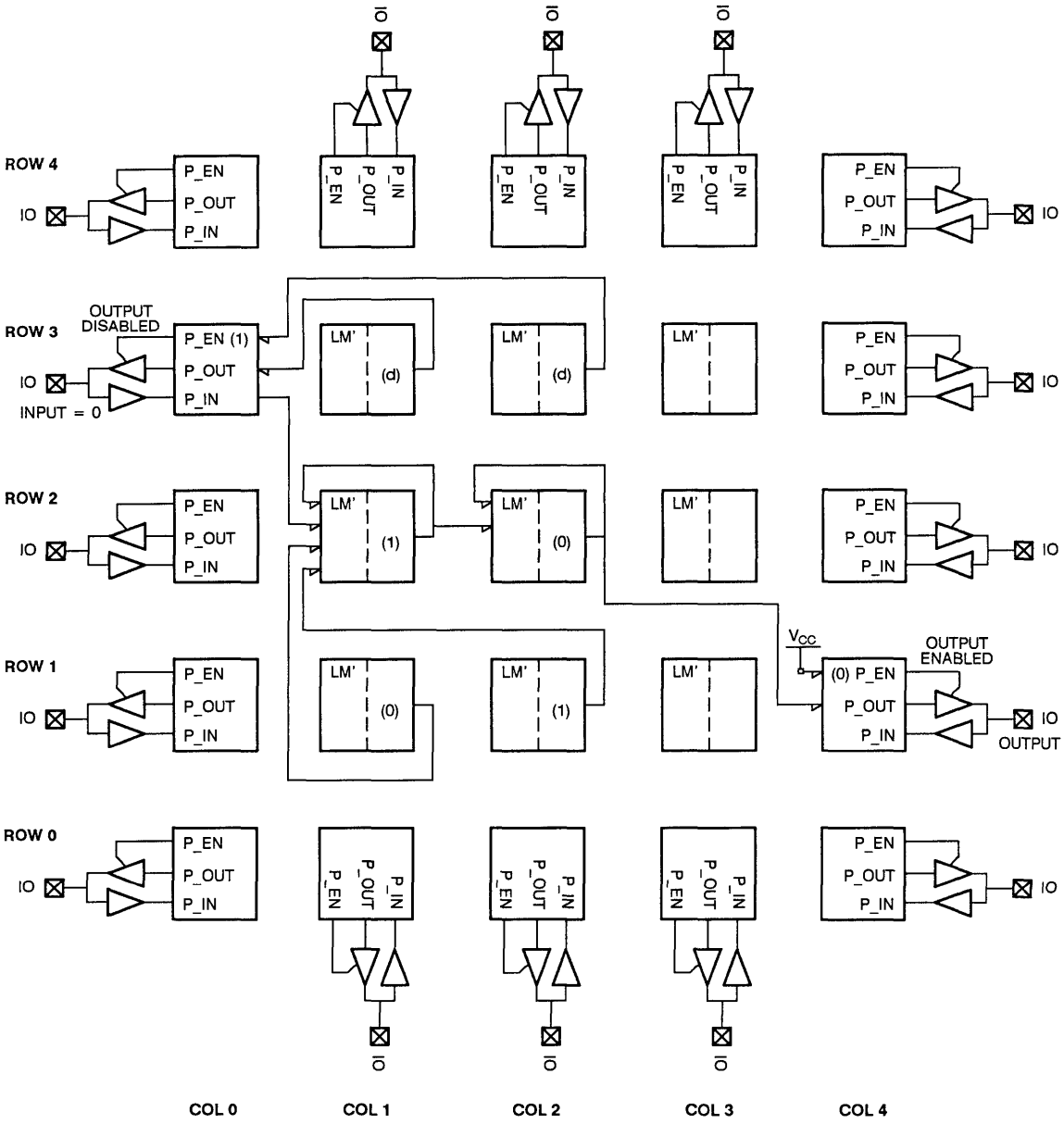


Figure 4. Logic and I/O Module Array

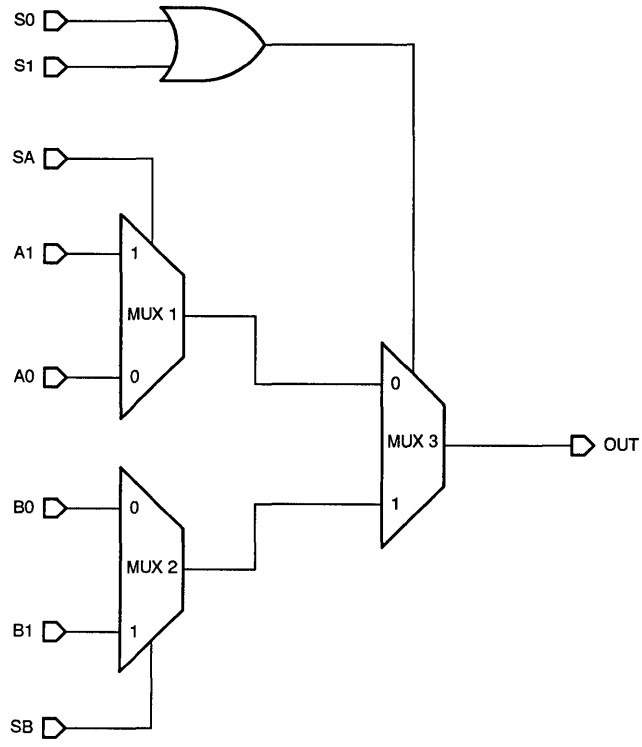


Figure 5. ATG Model of Logic Module

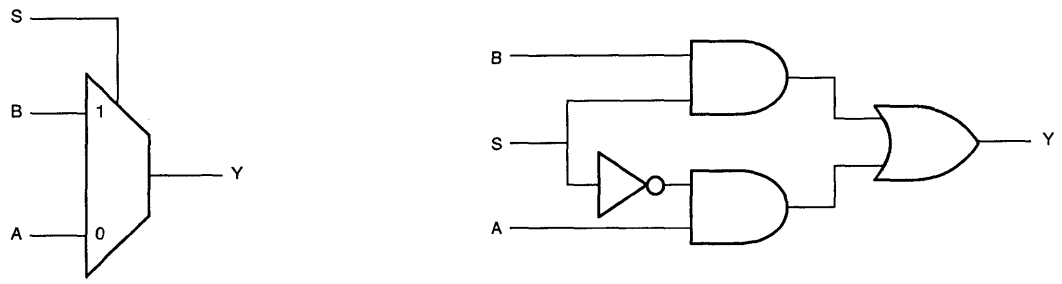


Figure 6. Multiplexor General Fault Modeling

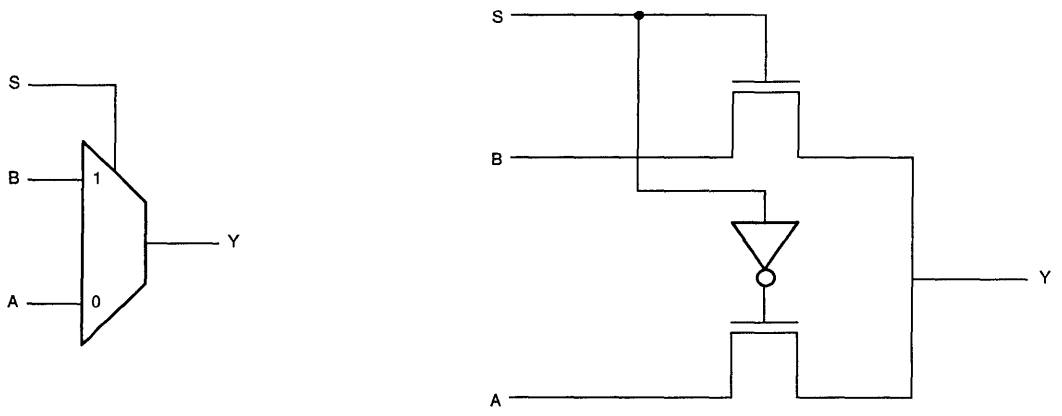
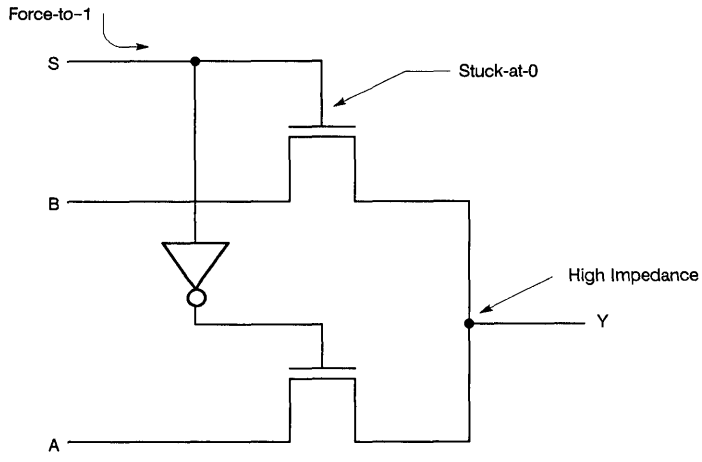


Figure 7. Realistic Multiplexor Model



Good Machine: Y = Value of B. Vector pair toggles B.
Bad Machine: Y = High impedance. Vector pair has no effect on value of Y.

Figure 8. Testing a MUX for Stuck-at-0 Fault with a Vector Pair

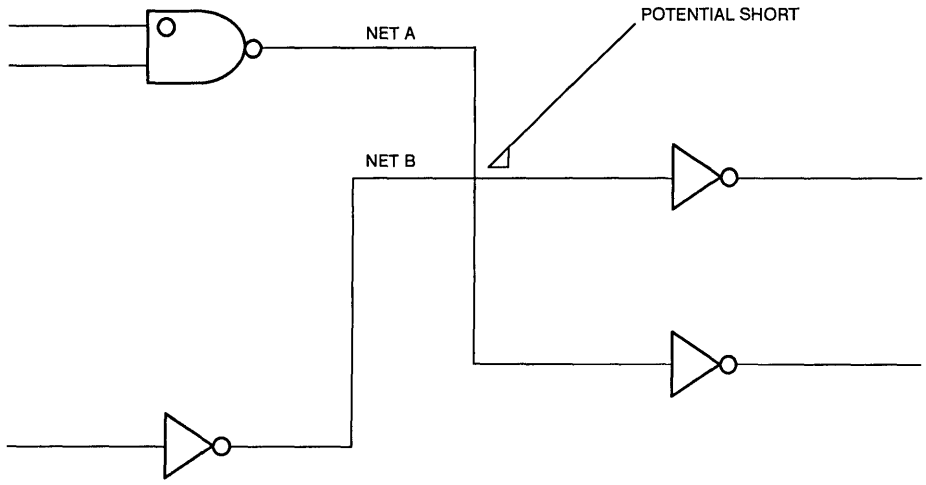
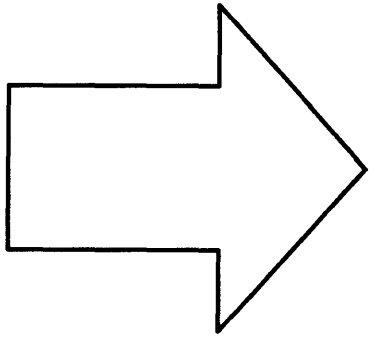


Figure 9. Layout of Two Independent Nets



Software Product Selector Guide

ALS System Selector Table

Host Environment	Actel System Part Number	Schematic Capture	Simulation	ACT1 FPGA Design Software	ACT2 FPGA Design	Activator 1 Programmer	Activator 2 Programmer	Actionprobe Diagnostics
386 PC with VIEWLOGIC®/ OrCAD/SDT III®	ALS-110	Includes VIEWDRAW® Supports OrCAD/SDT III	Optional VIEWSIM® Supports OrCAD/VST®	Included	Optional	Included	Optional	Included
386 PC with VIEWLOGIC/ OrCAD/SDT III	ALS-113	Includes VIEWDRAW Supports OrCAD/SDT III	Optional VIEWSIM Supports OrCAD/VST	Included	Optional	Included	Optional	Optional
386 PC with VIEWLOGIC/ OrCAD/SDT III	ALS-115	Includes VIEWDRAW Supports OrCAD/SDT III	Optional VIEWSIM Supports OrCAD/VST	Included	Optional	Optional	Optional	Optional
386 PC with VIEWLOGIC/ OrCAD/SDT III	ALS-210	Includes VIEWDRAW Supports OrCAD/SDT III	Optional VIEWSIM Supports OrCAD/VST	Included	Included	Not Required	Included	Included
386 PC with VIEWLOGIC/ OrCAD/SDT III	ALS-213	Includes VIEWDRAW Supports OrCAD/SDT III	Optional VIEWSIM Supports OrCAD/VST	Included	Included	Not Required	Included	Optional
386 PC with VIEWLOGIC/ OrCAD/SDT III	ALS-215	Includes VIEWDRAW Supports OrCAD/SDT III	Optional VIEWSIM Supports OrCAD/VST	Included	Included	Optional	Optional	Optional
MENTOR GRAPHICS CAE (HP Apollo®)	ALS-035	Supports NETED®	Supports QUICKSIM®	Included	Optional	Optional	Optional	Optional
MENTOR GRAPHICS CAE (HP Apollo)	ALS-230	Supports NETED	Supports QUICKSIM	Included	Included	Not Required	Included	Included
MENTOR GRAPHICS CAE (HP Apollo)	ALS-233	Supports NETED	Supports QUICKSIM	Included	Included	Not Required	Included	Optional
MENTOR GRAPHICS CAE (HP Apollo)	ALS-235	Supports NETED	Supports QUICKSIM	Included	Included	Optional	Optional	Optional
VALID LOGIC (Sun Microsystems™)	ALS-045	Supports VALIDGED®	Supports VALIDSIM®/ RAPIDSIM®	Included	Optional	Optional	Optional	Optional
VALID LOGIC (Sun Microsystems)	ALS-240	Supports	Supports VALIDGED RAPIDSIM	Included VALIDSIM/	Included	Not	Included Required	Included
VALID LOGIC (Sun Microsystems)	ALS-243	Supports	Supports VALIDGED RAPIDSIM	Included VALIDSIM/	Included	Not	Included Required	Optional
VALID LOGIC (Sun Microsystems)	ALS-245	Supports	Supports VALIDGED RAPIDSIM	Included VALIDSIM/	Included	Optional	Optional	Optional
VIEW LOGIC (Sun Microsystems)	ALS-055	VIEWDRAW	VIEWSIM (Supports)	Included (Supports)	Optional	Optional	Optional	Optional
VIEW LOGIC (Sun Microsystems)	ALS-250	VIEWDRAW	VIEWSIM (Supports)	Included (Supports)	Included	Not	Included Required	Included
VIEW LOGIC (Sun Microsystems)	ALS-253	VIEWDRAW	VIEWSIM (Supports)	Included (Supports)	Included	Not	Included Required	Optional
VIEW LOGIC (Sun Microsystems)	ALS-255	VIEWDRAW	VIEWSIM (Supports)	Included (Supports)	Included	Optional	Optional	Optional

Action Logic System FPGA Design Environment

Product Brief

Overview

The Action Logic™ System (ALS) is a high-productivity Computer Aided Engineering environment for designing with the ACT™ series of field programmable gate array devices. A menu-driven interface allows users to complete ACT designs, from concept to silicon, in hours without costly Non-Recurring Engineering costs. The system includes a software development environment and an Activator™ programmer, tester, and debugger. ALS is supported on most popular CAE platforms. Designers use their PCs or workstations to capture schematics; to simulate, verify, place and route; to perform timing analysis; to program and to debug the chip. On-line help screens and detailed reference manuals speed and simplify the design process.

To help you select the version of the Action Logic System that is correct for your needs, we will first explain the various modules that make up the software, and then show the platforms they run on.

Schematic Capture and Simulation

Users enter the design into the ACT device by drawing a schematic using the Actel Macro Library. When schematic capture is complete, functional simulation can be performed on the design. If the 386 PC Viewlogic version of the ALS is purchased, then the schematic capture system is provided by Actel. For all other platforms, Actel provides the Macro Library for an existing schematic capture system.

Gate Array Macro Library

The Actel Macro Library contains the logic function building blocks necessary to create a design. The library includes macros ranging in complexity from simple gates to complex functions. Each macro has a graphic symbol or icon. Hard macros also contain placement information, a netlist, and timing data.

Basic gates from the library are used to create soft macros, such as counters, adders, and decoders. The Actel Macro Library contains over 200 different macros.

Pin Editor

The Actel Pin Editor is an easy-to-use, menu-driven program for user assignment of logic I/Os and package pins. The Editor automatically scrolls a list of all user-designated I/Os. The user then chooses whether the pins should be assigned manually or automatically. To manually assign any pin to an I/O, the user simply enters the desired pin number next to the I/O node name. During each pin assignment, the Editor ensures that each pin is a valid package pin and is not already assigned to another chip I/O. Automatic I/O pin assignment is also available.

Design Validator

The Actel Design Validator examines an ACT design for adherence to design rules specific to the ACT device chosen for the design. Validation verifies routability and performs design rule checks prior to routing. The Validator produces error and information messages and system warnings regarding electrical rule violations such as excessive fan-out, shorted outputs, or unconnected inputs. For example, a warning message is issued if a net exceeds a fan-out of ten. An unconnected module input, however, produces an error message.

The Validator also provides statistical information about routability, logic module count, average fanout per net, and array utilization. After passing through the Validator, the design is free of electrical rule violations.

Automatic Place and Route

Fully automatic place and route software minimizes design delay by assigning macros to optimal locations in the chip. The system uses the design's netlist, critical net information, and I/O assignments to automatically place and route all the logic blocks within the circuit. No manual intervention is required, even at high device utilization.

The software provides the user with data on actual wire lengths, capacitive loading, and wiring congestion. The route program assigns the shortest possible net segments to connect the library macros with minimal delay, routing 100% of the nets automatically for 85% to 95% logic module utilization.

Timing Analysis

The timing analyzer (Timer) is an interactive tool that determines and highlights all critical and non-critical paths within a specified design. After the layout phase is completed, the Timer extracts accurate net delays. These delays are back annotated to the netlist and evaluated with the Timer or a CAE simulator. Using this information, the designer can optimize the design to meet timing specifications. The Timer accepts as input the design's netlist and delay information. The user directs the type of analysis and output. Delay reports generated by the timing analyzer using post-route numbers provide the final AC specifications for the design.
The user also can perform timing analysis using an optional CAE simulator supplied by vendors such as Viewlogic, Mentor or Cadence. The Action Logic System can generate a post-route annotation file which can be used by these simulators to provide accurate timing information.

Device Programming and Functional Test

Programming is controlled by the Activator programming system. The Activator 1 system only programs ACT 1 devices and is supplied with most of the entry level packages that support the ACT 1 family. The Activator 2 system programs both ACT 1 and ACT 2 families of devices and is supplied with most of the design packages that support both families.

Action Logic software generates a fuse map for the ACT device, which is used by the Activator for programming. A series of internal address registers that specify the programming element

2

(PLICE™ Antifuse) to be programmed are loaded automatically. A programming sequence is then initiated, creating a permanent link. These steps are repeated until all interconnections are made. The Activator also supports functional testing using an I/O test vector file.

In addition, Actel supports third party programmers such as the data I/O Unisite®.

In-Circuit Test and Debug

Once the device is programmed and functionally verified, it is ready for operation in the user's system. Actionprobe™ diagnostic tools may then be used to further evaluate circuit integrity. The Actionprobe diagnostic tool is an adapter to the Activator programmer which connects to the ACT device socket in the target system. Under full control of the Actionprobe software, any two of the internal networks can be selected to be brought out on the two diagnostic probe pins for analysis. Timing and waveform analysis is then accomplished using an oscilloscope or a logic analyzer. Versions of the Actionprobe system are available for both the Activator 1 and the Activator 2 programming systems.
Optional features are:

ALES Logic Optimizer

The Actel Logic Optimizer (ALES™ 1) allows designers to combine schematics with PAL) equations (PALASM™ 2, ABEL™, CUPL™). The synthesized logic can then be simulated and integrated into a hierarchical design with emphasis on optimizing either area or delay. ALES is available for the 386 PC platform, and the Apollo and Sun workstations.

Synopsys Libraries

Actel supplies a technology library for the Synopsys logic synthesis environment. It allows designers to capture Actel designs by entering VHDL/HDL format source files into Synopsys' design compiler. The design compiler outputs an EDIF netlist, which is read by the Actel supplied EDIF reader in the ALS design environment. Versions of the Synopsys libraries are available for all the design platforms except the 386 PC.

Annual Support/Update Program

An Annual Support agreement ensures that the software you purchase is up to date and that you get priority service when you have problems or technical questions. It also ensures that the software you have supports the most recently released devices and packages. Software upgrades are typically released twice a year and are sent to Annual Support agreement holders free of charge.

The Support/Update program also gives you access to technical expertise via the Actel Technical Hotline. Applications engineers are available anytime during Actel's regular working hours to answer your questions or fix your problems. You also have access to Actel's on-line Bulletin Board System. Services available via the BBS are:

- Known Bug List
- Software Corrections and Updates
- User-designed Macro Library.
- Design file Uploading and Downloading for troubleshooting purposes
- Message service for communicating with applications engineers
- User Forum for communicating with other users of Actel products

Design Platforms

Versions of the Action Logic System are available to run on a variety of platforms. Because not all users will need all of the capabilities (or want all the expense) provided by the complete system, Actel has made several versions of the ALS available for each platform. These versions include:

- ACT 1 software support only
- ACT 1 software support and the Activator 1 programmer
- ACT 1 software support, the Activator 1 programmer, and the Actionprobe diagnostics
- ACT 1 and ACT 2 software support
- ACT 1 and ACT 2 software support and the Activator 2 Programmer
- ACT 1 and ACT 2 software support, the Activator 2 programmer, and the Actionprobe diagnostics

The system can be upgraded to add missing functions whenever the customer desires.

The basic platforms supported are:

Viewlogic and OrCAD on 386 PC. This system is designed to run on an 80386 or 80486 processor based IBM-compatible PC running DOS. Actel provides the Viewlogic Viewdraw schematic capture package, the Actel Macro Library, and the Action Logic System design modules. Viewsim simulation support is available from Actel as an option. Libraries supporting the OrCAD schematic capture system are also provided.

Mentor Graphics on HP/Apollo Workstation. This version integrates with existing design systems utilizing Mentor Graphics' NETED schematic capture and QuickSim simulator running on HP/Apollo workstations. Actel provides the Actel Macro Libraries and the Action Logic System design software designed to link directly with the Mentor Graphics netlist format.

VALID Logic on Sun Workstation. This version integrates with existing design systems utilizing Valid's ValidGED schematic capture and ValidSIM and RapidSIM simulator running on Sun Workstations. Actel provides the Actel Macro Libraries and the Action Logic System design software. Design files can be exported directly from Valid's netlist format.

Viewlogic on Sun Workstations. Provides ACT 1 or ACT 1 and ACT 2 design and programming capability for an existing Viewlogic design system running on a Sun Workstation. Actel provides the Actel Macro Libraries and the Action Logic System design software. Design files can be exported directly from Viewlogic's netlist format into the Actel ALS system.

A selector guide was provided at the front of this chapter to help you select the version of the software that best suits your needs. Complete datasheets on each version of the software follow.

Action Logic System for 386 PC Platform

Product Brief

Action Logic System Software and Hardware with Viewlogic Schematic Capture for ACT 1 and ACT 2 Designs

Development System Capabilities

ACT 1 and ACT 2 FPGA Design, Programming and Design Verification/Probe capability for 80386 based IBM-PCs and compatibles.

Actel's Action Logic™ System (ALS) for the 386 PC platform is a low-cost Field Programmable Gate Array design and programming system for the ACT™ 1 and ACT™ 2 families. The software included with the system consists of Viewlogic's 3150 schematic capture software and the Actel design software and ACT 1 and ACT 2 Macro Libraries for the Viewlogic environment. Also included is the Actel Activator® Programmer and debugger, and the Actionprobe. diagnostic tools. The ACT Macro Library integrates with the Viewlogic schematic capture and simulator (optional) packages to provide all of the elements for a complete FPGA design, simulation, and programming environment. Design files can be exported from Viewlogic directly into the ALS environment.

After importing the files, the ALS Design Validator verifies design rule compliance by completing an electrical rules check and provides statistical use information such as utilization percentage and average fan-out. After validation, the automatic place and route software configures the device to the engineer's design. Through the use of the Timer, an engineer can check circuit timing before and after the place and route. Once the design is optimized, the Activator programmer programs the proper antifuses to configure the FPGA. The debugger software allows the designer to check the functionality of the FPGA by running test vectors through the device using the Activator programmer. The Actionprobe hardware and software provides 100% real-time observability of internal nodes while the FPGA is in the target system.

For users who do not need all of these capabilities, versions of the development system are offered without all of the features of the complete system. The hardware and software can be upgraded later as the user's needs change.

The Action Logic System for the 386 PC platform also includes the OrCAD/SDT and OrCAD/VST interface and macro libraries. These allow the system to work with an installed copy of OrCAD/SDT Version 3.1 or higher.

Software Requirements

MS-DOS 3.0 (or later)

Note: OrCAD users need SDT III Release 3.1 or 3.2.
Viewlogic users need Viewlogic release 3.2 or 4.0.

Hardware Requirements

386-Based PC-AT with:

- 4 Megabytes RAM (8Mb recommended)
- One Parallel Port
- One RS-232C Port (COM1 or COM2)
- 40 Megabyte Hard Disk (40 Mb recommended)
- 1.2 or 1.44 Megabyte Floppy Drive
- VGA, EGA, or Monochrome Graphics Card
- Vacant 1/2 Card AT Bus Slot

Simulators

ALS-016: Viewlogic's 3350 Simulator. Fully integrated to Viewlogic's schematic capture and Actel's ALS design system for complete FPGA simulation. The ALS-016 is a menu-driven interactive simulator that provides pre-layout and post-layout timing simulation with delay back annotation to verify performance after layout. Advanced interactive debugging tools help designers quickly find and eliminate problems.

ALS-016S: Annual Support Fee, per system. Order with ALS-016.

ALS-017: Viewlogic's low-cost simulator. Similar in capabilities to the ALS-016 with a maximum simulation capability of 3000 gates.

ALS-017S: Annual Support Fee, per system. Order with ALS-017.

ALES 1 Logic Optimizer

ALS-114: Actel Logic Optimizer (ALES™ 1) allows designers to combine schematics with PAL® equations (PALASM®2, ABEL, CUPL). The synthesized logic can be simulated and integrated into a hierarchical design with emphasis on optimizing either area or delay.

ALS-114S: Annual Support Fee, per system. Order with ALS-114.

Schematic Generator

ALS-VL-001: Viewlogic's Viewgen schematic generator. Allows Viewdraw schematics to be created from an Actel or Viewlogic netlist.

Activator 2 Programming Modules

ALS-280:	100 QFP (ACT 1)	ALS-287:	176PGA
ALS-281:	44PLCC	ALS-288:	84 PLCC (ACT 2)
ALS-282:	68PLCC	ALS-289:	100 PGA (ACT 2)
ALS-283:	84PLCC	ALS-290:	100QFP (ACT 2)
ALS-284:	84PGA	ALS-292:	144QFP
ALS-285:	84QFP	ALS-293:	160QFP
ALS-286:	132PGA	ALS-294:	172QFP

ALS System Selector Table

ACTEL System Part Number	ACT 1 FPGA Design Software	ACT 2 FPGA Design Software	Activator 1 Programmer	Activator 2 Programmer	Actionprobe Diagnostics
ALS-110	Included	Optional	Included	Optional	Included
ALS-113	Included	Optional	Included	Optional	Optional
ALS-115	Included	Optional	Optional	Optional	Optional
ALS-210	Included	Included	Not Required	Included	Included
ALS-213	Included	Included	Not Required	Included	Optional
ALS-215	Included	Included	Optional	Optional	Optional

Software and Hardware upgrades are available for Actel systems. Please contact your local sales representative for details and pricing.

Action Logic System for Mentor Graphics Design System

Product Brief

Action Logic System Software and Hardware for Existing Mentor Graphics Design System for ACT 1 and ACT 2 Designs

Development System Capabilities

ACT 1 and ACT 2 FPGA Design, Programming, and Design Verification/Probe Capability for Existing Mentor Graphics Design System on HP/Apollo Workstation

Description

The Action Logic System (ALS) is a complete ACT 1 and ACT 2 FPGS design, debugging, and programming system (for Mentor Graphics on HP/Apollo workstations). The ALS-230 macro library fully integrates with existing Mentor Graphics design systems utilizing Mentor Graphics' NETED schematic capture and QuickSim simulator. The design files can be exported from Mentor Graphics' netlist format directly into the Actel ALS environment, which is resident on the HP/Apollo workstation.

After importing the files, the ALS Design Validator verifies design rule compliance by completing an electrical rules check and provides statistical use information such as utilization percentage and average fanout. After validation, the automatic place and route software configures the gate array to the engineer's design. Through the use of the Timer, an engineer can check circuit timing for the place and route. Once the design is optimized, the Activator 2 Programmer programs the proper antifuses to configure the FPGA. The Activator 2 can program up to 4 devices simultaneously in approximately one-half the time of the Activator 1 Programmer. Modular approach allows for different packages to be programmed by switching programming modules. Lastly, the Actionprobe diagnostics hardware and software provides 100% real time observability of internal nodes while the FPGA is running in the target system.

For users who do not need all of these capabilities, versions of the development system are offered without all of the features of the complete system. The hardware and software can be upgraded later as the user's needs change.

Software Components

ACT 1 / ACT 2 FPGA Design System for Apollo:

- Macro Library
- Automatic Placement and Routing
- Timing Analysis
- Design Verification and In-Circuit Probe Software

Hardware Components

- Activator 2 Programmer
- Actionprobe Diagnostic Pod

Software Requirements

- Mentor Graphics Idea Station Release 7.0 (for Capture and Design) and AEGIS Release 10.3 or Greater

Hardware Requirements

- HP/Apollo series DN3000, DN4000, 400S, AND 400T

Options

ALES Logic Optimizer

ALS-134: Actel Logic Optimizer (ALES 1) for Mentor Graphics on HP/Apollo allows designers to combine schematics with PAL equations (PALASM2, ABEL, CUPL). The synthesized logic can be simulated and integrated into a hierarchical design with emphasis on optimizing either area or delay.

ALS-134S: Annual Support Fee, per system. Order with ALS-134.

Synthesis

ALS-SYN-DN: Actel's technology libraries for the Synopsys logic synthesis environment. Allows designers to capture Actel designs by entering VHDL/HDL format source files in Synopsys' design compiler. The design compiler outputs an EDIF format netlist which is read by the Actel supplied EDIF reader in the Actel ALS design environment. The remaining design validation, placement and routing, and programming steps are completed in the ALS environment.

Activator 2 Programming Modules

ALS-280:	100 QFP (ACT 1)	ALS-287:	176PGA
ALS-281:	44PLCC	ALS-288:	84 PLCC (ACT 2)
ALS-282:	68PLCC	ALS-289:	100 PGA (ACT 2)
ALS-283:	84PLCC	ALS-290:	100QFP (ACT 2)
ALS-284:	84PGA	ALS-292:	144QFP
ALS-285:	84QFQ	ALS-293:	160QFP
ALS-286:	132PGA	ALS-294:	172QFP

2

ALS System Selector Table

ACTEL System Part Number	ACT 1 FPGA Design Software	ACT 2 FPGA Design Software	Activator 1 Programmer	Activator 2 Programmer	Actionprobe Diagnostics
ALS-035	Included	Optional	Optional	Optional	Optional
ALS-230	Included	Included	Not Required	Included	Included
ALS-233	Included	Included	Not Required	Included	Optional
ALS-235	Included	Included	Optional	Optional	Optional

Software and Hardware upgrades are available for Actel systems. Please contact your local sales representative for details and pricing.

Action Logic System for Valid Logic Design System

Product Brief

Action Logic System Software and Hardware for Existing Valid Logic Design System for ACT 1 and ACT 2 Designs

Development System Capabilities

ACT 1 and ACT 2 FPGA Design, Programming, and Design Verification/Probe Capability for Existing Valid Logic Design System on Sun Workstation

Description

The Action Logic System (ALS) is a complete ACT 1 and ACT 2 FPGA design, debugging, and programming system (for Valid Logic on Sun workstations). The ALS-240 macro library fully integrates with existing Valid Logic design systems utilizing Valid's ValidGED schematic capture and ValidSIM/RapidSIM simulator. The design files can be exported from Valid's netlist format directly into the Actel ALS environment, which is resident on the Sun workstation.

After importing the files, the ALS Design Validator verifies design rule compliance by completing an electrical rules check and provides statistical use information such as utilization percentage and average fanout. After validation, the automatic place and route software configures the gate array to the engineer's design. Through the use of the Timer, an engineer can check circuit timing for the place and route. Once the design is optimized, the Activator 2 Programmer programs the proper antifuses to configure the FPGA. The Activator 2 can program up to 4 devices simultaneously in approximately one-half the time of the Activator 1 Programmer. Modular approach allows for different packages to be programmed by switching programming modules. Lastly, the Actionprobe diagnostics hardware and software provides 100% real time observability of internal nodes while the FPGA is running in the target system.

For users who do not need all of these capabilities, versions of the development system are offered without all of the features of the complete system. The hardware and software can be upgraded later as the user's needs change.

Software Components

ACT 1 / ACT 2 FPGA Design System for Sun:

- Macro Library
- Automatic Placement and Routing
- Timing Analysis
- Design Verification and In-Circuit Probe Software

Hardware Components

- Activator 2 Programmer
- Actionprobe Diagnostic Pod

Software Requirements

- Sun OS 4.0.3 or 4.1

Hardware Requirements

- Sun CAE Workstation

Options

ALES Logic Optimizer

ALS-144: Actel Logic Optimizer (ALES 1) for Valid on Sun allows designers to combine schematics with PAL equations (PALASM2, ABEL, CUPL). The synthesized logic can be simulated and integrated into a hierarchical design with emphasis on optimizing either area or delay.

ALS-144S: Annual Support Fee, per system. Order with ALS-144.

Synthesis

ALS-SYN-S4: Actel's technology libraries for the Synopsys logic synthesis environment. Allows designers to capture Actel designs by entering VHDL/HDL format source files in Synopsys' design compiler. The design compiler outputs an EDIF format netlist which is read by the Actel supplied EDIF reader in the Actel ALS design environment. The remaining design validation, placement and routing, and programming steps are completed in the ALS environment.

Activator 2 Programming Modules

ALS-280:	100 QFP (ACT 1)	ALS-287:	176PGA
ALS-281:	44PLCC	ALS-288:	84 PLCC (ACT 2)
ALS-282:	68PLCC	ALS-289:	100 PGA (ACT 2)
ALS-283:	84PLCC	ALS-290:	100QFP (ACT 2)
ALS-284:	84PGA	ALS-292:	144QFP
ALS-285:	84QFP	ALS-293:	160QFP
ALS-286:	132PGA	ALS-294:	172QFP

2

ALS System Selector Table

ACTEL System Part Number	ACT 1 FPGA Design Software	ACT 2 FPGA Design Software	Activator 1 Programmer	Activator 2 Programmer	Actionprobe Diagnostics
ALS-045	Included	Optional	Optional	Optional	Optional
ALS-240	Included	Included	Not Required	Included	Included
ALS-243	Included	Included	Not Required	Included	Optional
ALS-245	Included	Included	Optional	Optional	Optional

Software and Hardware upgrades are available for Actel systems. Please contact your local sales representative for details and pricing.

Action Logic System for Viewlogic/Sun Design System

Product Brief

Action Logic System Software and Hardware for Existing Viewlogic Design System for ACT 1 and ACT 2 Designs

Development System Capabilities

ACT 1 and ACT 2 FPGA Design, Programming, and Design Verification/Probe Capability for Existing Viewlogic Design System on Sun Workstation

Description

The Action Logic System (ALS) is a complete ACT 1 and ACT 2 FPGA design, debugging, and programming system (for Viewlogic on Sun workstations). The ALS-250 macro library fully integrates with existing Viewlogic design systems utilizing Viewlogic's Viewdraw schematic capture and Viewsim simulator. The design files can be exported from Viewlogic's netlist format directly into the Actel ALS environment, which is resident on the Sun workstation.

After importing the files, the ALS Design Validator verifies design rule compliance by completing an electrical rules check and provides statistical use information such as utilization percentage and average fanout. After validation, the automatic place and route software configures the gate array to the engineer's design. Through the use of the Timer, an engineer can check circuit timing for the place and route. Once the design is optimized, the Activator 2 Programmer programs the proper antifuses to configure the FPGA. The Activator 2 can program up to 4 devices simultaneously in approximately one-half the time of the Activator 1 Programmer. Modular approach allows for different packages to be programmed by switching programming modules. Lastly, the Actionprobe diagnostics hardware and software provides 100% real time observability of internal nodes while the FPGA is running in the target system.

For users who do not need all of these capabilities, versions of the development system are offered without all of the features of the complete system. The hardware and software can be upgraded later as the user's needs change.

Software Components

ACT 1 / ACT 2 FPGA Design System for Sun:

- Macro Library
- Automatic Placement and Routing
- Timing Analysis
- Design Verification and In-Circuit Probe Software

Hardware Components

- Activator 2 Programmer
- Actionprobe Diagnostic Pod

Software Requirements

- Viewlogic Workview 6000, Version 4.1
- Sun OS 4.0.3 or 4.1

Hardware Requirements

- Sun CAE Workstation

Options

ALES Logic Optimizer

ALS-144: Actel Logic Optimizer (ALES 1) for Viewlogic on Sun allows designers to combine schematics with PAL equations (PALASM2, ABEL, CUPL). The synthesized logic can be simulated and integrated into a hierarchical design with emphasis on optimizing either area or delay.

ALS-144S: Annual Support Fee, per system. Order with ALS-144.

Synthesis

ALS-SYN-S4: Actel's technology libraries for the Synopsis logic synthesis environment. Allows designers to capture Actel designs by entering VHDL/HDL format source files in Synopsys' design compiler. The design compiler outputs an EDIF format netlist which is read by the Actel supplied EDIF reader in the Actel ALS design environment. The remaining design validation, placement and routing, and programming steps are completed in the ALS environment.

Activator 2 Programming Modules

ALS-280:	100 QFP (ACT 1)	ALS-287:	176PGA
ALS-281:	44PLCC	ALS-288:	84 PLCC (ACT 2)
ALS-282:	68PLCC	ALS-289:	100 PGA (ACT 2)
ALS-283:	84PLCC	ALS-290:	100QFP (ACT 2)
ALS-284:	84PGA	ALS-292:	144QFP
ALS-285:	84QFP	ALS-293:	160QFP
ALS-286:	132PGA	ALS-294:	172QFP

ALS System Selector Table

ACTEL System Part Number	ACT 1 FPGA Design Software	ACT 2 FPGA Design Software	Activator 1 Programmer	Activator 2 Programmer	Actionprobe Diagnostics
ALS-055	Included	Optional	Optional	Optional	Optional
ALS-250	Included	Included	Not Required	Included	Included
ALS-253	Included	Included	Not Required	Included	Optional
ALS-255	Included	Included	Optional	Optional	Optional

Software and Hardware upgrades are available for Actel systems. Please contact your local sales representative for details and pricing.

Activator™ 2 Programmer/Tester/Debugger

Product Brief

Features

- Supports ACT™ 1 and ACT 2 Device Families
- Interfaces to 386™ PC, Sun™ and Apollo™ Workstations using a SCSI Bus
- Runs Adapter Modules for Each Package/Family Combination
- Up to Two Times Faster Than Activator™ 1 for ACT 1 Programming
- Supports Functional Verification with Actionprobe™ Diagnostic Pod
- Simultaneously Programs a Single Pattern in Up To Four Identical Devices
- Includes In-Circuit Probing of Up To Four Devices Simultaneously

Product Description

Activator 2 is Actel's state-of-the-art desktop programmer. It utilizes Actel's Action Logic™ System (ALS) software and PLICE™ antifuse technology to program custom-engineered devices from Actel's ACT 1 and ACT 2 device families. SCSI connectors, shipped with the unit, provide a convenient connection for 386 PC, Sun, and Apollo workstation support. Customized adapter modules for each device type permit easy interchange of programmable devices. Programming, Test, and Debug execute up to two times faster than on the Activator 1; users can program up to four devices at one time. The accompanying diagnostic pod and ALS debug software support observation of all internal signals.

The unit is software-driven, providing flexibility of application and a built-in barrier to obsolescence. Independently powered, the unit provides desktop device programming, functional testing, and in-circuit debugging.

The unit supports different CAE platforms using SCSI connectors.

The Activator 2 may operate with four different adapter modules inserted or with three of the sockets as slaves to the first, permitting simultaneous programming of four identical devices. The Activator 2 then addresses any one of the sockets for programming.

Activator 2 Base Unit

The base unit contains the control board and the analog board. The LED display on the top of the programmer shows when the unit receives power. Four adapter ports located on the top of the base unit accept the different adapter modules for each device type. The adapter ports are identical, allowing interchangeability of modules. SCSI connectors are located on the back of the unit.

The Adapter Module

The adapter modules customize pin configurations for each device; the user need only switch adapter modules to program another device. All four ports may be used simultaneously when programming identical devices. The adapter modules are compact and sturdy. Any module may be used on any available port.

The Diagnostic Pod

The diagnostic pod supports ALS diagnostics and connects to the programmer via cable. The Activator permits the user to view any internal circuit activity through Actel's on-chip diagnostic ports. Up to four pods may be used simultaneously. A six-foot cord connects the pod to the base unit and provides debugging flexibility.

Using Actionprobe™ Diagnostic Tools

Applications Note

Introduction

Actel's probe pin circuitry permits external monitoring of ACT™ 1 and ACT™ 2 device internal signals *after* device programming. This unique diagnostic feature allows 100 percent observability of a device. Observability reduces the time required for design verification and test vector generation; it also facilitates system troubleshooting. One hundred percent observability of all internal device signals is unique to Actel field programmable gate arrays; this feature is not available in conventional masked gate arrays or programmable logic devices.

Two dedicated probe pins, PRA and PRB, provide this observability on ACT family devices. Actel's Actionprobe™ software and Actionprobe diagnostics hardware permit the connection of any two signal nodes on the device to the probe pins. Signal node assignments may be changed freely under software control.

Setup

The Activator™1 and the Activator 2 programmer each have their own Actionprobe hardware.

Actionprobe 1 hardware consists of a tower probe with a footprint of the selected package. A socket on top of the tower probe holds the programmed ACT device in place. The Actionprobe 1 unit, with a programmed ACT device is then plugged directly into a system board.

The Actionprobe hardware for the Activator 2 programmer is a diagnostic pod that connects to the programmer via cable. The pod is connected to dedicated test points in the target system using several "flying lead" connections. The Activator 2 programmer supports up to four Actionprobe diagnostic pods.

In both cases the device is verified and debugged in the target board as it receives real-time stimuli from the system.

The Activator Programmer drives the control signals SDI, DCLK, MODE, and GND via a flat ribbon cable. The MODE pin determines whether the device is in debug mode. SDI receives the serial addresses of the internal nodes from the Activator bus board. DCLK clocks the serial address into the device. When the device is being debugged in-circuit, SDI, DCLK, and MODE are terminated to ground through a >10 kΩ resistor. Probe pins may be connected directly to a logic analyzer or oscilloscope.

In-Circuit Probing

Changing the signal nodes is done simply by changing node names with the Debugger software. The newly assigned signals are connected automatically to the probe pins. Internal signals up to 10 MHz can be monitored externally. The internal signal passes through an inverting buffer before reaching the probe pin.

The "ICP" (In-Circuit Probing) command connects the probe pins to internal nodes. The syntax is :

ICP node_1 node_2

where "node_1" (node name) is connected electrically to PRA, and "node_2" is connected electrically to PRB.

Probe Calibration

The probe circuitry does not introduce any additional loading to the design, so the AC characteristic of the observed internal nodes remains unchanged. And, because probe propagation delay is independent of layout, probe delay remains unchanged for all points in the device.

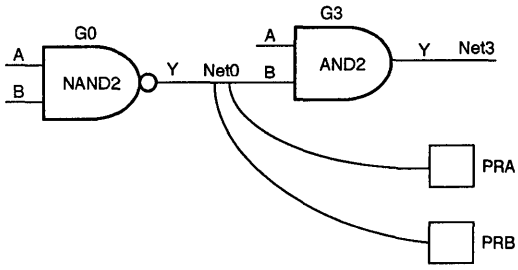
The skew of the probe pins can be measured, then used to calibrate for accurate measurement of propagation delay. When both probe pins are assigned to the same point on the device, the delay difference measured is the skew of the probe pins. This skew is subtracted from subsequent delay measurements in the circuit. In Figure 1a, for example, both PRA and PRB are connected electrically to node Net0. The delay difference is the skew, calculated as $t_{SK} = t_{PRA} - t_{PRB}$. Using the Debugger software, the slower probe (PRA) is assigned to node Net3. Figure 1b shows this configuration. In this example, actual propagation delay is the measured delay time between the output of G0 and the output of G3, minus the probe skew time. Actual delay is calculated as:

$t_{PD} = t_{PRA} - t_{PRB} - t_{SK}$.

Note: Due to the propagation delay difference between rising and falling signals, both probe pin signals must be either rising or falling when they are used to calibrate for delay measurements.

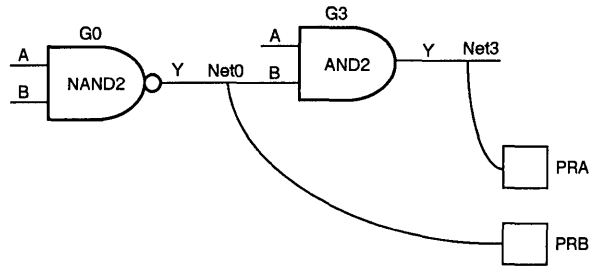
Pin Assignment for Dedicated I/O Pins

During device verification, dedicated pins SDI, DCLK, PRA, and PRB are assigned as special I/O pins. These pins should be assigned as non-critical so that the design is functional without them. After device verification, these pins can be assigned as regular I/Os by programming the security fuses. This disables the probe pins to prevent unauthorized device probing.



$t_{SK} = t_{PRA} - t_{PRB}$

Figure 1a. Measuring Skew of Probe Pins



$t_{PD} = t_{PRA} - t_{PRB} - t_{SK}$

Figure 1b. Calibrating for Accurate Propagation Delay Measurement

Using the Actel Debugger as a Functional Tester

Applications Note

Introduction

Actel's Activator™ programming and diagnostics unit, together with Actel's Debugger software, provide powerful tools to functionally test an ACT™ device. Device debugging begins after design configuration and device programming. Debugging is performed with the device inserted in the Activator unit. The user accesses Debugger software from the Action Logic™ System (ALS) main menu.

Debugger functional test allows the user to observe any internal node of the device. The user defines the device inputs with Debugger menu commands, with a command file, or with any combination of the two. Command files and test vector files are created with an ASCII text editor, then loaded into the Debugger. User-defined macros may be created in a command file, then executed in the Debugger.

This applications note shows Debugger commands for a sample design. The sample design is Actel's TT269 (TTL 74269), an eight-bit binary loadable up/down counter with count enable. Figure 1 shows the sample design; Table 1 shows the truth table for the part. P0 through P7 are parallel load inputs; Q0 through Q7 are counter outputs; CLK is the counter clock; UD is the up/down count selector. Internal nodes (nets) should be labeled during design capture for easy reference during debugging.

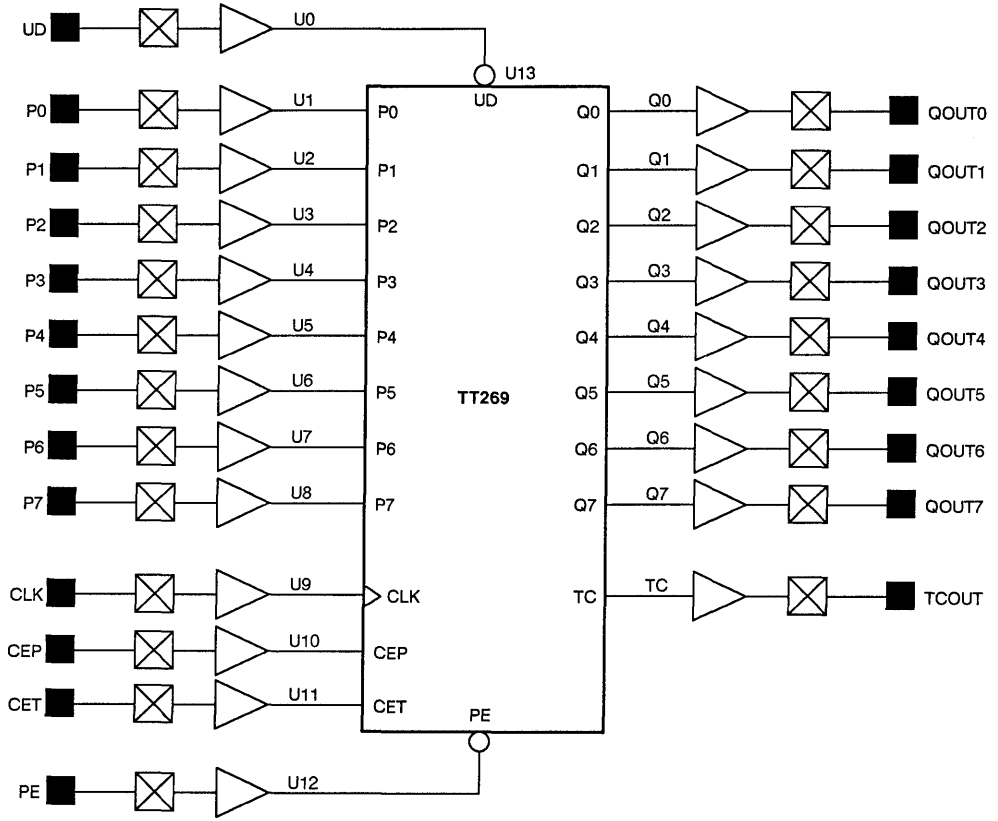


Figure 1. TT269

Table 1. TT269 Truth Table

Inputs						Outputs	
PE	CEP	CET	UD	P[7:0]	CLK	Q[7:0]	TC
0	X	X	X	0	↑	0	1
0	X	X	X	FF	↑	FF	0
1	X	1	X	X	↑	Hold	
1	1	X	X	X	↑	Hold	
1	0	0	1	X	↑	Increment	
1	0	0	0	X	↑	Decrement	

Assigning Test Vectors

The default input radix for all test vectors is decimal. To specify a binary, hex, or octal radix, add a 0b, 0h, or 0o prefix, respectively, to the vector (e.g., 0b1010 or 0h7e). Outputs are in binary format. To interactively define input test vectors, use the Debugger menu. Alternatively, use input command files to define test vectors. To view outputs and internal nodes, print them to the PC screen display or to an output file.

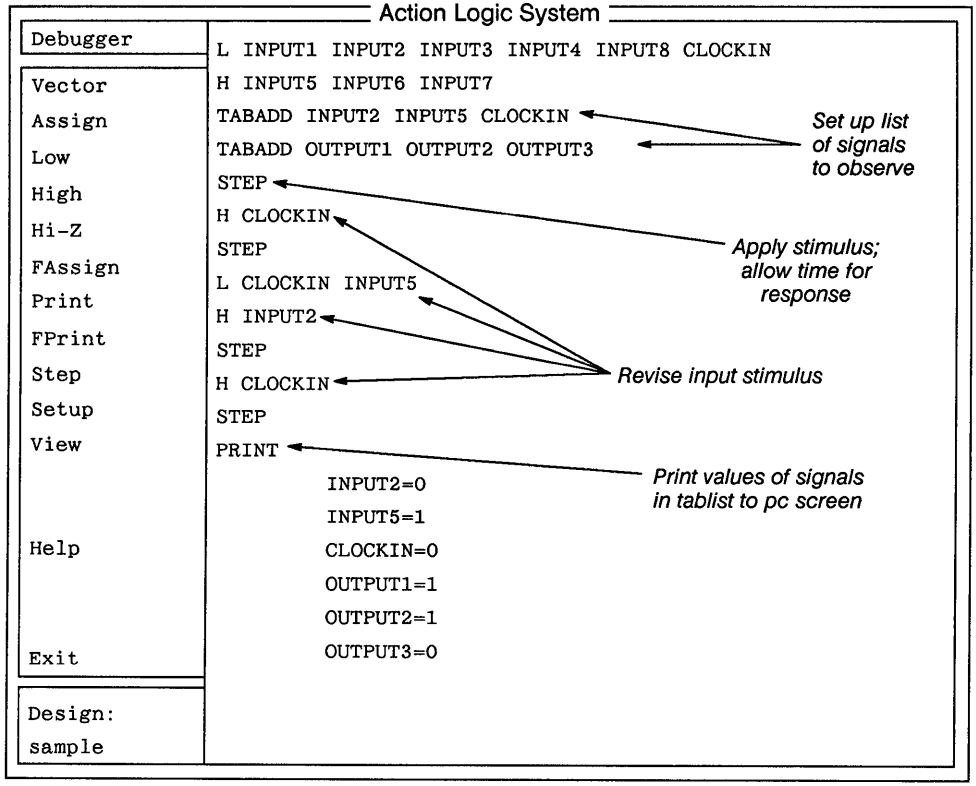


Figure 2. Typical Debug Command Sequence

Defining User Macros

You may save time by creating user-defined macros for the Debugger. These macros may contain a series of basic Debug commands or may nest any combination of basic commands and user-defined macros.

The sample macro in part A of Figure 3, `clk10`, provides 10 clock pulses to the pin CLK and prints the value of internal vector Q to a specified output file after each clock pulse. The `outfile` command specifies the output file.

Part B of Figure 3 shows a nested macro, `clk100`, that executes the `clk10` macro 10 times, providing 100 clocks to the CLK pin.

A

```
define (clk10) (repeat 10 (1 CLK) (step) (h CLK) (step) (fprint Q))
```

B

```
define (clk100) (repeat 10 (clk10))
```

Figure 3. Sample Command Macros

Creating a Command File (`TT269.cmd`)

The command file (see Figure 4) applies test vectors to the `TT269` counter. It redirects results to an output file, `TT269.out`, and compares the output vector Q of the counter to an existing results file, `TT269.cmp`. The following notes correspond to each line in the command file.

Lines 1 and 2: The `vector` command defines eight parallel load input bits as vector P and counter output as vector Q.

Line 3: The `tabadd` command defines the internal or external nodes to be displayed or printed when the `print` or `fprint` command is executed.

Lines 4, 5, and 6: The `infile`, `outfile`, and `compfile` commands define input and output files. The `infile` command opens a file containing input test vectors. The `outfile` command contains the output results. The `compfile` command contains the data to be compared against the current device status. Use the full path name of the file, and enclose it in question marks.

Line 7: The `define` commands create user-defined macros. In this example, the `clk10` macro provides 10 clock pulses to the CLK input, `fprint` prints all nodes in the `tabadd` command to a file defined by `outfile`, and `fcomp` compares the status of vector Q to the file specified by `compfile`.

Lines 8, 9, and 10: Defines three user macros: up, down, and load.

Loading a Command File

The `loadfile` command loads a defined command file into the Debugger. Select `setup | loadfile` from the Debugger menu, then enter the full path name of the command file. For example:

```
/designs/TT269/TT269.cmd
```

Executing User-Defined Macros

To execute any previously defined macro, type the macro at the command line while in the Debugger.

```
Line
  1       (vector P P0 P1 P2 P3 P4 P5 P6 P7)
  2       (vector Q Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7)
  3       (tabadd PE CEP CET UD P CLK Q TC)
  4       (infile "/designs/tt269/tt269.pat")
  5       (outfile "/designs/tt269/tt269.out")
  6       (compfile "/designs/tt269/tt269.cmp")
  7       (define (clk10) (repeat 10 (l CLK)(step)(h CLK)(step)(fprint)(fcomp Q)))
  8       (define (up) (l CEP CET)(h PE UD)(step)(clk10))
  9       (define (down) (h PE)(l CEP CET UD)(step)(clk10))
 10       (define (load) (l PE CLK)(step)(fassign P)(h CLK)(step))
```

Figure 4. Debug Command File (`TT269.cmd`)

Running the Sample Command File

In the following example, we will assign input test vectors from an input pattern file named `TT269.pat` and will write output results to a file named `TT269.out`. The command file (`TT269.cmd`) compares the counter's output vector Q to an existing results file (`TT269.cmp`.)

Input Pattern File (`TT269.pat`)

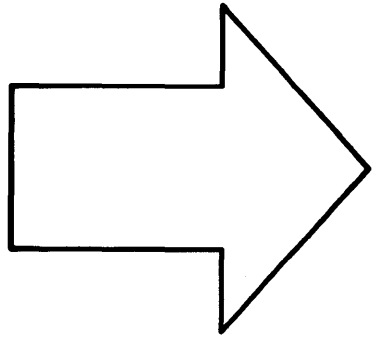
```
0b00000000
0b10000000
0b01000000
0b11000000
```

Output Results File (`TT269.out`)

```
  S    P C C U         P C         Q T
  T    E E E D           L           C
  E      P T             K
  P
00005: 1 0 0 1 00000000 1 10000000 0
00007: 1 0 0 1 00000000 1 01000000 0
00009: 1 0 0 1 00000000 1 11000000 0
00011: 1 0 0 1 00000000 1 00100000 0
00013: 1 0 0 1 00000000 1 10100000 0
00015: 1 0 0 1 00000000 1 01100000 0
00017: 1 0 0 1 00000000 1 11100000 0
00019: 1 0 0 1 00000000 1 00010000 0
00021: 1 0 0 1 00000000 1 10010000 0
00023: 1 0 0 1 00000000 1 01010000 0
00028: 1 0 0 0 10000000 1 00000000 1
00030: 1 0 0 0 10000000 1 11111111 0
00032: 1 0 0 0 10000000 1 01111111 0
00034: 1 0 0 0 10000000 1 10111111 0
00036: 1 0 0 0 10000000 1 00111111 0
00038: 1 0 0 0 10000000 1 11011111 0
00040: 1 0 0 0 10000000 1 01011111 0
00042: 1 0 0 0 10000000 1 10011111 0
00044: 1 0 0 0 10000000 1 00011111 0
00046: 1 0 0 0 10000000 1 11101111 0
00051: 1 0 0 1 01000000 1 11000000 0
00053: 1 0 0 1 01000000 1 00100000 0
00055: 1 0 0 1 01000000 1 10100000 0
00057: 1 0 0 1 01000000 1 01100000 0
00059: 1 0 0 1 01000000 1 11100000 0
00061: 1 0 0 1 01000000 1 00010000 0
00063: 1 0 0 1 01000000 1 10010000 0
00065: 1 0 0 1 01000000 1 01010000 0
00067: 1 0 0 1 01000000 1 11010000 0
00069: 1 0 0 1 01000000 1 00110000 0
00074: 1 0 0 0 11000000 1 01000000 0
00076: 1 0 0 0 11000000 1 10000000 0
00078: 1 0 0 0 11000000 1 00000000 1
00080: 1 0 0 0 11000000 1 11111111 0
00082: 1 0 0 0 11000000 1 01111111 0
00084: 1 0 0 0 11000000 1 10111111 0
00086: 1 0 0 0 11000000 1 00111111 0
00088: 1 0 0 0 11000000 1 11011111 0
00090: 1 0 0 0 11000000 1 01011111 0
00092: 1 0 0 0 11000000 1 10011111 0
```

Output Compare File (`TT269.cmp`)

```
0b10000000
0b01000000
0b11000000
0b00100000
0b10100000
0b01100000
0b11100000
0b00010000
0b10010000
0b01010000
0b00000000
0b11111111
0b01111111
0b10111111
0b00111111
0b11011111
0b01011111
0b10011111
0b00011111
0b11101111
0b11000000
0b00100000
0b10100000
0b01100000
0b11100000
0b00010000
0b10010000
0b01010000
0b11010000
0b00110000
0b01000000
0b10000000
0b00000000
0b11111111
0b01111111
0b10111111
0b00111111
0b11011111
0b01011111
0b10011111
```



ACT™ Family Reliability Report

By Steve Chiang and Ken Hayes

A1010/A1020 are 1200- and 2000-gate (respectively) field programmable gate arrays (FPGAs). The programming element is an Actel-invented PLICE™ (Programmable Low-Impedance Circuit Element) antifuse. An antifuse is a normally open device in which an electrical connection is established by the application of a programming voltage. Although the A1010/A1020 are one-time programmable devices, their unique architecture includes complete functional testability.

Actel currently manufactures two versions of each product. The A1010/A1020 device is processed using 2 µm design rules while the A1010A/A1020A is a 20% linear shrink which uses 1.2 µm design rules. Both the full sized and shrink products are manufactured using the same wafer fab lines and process flows. The technology used is a standard double metal, twin well, CMOS process in which three additional masking steps have been added to implement the PLICE antifuse. A description of the main process parameters is shown in Table 1. Because the A1010/A1020 are manufactured with a conventional CMOS process, normal CMOS failure modes will be observed. However, the addition of the antifuse adds another structure which could affect the device's reliability.

Actel has completed numerous studies in order to quantify the reliability of the antifuse. These studies lead to the conclusion that the time to failure of the antifuse is substantially more than 40 years under normal operating conditions and that the combined contribution of all antifuses to the gate array product's hard failure rate is less than 10 FITs (Failures-in-Time or 0.001% failures per 1000 hours).

The PLICE Antifuse

The antifuse is a vertical, two-terminal structure. It consists of a polysilicon layer on top, N+ doped silicon on the bottom, and an ONO (oxide-nitride-oxide) dielectric layer in between. A Scanning Electron Microscope (SEM) cross-section of the antifuse is shown in Figure 1. On the A1010/A1020 the size of the antifuse is 3.2 μm^2 while it is 1.4 μm^2 on the A1010A/A1020A. This small size, along with a low programmed on-resistance, typically 500 Ohms, makes the PLICE antifuse a very attractive alternative to EPROM, EEPROM, or RAM for use as a programming element in a large programmable gate array. In the unprogrammed state, the resistance of the antifuse is in excess of 100 MOhms. The A1010 and A1020 contain 112,000 and 186,000 antifuses respectively. However, typical applications utilizing 85% of the available gates require programming only 2% to 3% of the available antifuses.

Table 1. A1010/A1020 Process Description

Process Type: CMOS, double metal, dual polysilicon, dual well, EPI wafer

Dimensions	2.0 µm Process		1.2 µm Process	
	Width (µm)	Space (µm)	Width (µm)	Space (µm)
N+	4.0	2.0	3.2	1.6
P+	4.0	2.0	3.2	1.6
Cell Poly-Si	2.0	3.6	2.1	2.4
Gate Poly-Si	1.6	2.4	1.6	1.6
Metal I	4.0	2.0	3.2	1.6
Metal II	4.8	2.2	3.8	1.8
Contact	1.8 x 1.8	2.0	1.2 x 1.2	1.8
Via	2.0 x 2.0	2.0	1.3 x 1.3	1.9
Thickness	**2.0 µm Process**		**1.2 µm Process**	
Normal Gate Oxide	25 nm		25 nm	
High Voltage Gate Oxide	40 nm		40 nm	
Cell Poly-Si	450 nm		450 nm	
Gate Poly-Si	450 nm		450 nm	
Metal I	900 nm		900 nm	
Metal II	1000 nm		1000 nm	
Passivation	1100 nm		1100 nm	
Compositions				
Metal I	Al - Si (1%) - Cu (0.5%)		Al - Si (1%) - Cu (0.5%)	
Metal II	Al - Si (1%) - Cu (0.5%)		Al - Si (1%) - Cu (0.5%)	
Passivation	3000 nm SiO_2, 800 nm SiN		3000 nm SiO_2, 800 nm SiN	

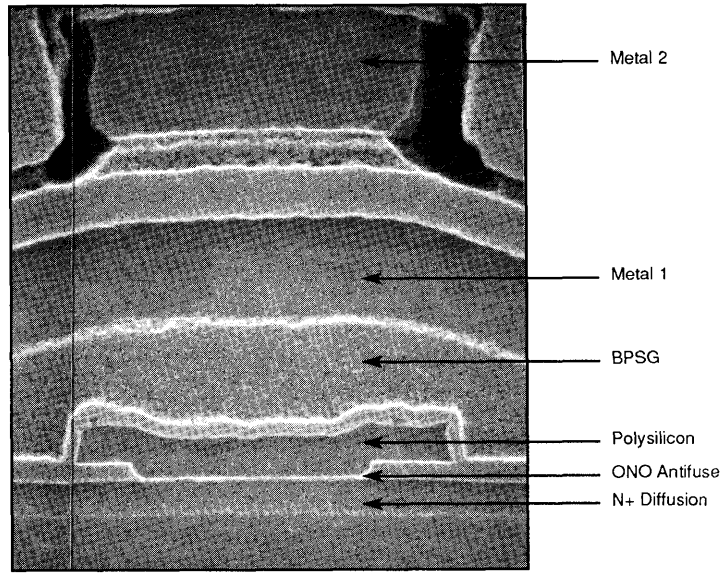


Figure 1. Antifuse SEM Cross-Section

The Unprogrammed Antifuse

In order to evaluate antifuse reliability, Actel has developed models and collected data for both unprogrammed and programmed antifuses[1,2]. We'll consider the unprogrammed antifuse first. Since the antifuse is a dielectric sandwiched between polysilicon and silicon, the model for its reliability, in the unprogrammed condition, is the same as that used to evaluate reliability of MOS transistor gate oxides[3]. The parameter we wish to evaluate is the time to breakdown (t_{bd}) of the dielectric. This parameter is a function of the electric field across the dielectric as well as temperature and has the following relationship[3].

$$t_{bd} = t_0 * \exp(G/E) \quad (1)$$

where t_{bd} is the time to breakdown in seconds, t_0 is a constant in seconds, E is the electric field in Mv/cm, and G is the field acceleration factor in Mv/cm (G is temperature dependent and will be discussed later).

By taking the log of both sides of equation 1 we have:

$$\ln(t_{bd}) = G * (1/E) + \ln(t_0) \quad (2)$$

From experimental data, we can plot the log of the time to breakdown of the antifuse at various temperatures versus the reciprocal of the electric field across it and derive G from the slope and t_0 from the Y intercept. Actel has done this on single antifuses, large antifuse capacitors, test arrays of 28,000 antifuses, and actual A1010/A1020 products. These antifuse areas range from 3.2 μm^2 to 0.35 mm^2. Figure 2 shows plots of data collected on these different sized antifuses.

There is some discussion in the literature regarding whether time to breakdown depends on E or 1/E. To verify the validity of equation 2, we conducted the following experiment. Large 200 μm by 200 μm (0.04 mm^2) area capacitors were packaged and then stressed at more than eleven different voltages. Capacitors were chosen from two different wafer runs with thicknesses ranging from a low of 8.0 nm to a high of 9.5 nm. A total of 642 capacitors were used in the experiment. The test splits and sample sizes are summarized in Table 2. The distribution of time to breakdown of the dielectric at each voltage is shown in Figure 3. In Figure 4, we plot the median of the cumulative failure percentage rates (t_{50}) from Figure 3 versus 1/E. In Figure 5 the median failure percentage is plotted versus E. By comparing the two figures, the validity of the 1/E model is clearly established. A more detailed statistical verification of the 1/E model for the ONO antifuse is given in Reference 2.

Table 2. Field Accelerated Test Data for Two Lots with Thickness Ranging from 8 nm to 9.5 nm.
(The test was done on 0.04 mm^2 area capacitor.)

Lot A					Lot B				
Voltage (V)	Tox (nm)	E-Field (MV/cm)	# of Capacitors	t_{50} (sec)	Voltage (V)	Tox (nm)	E-Field (MV/cm)	# of Capacitors	t_{50} (sec)
13.5	8.3	16.2	22	4.2 e-3	14.0	8.7	15.9	25	9.8 e-3
12.5	8.3	15.1	22	3.7 e-2	13.0	8.7	14.9	25	5.0 e-2
12.0	8.3	14.4	22	1.5 e-1	12.5	8.7	14.3	25	2.4 e-1
11.5	8.3	13.8	22	8.6 e-1	12.0	8.7	13.7	25	1.3 e0
11.0	8.4	13.1	22	4.7 e0	11.4	8.7	13.1	25	9.0 e0
10.5	8.4	12.5	9	5.8 e1	11.2	8.7	12.5	45	8.0 e1
10.0	8.3	12.0	6	3.2 e2	10.8	9.0	12.0	45	3.52 e2
9.5	8.3	11.4	6	2.5 e3	10.2	9.0	11.3	45	2.88 e3
9.0	8.3	10.7	36	2.5 e4	9.7	9.0	10.8	45	2.07 e4
8.5	8.3	10.2	15	2.3 e5	9.0	8.7	10.3	32	3.35 e5
8.0	8.3	9.6	59	1.5 e6	9.0	9.3	9.7	32	2.22 e6
Subtotal of tested capacitors:			241					401	
Total of tested capacitors:			642						

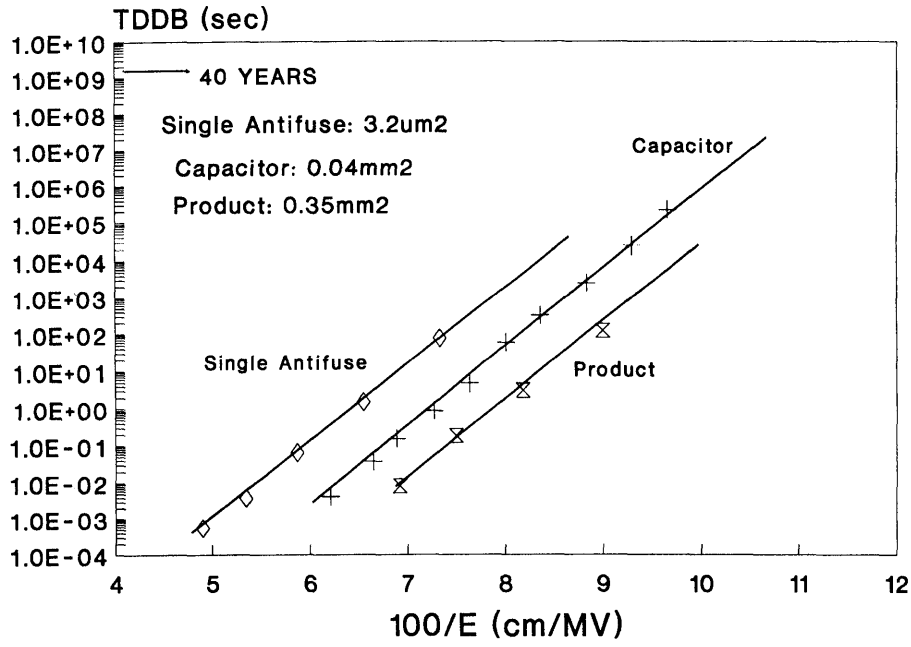


Figure 2. Field Accelerated Test

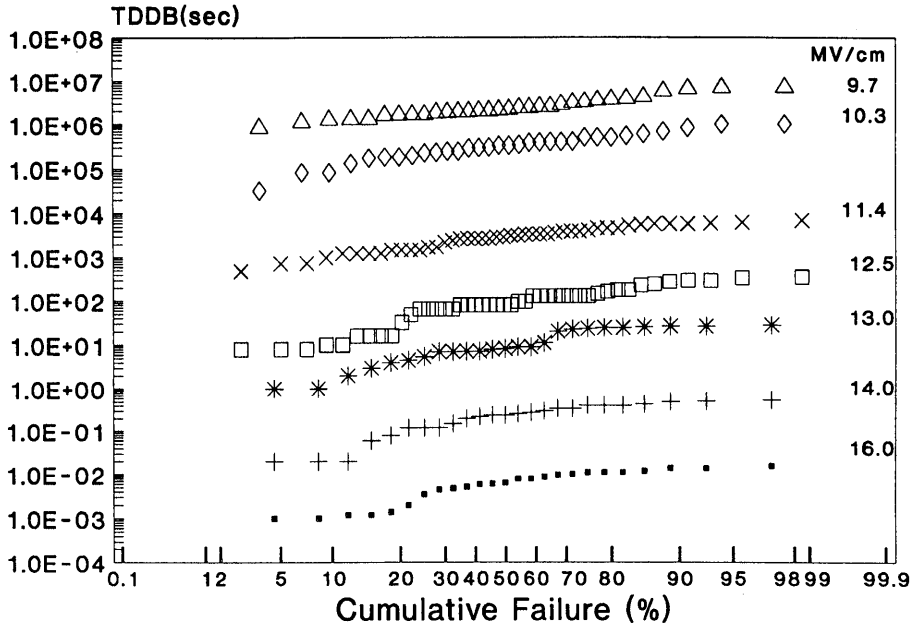


Figure 3. TDDB Distribution

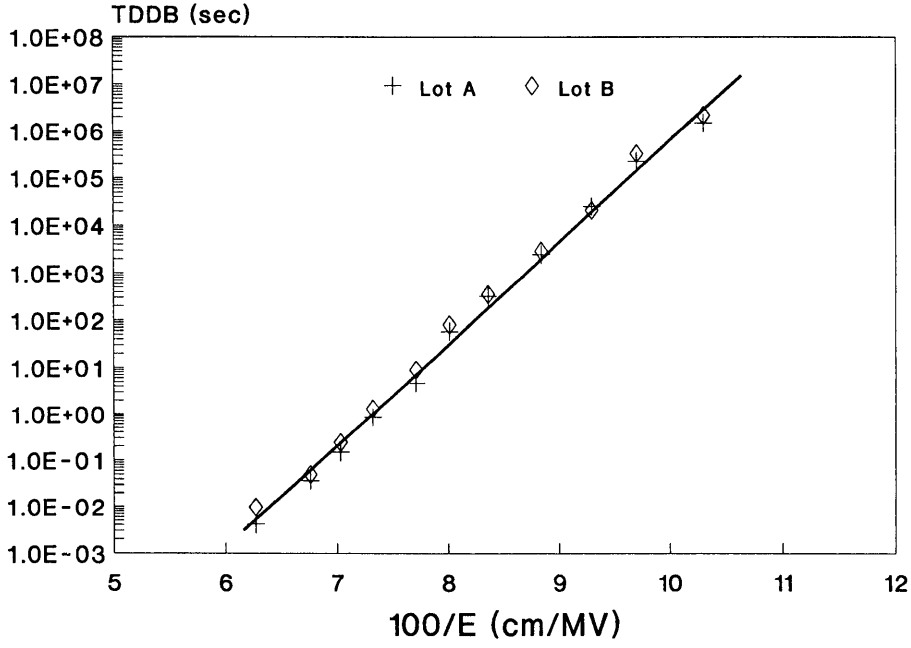


Figure 4. ONO Reliability (1/E Model)

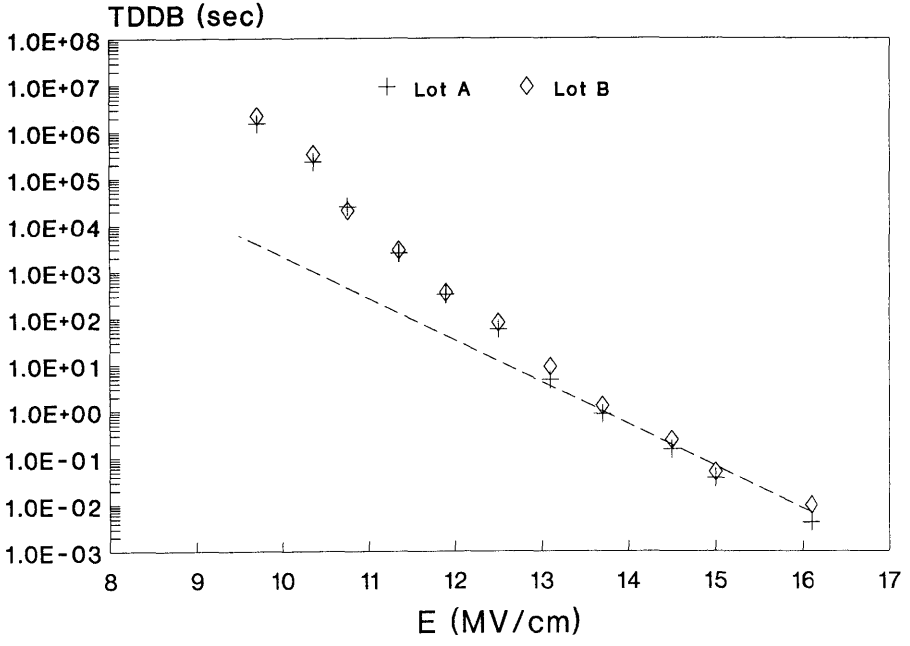


Figure 5. ONO Reliability (E Model)

In order to quantify the temperature dependence of the time to breakdown, we use the Arrhenius equation to determine the semiconductor failure rate of a given process (failure mode) over temperature:

$$R = R_0 * \exp(E_a/kT) \quad (3)$$

where R is the failure rate, R_0 is a constant for a particular process, T is the absolute temperature in degrees Kelvin, k is Boltzmann's constant (8.62×10^{-5} eV/°K) and E_a is the activation energy for the process in electron volts. To determine the acceleration factor for a given failure mode at temperature T_2 as compared with temperature T_1 we use equation 3 to derive:

$$A(T_1, T_2) = \exp[(E_a/k) * \{(1/T_1) - (1/T_2)\}] \quad (4)$$

where A is the acceleration factor.

In Figure 6 we plot t_{50} at different temperatures and electric fields. This plot shows that time to breakdown is dependent on temperature as well as electric field. For a given time to breakdown of a dielectric, the expression,

$$E_a = k * d\ln(t_{bd})/d(1/T) \quad (5)$$

gives us the activation energy[2]. The slope in Figure 6 represents the activation energy E_a. E_a also shows a linear correlation with 1/E as shown in Figure 7. The field acceleration factor, G, is also temperature dependent, i.e.

$$G(T) = G(298) * [1 + \delta/k * \{1/T - 1/298\}] \quad (6)$$

where G(298) is the field acceleration factor at room temperature (25°C = 298°K) and δ (in eV) characterizes the temperature dependence of G.

By combining equations 1, 5, and 6, E_a can be related to G(T) by:

$$E_a = G(298) * \delta/E - E_b \quad (7)$$

where δ and E_b are treated as fitting parameters between E_a and G.

From the data shown in Figures 3, 4, 6, and 7 we can obtain values of G(298), δ, E_b, and E_a regardless of antifuse area. Typical values of G(298), δ, E_b, and E_a at 5.5V are 480 MV/cm, 0.014 eV, 0.43 eV, and 1×10^{-16}. By combining equations 1, 6, and 7, we obtain an overall equation for the time to breakdown for a given temperature and E field:

$$t_{bd} = t_0 * \exp\{(G(298)/E)[1+(\delta/k) * (1/T-1/298)] - (E_b/k) * (1/T-1/298)\} \quad (8)$$

By applying the values for the constants as defined above, the time to breakdown for the antifuse dielectric can be derived for a given temperature and electric field. In Table 3, we have used equation 8 to solve for the acceleration factors associated with powering up a device at high voltage and/or temperature and comparing the failure rate with more typical voltages or temperatures. We can see the effect of temperature by comparing 125°C at 5.5 V with 55°C at 5.5 V in which the Actel model (equation 8) gives us an acceleration factor of 55.3, or 6.3 equivalent years for a 1000 hour

burn-in at 125 °C. Note that this acceleration factor of 55.3 is close to the value of 41.8 derived from the Arrhenius equation (equation 4) using an activation energy of 0.6 eV and the same temperatures. We use 0.6 eV (and 0.9 eV) as a general semiconductor failure mode activation energy when calculating failure rates from high temperature operating life (HTOL) later in this report.

We can also see from Table 3 that a small change in voltage is a much more effective reliability screen than is a change in temperature. For example, if we compare 25 °C at 5.75 V to 25 °C at 5.25 V we see that just a half volt change yields an acceleration factor of 1092.6, or 124.7 equivalent years per 1000 hours at 5.75 V. This strong dependence on voltage allows Actel to screen out antifuse infant mortality failures during normal wafer sort testing simply by performing a special test in which a higher than normal voltage is applied across all antifuses. Because antifuse infant mortality failures can be detected and effectively screened, A1010/A1020 devices have as high a level of reliability as standard CMOS processed products.

In order to establish that the antifuse contributes less than 10 FITs (at 5.5 V, 125°C) to the overall product reliability, Actel has calculated the product failure rates due to the antifuse using three different techniques. In the first case, we evaluated the t_{bd} distribution of 125 A1010 units in which the antifuses received an 11 V stress. Using E_a = 0.9 eV and extrapolating to 5.5 V, we find that the 1% antifuse failure lifetime at 5.5 V is well over 40 years and less than 10 FITs.

The second method of determining product reliability was to look at production wafer sort results. As was mentioned earlier, all antifuses receive a high voltage stress at wafer sort to screen out infant mortality failures. Specifically, all antifuses receive the equivalent of two, 10 V stresses for one second each. The first stress is to screen out clearly defective antifuses. The second stress is to catch weaker antifuses which could cause product programming yield problems or infant mortality failures. Actual failure rates observed on the A1010 over ten runs for these two stresses (FS-1 and FS-2) demonstrate average yield loss at the second stress screen of less than 0.3%. By extrapolating this yield loss to a normal 5.5 V operating voltage, we thus conclude that the contribution of the antifuse to the overall product's lifetime is less than 10 FITs.

The third technique of determining the product's antifuse failure rate is by doing an accelerated burn-in of A1010/A1020 products. The acceleration is accomplished by using both higher voltage (5.75 V to 6.0 V) and high temperature (125 °C to 150 °C). Units are programmed to a specific design and exercised in a manner similar to what may occur in a real application. For a detailed description of the test and the results, see the High Temperature Operating Life section later in this report. Here, too, the conclusion is that the antifuse contributes less than 10 FITs to the product's overall failure rate and it is thus an insignificant factor in product lifetime of 40 years at 5.5 V and 125 °C.

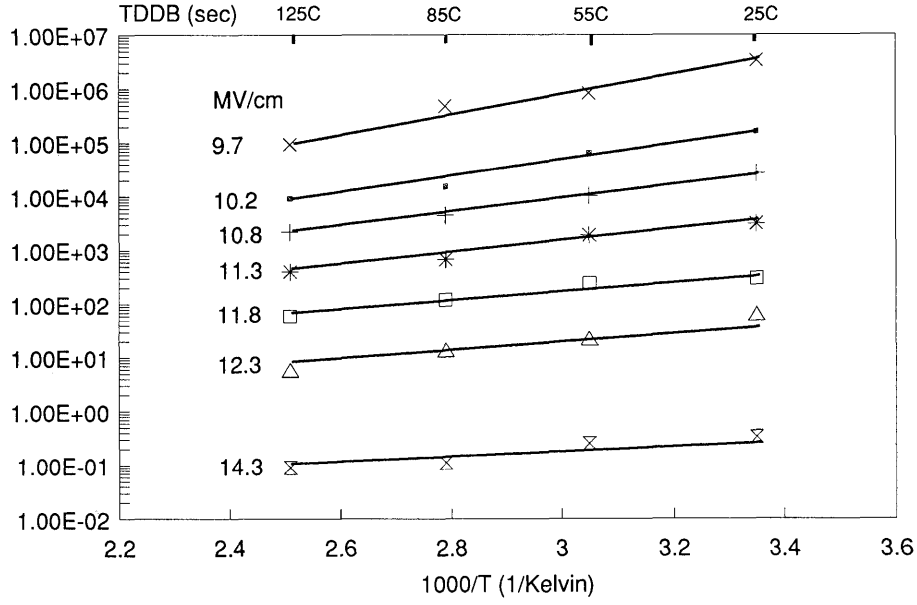


Figure 6. Dependence of E-Field Acceleration on Temperature

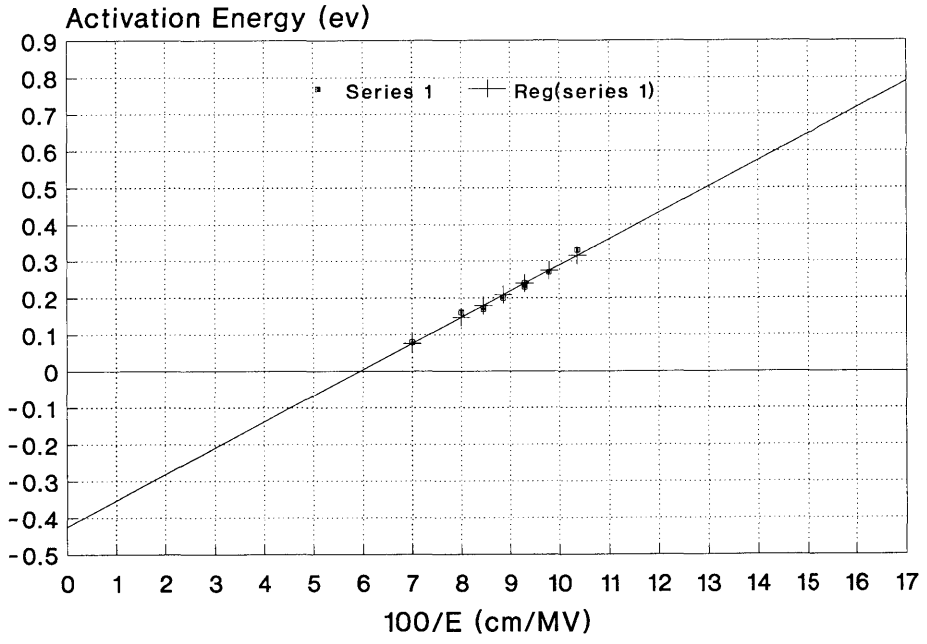


Figure 7. Activation Energy versus 1/E

Table 3. Acceleration Factor vs. Operating Conditions (Unprogrammed Antifuse)

$t_0 = 1 \times 10^{-16}$ sec., G = 480 MV/cm, δ = 0.014 eV, E_b = 0.43 eV.

Model	Temperature/Voltage		Acceleration Factor	Equivalent Years for 1000 Hour 125°C Burn-In
	High	Typical		
Fixed Voltage	125°C / 5.5 V	55°C / 5.5 V	55.3	6.3
	125°C / 5.5 V	90°C / 5.5 V	6.1	0.7
Fixed Temperature	25°C / 5.5 V	25°C / 5.25 V	38.8	4.4
	25°C / 5.75 V	25°C / 5.25 V	1092.6	124.7
	25°C / 5.75 V	25°C / 5.5 V	28.2	3.2
	25°C / 6.0 V	25°C / 5.25 V	23321	2662
	25°C / 6.0 V	25°C / 5.5 V	601.8	68.7
Varied Temperature and Voltage	125°C / 5.5 V	55°C / 5.25 V	1787.2	204.0
	125°C / 5.75 V	55°C / 5.5 V	987.8	112.8
	125°C / 5.75 V	90°C / 5.5 V	109.4	12.5
	125°C / 6.0 V	55°C / 5.5 V	13865	1583
	125°C / 6.0 V	90°C / 5.5 V	1535.9	175.3
Fixed 0.6 eV Activation Energy Voltage - Independent	150°C / 5.5 V	55°C / 5.5 V	117.6	13.4
	150°C / 5.5 V	90°C / 5.5 V	15.2	1.7
	125°C / 5.5 V	55°C / 5.5 V	41.8	4.8
	125°C / 5.5 V	90°C / 5.5 V	5.4	0.6

The Programmed Antifuse

A Kelvin test structure as shown in Figure 8 was used to evaluate reliability of a programmed antifuse. Here, a strip of polysilicon crosses an N+ diffusion. The antifuse is located at their intersection. There are metal-to-poly contacts at nodes 1 and 3 as well as metal-to-N+ contacts at nodes 2 and 4. A four terminal Kelvin structure is useful should a failure occur, because antifuse opens can be separated from other problems (such as polysilicon or contact opens) simply by checking for continuity on appropriate pairs of nodes.

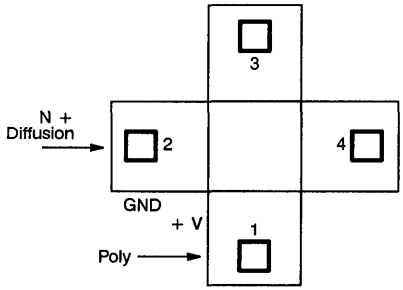


Figure 8. Antifuse Kelvin Structure

Test devices were stressed by forcing a constant 5 mA current from polysilicon to N+ through the antifuse at 250°C. Note that this stress is far greater than a programmed antifuse would see in a device under normal operating conditions. Because the antifuse is used to connect two networks together, there is usually no voltage across it and hence no current passes through. A voltage will appear across the antifuse only momentarily while a network switches from low-to-high or high-to-low.

During the 5 mA, 250°C stress, the voltage across the antifuse was monitored. Figure 9 is a plot of the monitored voltage as a function of stress time. A sudden increase in voltage indicates that an open occurred. As can be seen from the figure, failures occurred at about 300 hours of stress. However, by probing on nodes 3 and 4 of the Kelvin structure, we were able to measure continuity and determine that the cause of failure was not the antifuse. The failed units were then examined on an SEM, where the cause of failure was revealed as metal-to-poly contact electromigration. This is a well-known failure mode in CMOS, which has been determined to have an activation energy of 0.9 eV. Using equation 4 we can predict a lifetime under normal operating conditions in excess of 40 years for this failure mode. The lifetime of the programmed antifuse is even longer.

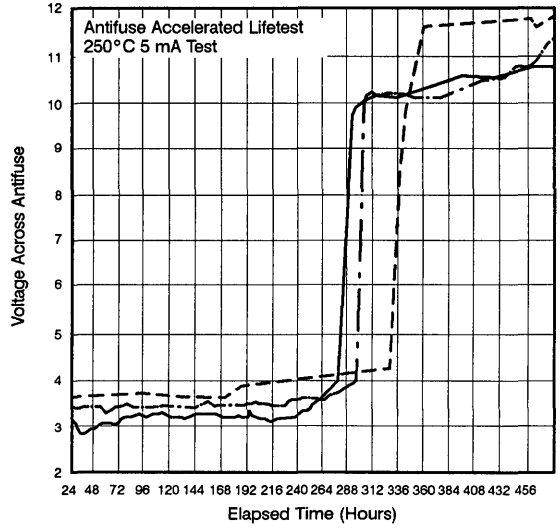


Figure 9. Voltage Across Antifuse versus Stress Time

A1010/A1020/A1280 Product Reliability

Product Reliability was evaluated on five Actel products; a 64K PROM (PROM64), a 300-gate FPGA (1003), a 1200-gate FPGA (A1010/A1010A), a 2000-gate FPGA (A1020/A1020A), and an 8000-gate FPGA (A1280). The PROM64 product uses the same process and antifuse as the A1010/A1020. The 1003 is a test device which is a smaller version of the A1010/A1020, and was used for early characterization and qualification. As mentioned earlier, the A1010A and A1020A are 20% linear die shrink versions of the A1010 and A1020, respectively. The PROM64 units were packaged in 24 pin side-brazed packages while the FPGA units were in 68 and 84 pin JLCC (ceramic J-leaded chip carriers), JQCC (ceramic leaded chip carriers), and PLCC (plastic leaded chip carriers) packages. Package characteristics for the A1010/A1020 are shown in Table 4.

High Temperature Operating Life (HTOL)

The intent of HTOL is to dynamically operate a device at high temperature (usually 125°C or 150°C) and extrapolate the failure rate to typical operating conditions. This test is defined by Military Standard-883 in the Group C Quality Conformance Tests. The Arrhenius relationship in equations 3 and 4 is used to do the extrapolation. To use the Arrhenius equation, we need to know the activation energy of the failure mode. Activation energies of antifuse failure modes were discussed earlier. Table 5 gives the Activation energies of general semiconductor failure modes.

Table 4. A1010/A1020 Packaging Description

PLCC	
Molding Compound	Sumitomo 6300H
Filler Material	Fused silicon 70% by weight
Lead Frame Material	Copper
Lead Plating Composition	Solder, 300-800 micro inches (μin)
Die Attach Material	Silver Epoxy
Flame Retardance	UL-94, V-0
Bond Wire	Gold, 1.3 mil diameter
Bond Attach Method	Thermosonic

JQCC	
Body Material	Ceramic
Lid Material	Ceramic
Sealant	Glass
Lead Frame Material	Alloy 42 (40% Nickel, 60% Iron)
Bond Wire	99% Aluminum, 1% Si, 1.25 mil diameter
Bond Attach Method	Ultrasonic
Lead Finish	Solder dip, 200 μin. min.

Thermal Resistances (°C/Watt)

Package	44 PLCC	44 JQCC	68 PLCC	68 JQCC	84 PLCC	84 JQCC	84 PGA	84 CQFP	100 PQFP
θ_{JC}	15	8	13	8	12	8	8	8	20
θ_{JA}	52	38	45	35	44	34	35	38	65

Six different data patterns were programmed into the 64K PROMs for HTOL testing: a diagonal of zeros (98% programmed); a diagonal of ones (2% programmed); a topological checkerboard pattern (50%); all zeros (100%); all ones (0%); and an incrementing pattern (50%). During burn-in, all addresses are sequenced through at a 1 MHz clock rate. The outputs are enabled and loaded with a 100 ohm resistor to a 2 V supply. This results in an output loading of equal to or greater than the specified limits of Ioh = -4 mA and Iol = 16 mA. In most cases, the PROMs were burned-in at Vcc = 5.5 V and at 125°C. However, voltage acceleration experiments were also done at 7 V, 125°C as well as 8 V, 25°C.

The PROM is useful for antifuse reliability studies for several reasons. First of all, we can program anywhere from 0% to 100% of the antifuses although we program only 2-3% of the antifuses for a given design on the A1010/A1020 device. Also, an antifuse failure on the PROM is very noticeable, since the antifuse is directly addressed. A weak fuse would show an AC speed drift, and a failed antifuse would read the wrong data.

For evaluating the 1003/A1010/A1020/A1280, we programmed an actual design application into most devices (some units were burned-in unprogrammed) and performed a dynamic burn-in by toggling the clock pins at a 1 MHz rate. The designs selected utilized 85-97% of the available logic modules and 85-94% of the I/Os. Outputs were loaded with 1.2 K ohm resistors to Vcc which results in greater than 4 mA of sink current as each I/O toggled low. Under these conditions, each A1010 typically draws about 100 mA during dynamic burn-in. Most of this current comes from the output loading while about 5 mA is from the device supply current. The thermal resistance (junction to ambient) of the 68 and 84 pin PLCC packages is about 45°C/Watt and for the JLCC packages it is about 35°C/Watt. For a 125°C burn-in, this results in junction temperatures of about 150°C for plastic packages and 145°C for ceramic packages. Most burn-in was done at 5.75 V or 6.0 V (for voltage acceleration of the antifuse) and 125°C or 150°C.

Table 5. CMOS Failure Mechanisms

Failure Mechanism	Activation Energy
Ionic Contamination	1.0 eV
Oxide Defects	0.3 eV
Hot Carrier Trapping in Oxide (Short Channels)	-0.06 eV
Silicon Defects	0.5 eV
Aluminum-Silicon-Copper Electromigration	0.6 eV
Contact Electromigration	0.9 eV
Electrolytic Corrosion	0.54 eV

Some initial burn-in evaluation was also done on the first member of the new ACT 2 family — the A1280. This is an 8000-gate product which is manufactured using the same processing technology as used for the A1010A/A1020A (1.2 µm).

As was mentioned earlier, some units are burned-in unprogrammed. To accomplish this, we use a special burn-in circuit which allows us to use the product's test features in order to serially shift in commands to the chip during burn-in. All internal routing tracks are toggled between Vss and Vcc. When vertical tracks are at Vcc, horizontal tracks are held at Vss and vise versa. Thus all antifuses which can connect vertical and horizontal tracks receive a full Vcc stress in both directions. Since vertical tracks connect to logic module inputs and outputs, these too are toggled between Vss and Vcc. Finally, a command is sent to the chip to toggle some external I/O pins between Vss and Vcc. This special dynamic burn-in circuit is the same that is used by Actel to screen unprogrammed product to MIL-883C requirements. Since virtually all antifuses receive a full Vcc stress, this screen is much more effective at catching unprogrammed antifuse infant mortality failures than is burning-in programmed devices where only a fraction of the antifuses are stressed.

A summary of the HTOL data collected by Actel is shown in Table 6. A failure is defined as any device which shows a functional failure, exceeds datasheet DC limits, or exhibits any AC speed drift. Among the parts tested, no speed drift, faster or slower, was observed within the accuracy of the test set-up. Failure rates at 55°C, 70°C, and 90°C were extrapolated by using the Arrhenius equation and general activation energies of 0.6 eV and 0.9 eV. Poisson statistics were used to derive a calculated failure rate with a 60% confidence level. Use of Poisson statistics is valid for a failure rate which is low and a failure mode which occurs randomly with time. At 55°C, the calculated failure rate with a 60% confidence level was found to be 36 FITs or 0.0036% failures per 1000 hours. This number was derived from over 4.8 million device hours (125°C) of data. There were six total failures. Only one occurred in the first 80 hours of burn-in (1003 product). The others failed at 300, 417, 500 (x2), and 650 hours. Five of the six failures observed were due to common CMOS failure mechanisms (gate oxide failure, silicon defects, open via). Only one unit failed due to an antifuse failure. This unit was burned-in in the unprogrammed state to stress all antifuses. It was stressed at 6 V, 150°C. It passed at 168 hours and failed at 650 hours due to an antifuse becoming programmed. By passing at 168 hours, the unit received a total stress well in excess of 100 years of operation at 5.5 V, 125°C (using equation 8). With only one antifuse related failure in 4,830,000 device hours at 125°C, we use equation 8 to derive that this one antifuse failure at 6 V is less than 10 FITs at 5.5 V.

Unbiased Steam Pressure Pot

This test is used to qualify products in plastic packages. Units are placed in an autoclave (pressure pot) and exposed to a saturated steam atmosphere at 121°C and 15 psi. Problems with bonding, molding compounds, or wafer passivation can cause metal corrosion to occur in this atmosphere. The existence of metal corrosion is detected during a full electrical test of the device following exposure to the autoclave environment.

A total of 773 units from 17 wafer runs were evaluated. Read points were taken at 96, 168, 240, and 336 hours. There were a total of five failures (Table 7). All five failures were found to be due to bond wires lifting off bond pads. These were due to assembly problems which occurred only on our first lots of plastic units built. The failures were caused by temperature and not by metal corrosion. The assembly problems have been corrected, with no further failures observed.

Biased Moisture Life Test (85/85)

In this test, the units are placed in a chamber at a temperature of 85°C and a relative humidity of 85%. A voltage of 5.5 V is applied to every other device pin while other pins are grounded. 5.5 V is applied to Vcc while Vss is grounded. This test is effective at detecting die related and plastic package related problems.

As shown in Table 8, a total of 481 units have been stressed. There have been three failures. Two failures were due to lifted bond wires and came from the same lot in which we saw failures in steam pressure pot. The 1000 hour failure is nonfunctional due to an open Metal 1 line.

Temperature Cycling

This test checks for package integrity by cycling units through temperature extremes. Data was taken for cycles of 0°C to 125°C, -40°C to 125°C, and -65°C to 150°C. Both programmed and unprogrammed units are placed on temperature cycle. As shown in Table 9, of 1466 units tested to date, there have been no failures.

Table 6. High Temperature Operating Life HTOL Test Summary

Product	Units	Wafer Runs	Device Hours At 125°C	Failures	Eqiv Dev Hrs (in millions) At 55°C (0.6 eV)	Eqiv Dev Hrs (in millions) At 70°C (0.6 eV)
PROM64	295	4	618,000	0	25.9	10.2
1003	238	3	360,000	1	15.0	5.9
A1010	703	10	1,170,000	1	48.7	19.3
A1010A	479	11	681,000	1	28.5	11.3
A1020	334	5	216,000	0	9.0	3.6
A1020A	909	13	1,710,000	3	71.5	28.3
A1280	80	3	80,000	0	3.4	1.3
Totals	**3038**	**48**	**4,830,000**	**6**	**202.0**	**79.8**

Overall FITs

Ambient Temp	Activation Energy (eV)	Observed	60% Confidence
90°C	0.6	230	281
70°C	0.6	75	92
55°C	0.6	30	36
90°C	0.9	80	98
70°C	0.9	15	18
55°C	0.9	4	5

High Temperature Operating Life

Product	Run #	Package	# Units	# Hours	# Fail	Temp (°C)	Vcc (Volts)
64KPR	DG1060	24 SB	59	2000	0	125	5.50
64KPR	DG1064	24 SB	36	2500	0	125	5.50
64KPR	JB13	24 SB	40	2000	0	125	5.50
64KPR	JB13	24 SB	40	2000	0	125	7.00
64KPR	JB13	24 SB	10	2000	0	25	8.00
64KPR	JB14	24 SB	50	2500	0	125	5.50
64KPR	JB14	24 SB	50	2500	0	125	7.00
64KPR	JB14	24 SB	10	2500	0	25	8.00
1003	1063	84 JLCC	25	2000	0	125	5.75
1003	1065	84 JLCC	32	2000	0	125	5.75
1003	1065	84 JLCC	159	500	1	150	7.00
1003	1067	84 JLCC	22	1000	0	125	5.75
A1010	DG1042	84 JLCC	3	1000	0	125	5.75
A1010	DG1047	84 JLCC	2	1000	0	125	5.75
A1010	DG1073	84 JLCC	10	2000	0	125	5.75
A1010	DG1077	84 JLCC	15	2000	0	125	5.75
A1010	JB13	84 PLCC	32	2000	0	125	5.75
A1010	JB13	68 PLCC	126	2000	1	125	5.75
A1010	JB13	84 JLCC	64	2000	0	125	5.75
A1010	JB14	68 PLCC	100	2000	0	125	5.75
A1010	JB14	68 JLCC	50	2000	0	125	5.75
A1010	JB22	68 PLCC	100	1000	0	125	5.75
A1010	JB42	68 PLCC	47	1000	0	125	5.75
A1010	JB44	68 PLCC	40	1000	0	125	5.75
A1010	JB46	68 PLCC	49	1000	0	125	5.75
A1010	T124	68 PLCC	65	2000	0	125	5.75

Table 6. High Temperature Operating Life HTOL Test Summary (continued)

High Temperature Operating Life							
Product	**Run #**	**Package**	**# Units**	**# Hours**	**# Fail**	**Temp (°C)**	**Vcc (Volts)**
A1010A	JG03	68 PLCC	59	2000	0	125	5.75
A1010A	JG03	68 PLCC	117	1000	0	125	5.75
A1010A	TI24	68 PLCC	74	2000	0	125	5.75
A1010A	TI29	68 PLCC	53	1000	1	125	5.75
A1010A	TI31	68 PLCC	26	2000	0	125	5.75
A1010A	TI32	68 PLCC	9	2000	0	125	5.75
A1010A	TI33	68 PLCC	19	2000	0	125	5.75
A1010A	TI35	68 PLCC	15	2000	0	125	5.75
A1010A	TI1104 TI1243 TI1263 TI1297	68 PLCC	107	1000	0	125	5.75
A1020	DG1133	84 JLCC	29	2000	0	125	5.75
A1020	JB22	84 PLCC	16	1000	0	125	5.75
A1020	JB22	84 JLCC	32	1000	0	125	5.75
A1020	JB25	84 PLCC	16	1000	0	125	5.75
A1020	JB26	84 PLCC	32	500	0	125	5.75
A1020	JE03	84 JQCC	104	186	0	150	5.75
A1020	JB33	84 JLCC	105	80	0	150	5.75
A1020A	JF01	84 JLCC	25	2000	0	125	5.75
A1020A	JF01	84 PLCC	15	2000	0	125	5.75
A1020A	JF02	84 JLCC	44	2000	0	125	5.75
A1020A	JF02	84 JLCC	41	2000	0	125	5.75
A1020A	JF04	84 PLCC	77	1000	0	125	5.75
A1020A	JF04	84 PLCC	20	500	0	125	5.75
A1020A	JF14	84 PLCC	58	417	0	150	6.00
A1020A	JF14	84 PLCC	100	417	1	150	6.00
A1020A	JF37	84 PLCC	14	300	1	150	6.00
A1020A	JF37	84 PLCC	20	300	0	150	6.00
A1020A	JF39	84 PLCC	32	300	0	150	6.00
A1020A	JF39	84 PLCC	29	300	0	150	6.00
A1020A	JF42	68 PLCC	49	1000	0	150	6.00
A1020A	JF42	68 PLCC	79	1000	1	150	6.00
A1020A	JF67	84 PLCC	49	500	0	125	5.75
A1020A	TI1130 TI1139 TI1210	84 PLCC	223	1000	0	150	6.00
A1020A	TI1800 TI1803	84 PLCC	34	1000	0	150	6.00
A1280	JG03 JG05 JG06	176 PGA	80	1000	0	125	5.75

Table 7. 121°C, 15 psi Steam Pressure Pot (unbiased autoclave)

				Number of Failures			
Product	**Run #**	**Package**	**# Units**	**96 Hours**	**168 Hours**	**240 Hours**	**336 Hours**
A1010	JB13	84 PLCC	34	0	3	–	0
A1010	JB13	68 PLCC	71	1	0	–	0
A1010	JB14	68 PLCC	71	0	0	–	0
A1010	JB22	68 PLCC	50	0	0	–	0
A1010	JB27	68 PLCC	50	0	0	–	0
A1010	JB28	68 PLCC	42	1	0	–	0
A1010A	TI15	68 PLCC	77	0	0	–	0
A1010A	TI24	68 PLCC	129	0	0	–	0
A1010A	TI1104 TI1243 TI1263 TI1297	68 PLCC	77	0	–	0	0
A1020A	TI1800 TI1859 TI2156	84 PLCC	77	0	–	0	–
A1020A	JF33	84 PLCC	30	0	0	0	0
A1020A	JF64	84 PLCC	30	0	0		
A1020A	JF68	84 PLCC	35	0	0		

Failure Analysis:

Three A1010 JB13 failures at 168 hours due to lifted bond wires. Corrective action implemented at assembly vendor.

A1010 JB13 failure at 96 hours same problem as above.

A1010 JB28 failure at 96 hours due to open bond wire caused by lifted die paddle. This was the first qual lot from a new assembly vendor and corrective action was implemented.

Table 8. 85°C/85% Humidity with DC Alternate Pin Bias of 0–5.5 V

				Number of Failures			
Product	**Run #**	**Package**	**# Units**	**168 Hours**	**500 Hours**	**1000 Hours**	**2000 Hours**
A1010	JB13	68 PLCC	80	–	2	1	0
A1010	JB14	68 PLCC	81	–	0	0	0
A1010	JB22	68 PLCC	54	–	0	0	–
A1010	JB26	68 PLCC	54	–	0	0	–
A1010	JB27	68 PLCC	19	–	0	0	–
A1010A	TI1104 TI1243 TI1263 TI1297	68 PLCC	80	0	0	0	–
A1020	JF48	84 PLCC	34	0	0	–	–
	JF49	84 PLCC	49	0	0	–	–
A1020A	JF33	84 PLCC	30	0	0		

Failure Analysis:

A1010 JB13: Two failures at 500 hours. Open pins due to bond lifting. Corrective action implemented at assembly vendor.

One failure at 1000 hours. Horizontal track open (Metal I).

Table 9. Temperature Cycling Test

Product	Run #	Package	# Units	Number of Failures			
				100 Cycles	500 Cycles	1000 Cycles	2000 Cycles
0°C–125°C Cycles							
A1010	DG1077	84 JLCC	20	0	–	–	–
A1010	JB13	68 PLCC	158	0	–	0	–
A1010	JB14	68 PLCC	28	0	–	0	–
A1010	JB26	68 PLCC	21	0	–	0	–
A1010	JB28	68 PLCC	31	0	–	0	–
A1010A	TI15	68 PLCC	125	0	–	0	–
A1010A	TI24	68 PLCC	176	0	–	0	–
A1010A	TI1104 TI1243 TI1263 TI1297	68 PLCC	129	0	0	0	0
A1020	JB22	84 PLCC	17	0	–	0	–
A1020A	TI1800 TI1859 TI2156	84 PLCC	129	0	0	0	0
-40°C–125°C Cycles							
A1010A	TI1104 TI1243 TI1263 TI1297	68 PLCC	129	0	0	0	0
A1020A	TI1800 TI1859 TI2156	84 PLCC	129	0	0	0	0
-65°C–150°C Cycles							
A1010A	TI1104 TI1243 TI1263 TI1297	68 PLCC	129	0	0	0	0
A1020A	TI1800 TI1859 TI2156	84 PLCC	129	0	0	0	0
A1020A	JF33	84 PLCC	116	0	0	0	–

Other Tests

Electro Static Discharge (ESD)

All Actel products contain static electricity protection circuitry and are tested for sensitivity to static electricity by using the human body model as described in MIL-883C (100 pf discharged through 1.5 K ohms). Three positive and three negative pulses are discharged into each pin tested at each voltage level characterized. For inputs and I/Os, these six pulses are applied with three different grounding conditions; Vss only grounded, Vcc only grounded, and all other I/Os grounded. Thus each pin receives a total of eighteen pulses for each test voltage. After pulsing, the units are then tested on a VLSI tester. Leakage currents are measured at 0 V and 5.5 V. Any pin showing more than 1 μA of leakage current is considered to be a failure. To date, all Actel products pass ESD testing at 1000 V. For further information about specific products and packages, please contact Actel.

Latch-Up

Latch-up is a well-known cause of failure in CMOS circuits. Parasitic bipolar transistors are created by the P-Channel transistors, the N-Channel transistors, the N-Well, and the P-Substrate. These transistors are connected in a manner which effectively creates an SCR. If a voltage on an external pin were to forward bias to the substrate, the parasitic SCR can be latched to the on state creating a low impedance path between Vcc and ground. A large amount of current then flows through this path. This current can, at best, temporarily make the device nonfunctional and, at worst, cause permanent damage.

There are several techniques used by CMOS designers to reduce the chance of latch-up. One of the most common techniques is the use of guard rings to isolate P-Channel and N-Channel transistors. The disadvantage of this method is that it requires additional silicon die area. Another method is to use a substrate bias

generator. Creating a negative substrate bias means that an input must go even more negative to cause latch-up. A third technique is to use EPI wafers in order to achieve low substrate resistance, which lowers the chance of triggering latch-up. Actel uses both guard ring and EPI wafer techniques for the A1010/A1020 devices.

The latch-up test method used is defined by JEDEC Standard No. 17. Each I/O pin on a tested device was forward biased in both directions (to Vss and Vcc) by forcing negative and positive currents ranging from +-50 mA to +-250 mA in 50 mA increments. Following each stress, the device Icc current was measured. If the current exceeded the datasheet limit of 10 mA, the unit would be rejected. The device was also functionally tested.

Fifteen units from three different wafer lots were tested. Testing was done at room temperature as well as at a worst case temperature of 135°C. All device I/Os and power supplies were tested. No failures were detected up through 250 mA.

Radiation Hardness

A programmed antifuse makes a connection between an upper layer of polysilicon and an N+ diffusion on the bottom. This connection is very similar to a "buried contact" used in some MOS processes. Many other programmable logic products rely on stored charge to make their connections (i.e., RAM, EPROM, or EEPROM). This stored charge can be susceptible to degradation due to radiation exposure. The Actel antifuse makes a hard contact and does not rely on stored charge. As a result, one would expect the Actel products to have superior radiation tolerance as compared to products which use stored charge.

Although Actel has not yet performed any radiation testing, several customers and independent laboratories have performed tests and shared their data. This data shows the A1010/A1020 devices can withstand a total radiation dose in excess of one million RADs. Upsets/bit-day have been measured at 1×10^{-6}. Single Event Upset (SEU) sensitivity measurements gave an asymptotic cross-section of 3.6×10^{-6} cm^2/bit. The threshold for Linear Energy Transfer (LET) was 22 MeV-cm^2/mg. For further information, please contact Actel.

Summary

The data presented in this report establishes the excellent reliability of the Actel A1010/A1020. Both Actel models and actual device testing show that the antifuse is highly reliable and that the combined contribution of all antifuses to the gate array product's hard failure rate is less than 10 FITs (Failures-in-Time) or 0.001% failures per 1000 hours.

References

1) E. Hamdy, et al, "Dielectric Based Antifuse for Logic and Memory ICs", IEDM paper, p. 786-789, 1988.

2) S. Chiang, et al, "Oxide-Nitride-Oxide Antifuse Reliability", Proc. Int. Rel. Phys. Symp., 1990

3) J. Lee, I-Chen, and C.Hu, "Modeling and Characterization of Gate Oxide Reliability", IEEE Trans. of Elec. Dev., Dec. 1988.

ACT 2 Addendum

High Temperature Operating Life

Product	Run #	Package	# Units	Pattern	# Hours	# Fail	Temp	Vcc
1240	TI3257	132 PGA	7	CHI1240	500	0	125	5.75
1240	TI3257	144 PQFP	129	CHI1240	1000	0	125	5.75
1240	TI1045571	132 PGA	38	CHI1240	2000	0	125	5.75
1240	TI1053933	132 PGA	55	CHI1240	2000	0	125	5.75
1240	TI1053932	132 PGA	36	CHI1240	2000	0	125	5.75
1240	UI-01	132 PGA	50	CHI1240	1000	0	125	5.75
1280	JH05	176 PGA	15	BETA12	2000	0	125	5.75
1280	JH06	176 PGA	15	BETA12	2000	0	125	5.75
1280	JH03(K)	176 PGA	25	BETA12	2000	0	125	5.75
1280	JH03(SB)	176 PGA	25	BETA12	2000	0	125	5.75
1280	TI1143649	176 PGA	44	BETA12	1000	1	125	5.75
1280	TI1143650	176 PGA	44	BETA12	1000	0	125	5.75
1280	TI1136307	176 PGA	42	BETA12	1000	0	125	5.75
1280	UH-01	176 PGA	26	BETA12	1000	0	125	5.75
1280	UH-02	176 PGA	26	BETA12	1000	0	125	5.75
1280	UH-05	176 PGA	40	SPEED9	1000	0	125	5.75
1280	UH-04	160 PQFP	80	SPEED12	168	0	125	5.75

HTOL Summary:

Total Units:	697
Total Runs:	15
Total Device Hours:	8.23E+05
Total Failures:	1

Equivalent Device Hours:

Ambient Temp, Activation Energy	Device Hours
70C, 0.6EV	1.36E+07
55C, 0.6EV	3.44E+07
70C, 0.9EV	5.53E+07
55C, 0.9EV	2.23E+08

FITS:

	Observed	60% Confidence
70C, 0.6EV	74	162
55C, 0.6EV	29	64
70C, 0.9EV	18	40
55C, 0.9EV	4	10

Failure Analysis:

Product	Run #	Hours	Cause
1280	TI1143649	500	TRISTATE LKG PIN 28 (IN FAILURE ANALYSIS)

85°C/85% Humidity with DC Alternate Pin Bias of 0–5.5 V:

				Number of Failures			
Product	Run #	Package	# Units	168 Hours	500 Hours	1000 Hours	2000 Hours
1240	TI3256	144 PQFP	78	–	0	0	–

Temperature Cycle:

-65°C–150°C Cycles:

				Number of Failures			
Product	Run #	Package	# Units	200 Cycles	500 Cycles	1000 Cycles	2000 Cycles
1225	UJ-01	100 PGA	80	0	–		
1240	TI1053932	132 PGA	15	0	0	0	
	TI1045571	132 PGA	20				
	TI1053933	132 PGA	42				
1240	TI 3256	144 PQFP	80	–	0	0	
1240	UI-01	132 PGA	50	0	–		
1240	UI-02	132 PGA	50	0	–		
1280	TI1136307	176 PGA	71	0	–	0	
	TI1143650	176 PGA	5	0	–	0	
	TI1143649	176 PGA	1	0	–	0	
1280	UH-01	176 PGA	25	0	–	0	
1280	UH-02	176 PGA	26	0	–	0	
1280	UH-04	160 PQFP	34	0	–		
1280	UH-14	160 PQFP	48	0	–		

Thermal Shock -65°C–150°C:

					Number of Failures			
Product	Run #	Package	# Units	100 Cycles	200 Cycles	500 Cycles	1000 Cycles	2000 Cycles
1280	UH-01, 02	176 PGA	30	0	–			
1240	TI1149935		43	–	0			

121°C, 15 PSI Steam Pressure Pot (Unbiased Autoclave):

				Number of Failures			
Product	Run #	Package	# Units	96 Hours	168 Hours	240 Hours	336 Hours
1240	TI10301	144 PQFP	79	–	0	–	0

Testing and Programming the A1010/A1020

By Ken Hayes

Introduction

Users of masked gate arrays have long had to struggle with testability issues. In order to avoid board level, system level, or even possible field failures, the system designer is forced to extend much effort to develop test vectors for gate array designs. Even after the vectors are developed, fault coverage for typical designs may be only about 70% with 95% coverage being about the best possible. With a 70% fault coverage, it has been shown that typical masked gate array designs are likely to have 2% to 5% defective devices[1].

Field programmable logic devices have allowed the user to generally avoid the need to develop test vectors due to tests performed by the semiconductor vendor prior to programming. However, most one-time programmable logic devices have not yet achieved the functional quality levels of other semiconductor devices because it is not possible for the chip manufacturer to access and test all internal gates. Early one-time programmable devices had poor test coverage and users were often disappointed to see functional failure rates of more than 10 percent on parts that had passed programming. However, on-chip test circuits and testing techniques have greatly improved over time and now one-time programmable devices have functional defect rates in the range of 0.1 to 1 percent[2]. Although this failure rate is low for individual chips, putting 10 such chips on a single board can contribute to a 5 to 10 percent board failure rate.

Reprogrammable logic devices which use EPROM, EEPROM, or RAM technology have improved functional quality levels to nearly 100%. Since the semiconductor manufacturer can program these chips to any desired configuration, it is possible to test all internal gates. This can result in functional failure rates equivalent to most other semiconductor devices.

Testability of the A1010/A1020

Although Actel's ACT™ 1 Family arrays use a one-time programmable technology, the device's unique architecture permits a degree of testability comparable to reprogrammable devices. Special test modes allow functional testing of unprogrammed devices at essentially 100% fault coverage. This testability is independent of the large number of equivalent gates in the A1010 (1200 gates) and the A1020 (2000 gates). In order to show how this is accomplished, we will first review the architecture of the A1010/A1020 describe how they are programmed.

Architecture

The basic building block of the A1010/A1020 is the Logic Module. Each Logic Module is programmable and capable of implementing all two input logic functions, most three input functions, and many other functions up to seven inputs. For sequential circuits, latches can be implemented with one Logic Module while flip-flops use two. With an architecture similar to a channeled gate array, Logic Modules are organized in rows and columns across the chip (Fig. 1). Adjacent to each row of Logic Modules are routing channels. Horizontal routing channels are shown in the figure but vertical channels also exist (running through the Logic Modules). Routing channels are used to configure a Logic Module and connect inputs and outputs of Logic Modules together to implement a design. Surrounding the array of Logic Modules and routing channels are I/O buffers and test circuits.

Within the routing channels are programmable antifuse (PLICE™) elements. The antifuse is normally open and is programmed to form an electrical connection between routing elements. An antifuse which connects a horizontal routing track to a vertical track is called a cross antifuse. An example of a Logic Module interconnection (or a net) is shown in Figure 2. Here, the output from Module 3 is connected to a horizontal routing track by programming a cross antifuse. Another cross antifuse is programmed to connect an input from Module 4. In a similar manner, the output of Module 3 is connected to the input of Module 2. Notice that not all horizontal tracks are continuous across the chip. Often tracks are broken into a series of smaller tracks called "segments". Segments are useful because it is often desirable to connect Logic Modules which are close to each other, and using a full horizontal track would waste routing resources and slow down circuit performance. Sometimes, however, it is necessary to connect two segments together to form a longer segment. This can be done by programming a special type of antifuse referred to as a horizontal antifuse. As an example, the output of Module 3 is also connected to the input of Module 1 by programming two cross antifuses and one horizontal antifuse. The A1010/A1020 also have vertical antifuses used to connect two vertical segments (not shown).

A more detailed example of the A1010/A1020 architecture is shown in Figure 3. Six Logic Modules (two rows, three columns) are shown. Between the two rows are six horizontal tracks. Down each column are five vertical tracks. Note that the actual A1010/A1020 typically have 25 horizontal and 13 vertical tracks. The circles at the intersection of vertical and horizontal tracks represent cross antifuses. There are also circles at certain points on the horizontal tracks which are horizontal antifuses. No vertical antifuses are shown. Notice the transistors which connect both horizontal and vertical tracks. These are referred to as horizontal and vertical pass transistors. By turning on selected transistors, various horizontal or vertical tracks can be connected together even though an antifuse has not been programmed. This ability to connect tracks in unprogrammed devices is used extensively during antifuse programming and is one of the key elements responsible for the excellent testability of the A1010/A1020.

Configuration of Logic Modules is interesting because there are no dedicated antifuses in the Module in order to accomplish this. Instead, the inputs (and outputs) of Logic Modules extend into the cross antifuse array. Each Logic Module has eight inputs and one output. By programming appropriate antifuses, an input can be connected to a dedicated horizontal ground line, a Vcc line, or a horizontal routing track. The Logic Module implements a particular logic function by tying appropriate unused inputs to ground or Vcc.

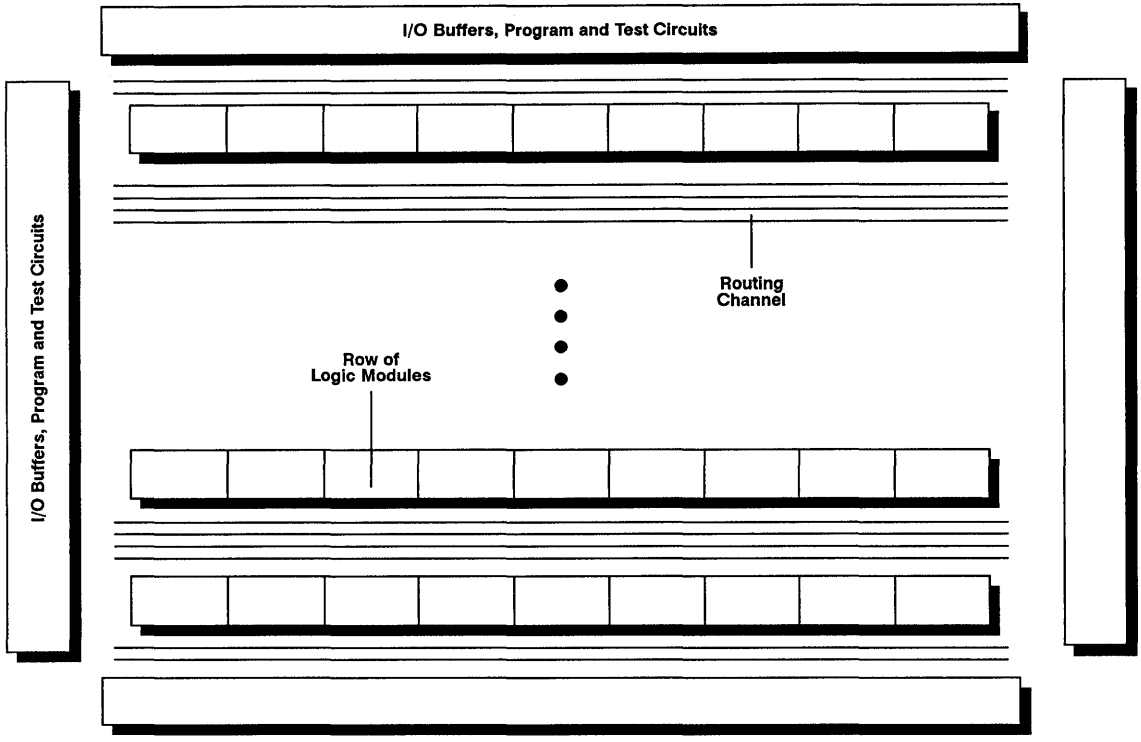


Figure 10. Architecture

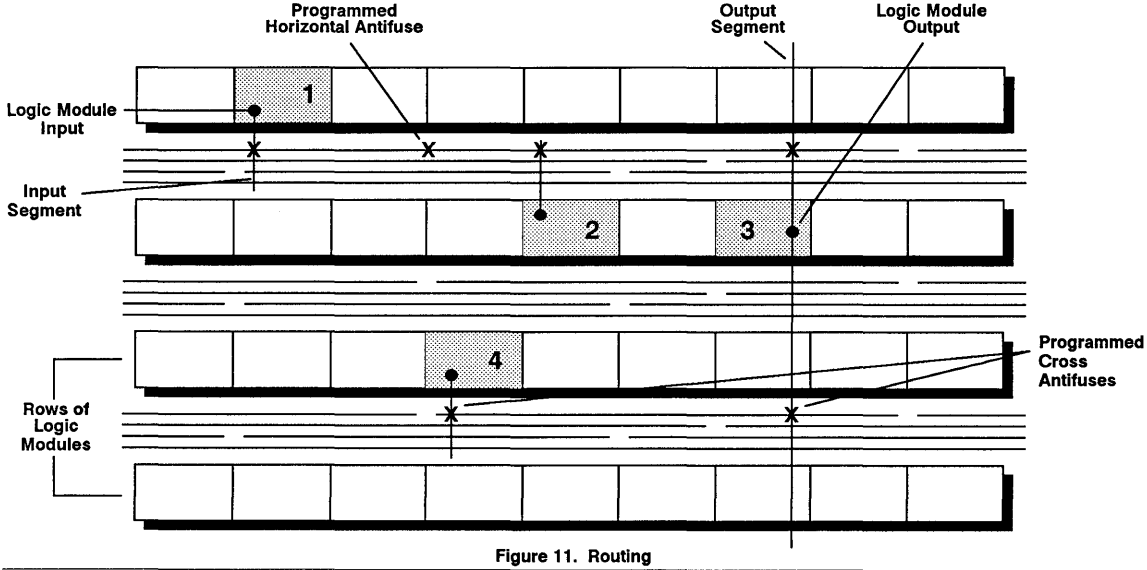


Figure 11. Routing

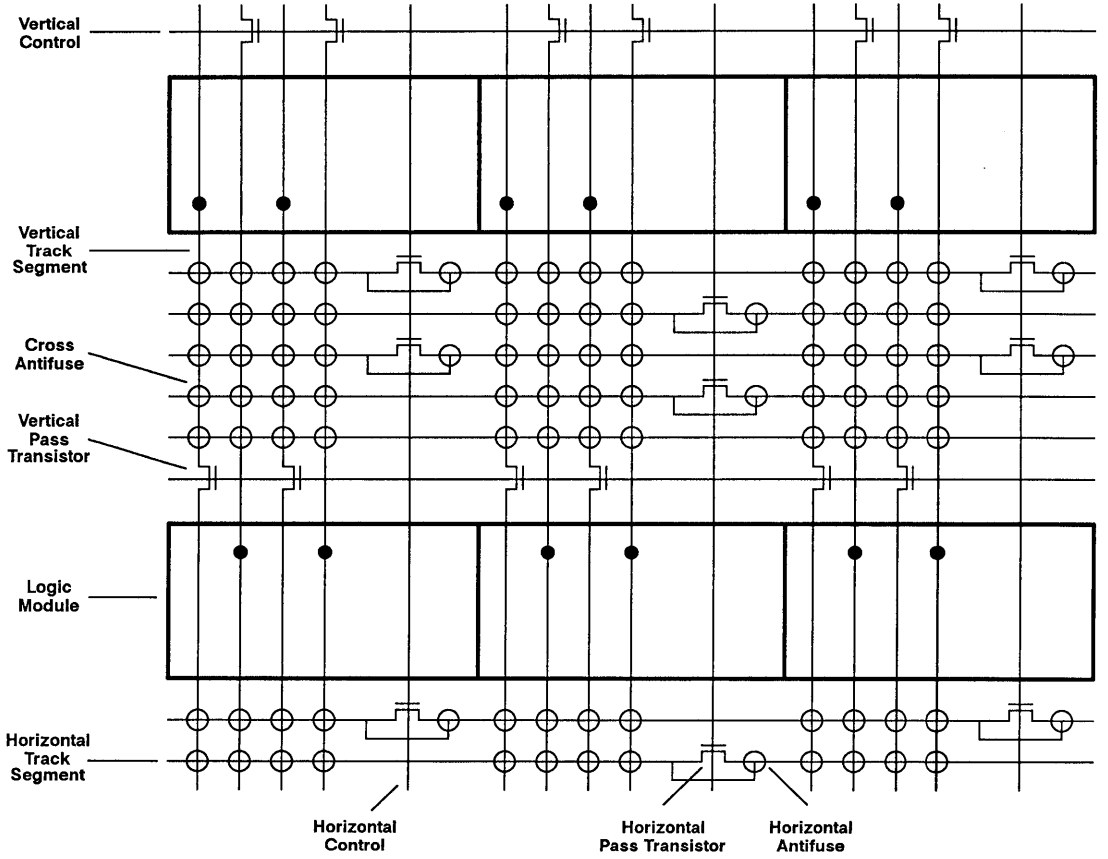


Figure 12. Programmable Interconnect

Programming

An antifuse is programmed by applying a sufficiently high voltage across it. This voltage is referred to as Vpp. In order to access an antifuse deep inside the chip, it is necessary to create electrical paths from Vpp and ground to the antifuse. This is done by turning on the appropriate horizontal and vertical pass transistors (in normal chip operation, these transistors are always off). The transistors are turned on by applying Vpp to their gates. In Figure 4A, we see an example of programming a typical cross antifuse. Vpp is applied to a vertical track at the top of the chip and ground is applied to a horizontal track on the right side. The design of the A1010/A1020 actually allows applying Vpp or ground from the top, bottom, left, or right as is appropriate to best access a particular antifuse. Notice that Vpp is also applied to the gates of the horizontal and vertical pass transistors on the tracks accessing the cross antifuse. The circled cross antifuse now has Vpp applied to it on one side and ground on the other. This voltage breaks down the antifuse's dielectric and creates an electrical connection between the horizontal and vertical routing tracks.

There is one other important consideration when programming an antifuse. Notice that the cross antifuses in the same vertical track as the antifuse to be programmed also have Vpp applied to them on one side. This is true until the track is broken by a vertical pass transistor below it which is turned off. However, the potential on the other side of the antifuses is not being driven. Should this potential be at ground, the other cross antifuses on the vertical segment could be accidently programmed. The same logic applies to other antifuses on the same horizontal track. Here, one side of the antifuse is being driven to ground and if the other side were at Vpp, extra antifuses could program.

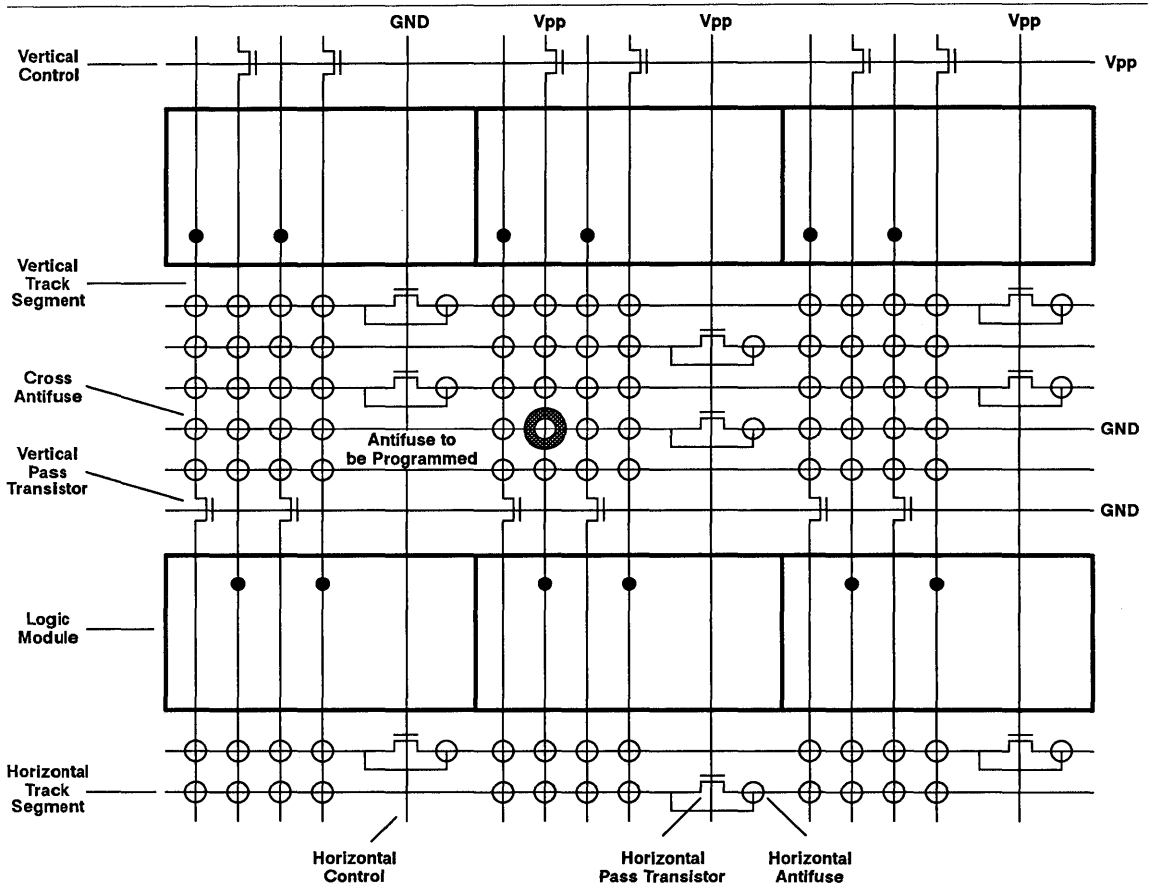


Figure 4A. Programmable Interconnect

The above problem is solved by first applying what is referred to as a "precharge cycle." During the precharge cycle, all horizontal and vertical tracks are charged to Vpp/2. As a result, there is no voltage across the antifuses. The appropriate vertical track is then driven to Vpp and a horizontal track to ground (Fig. 4B). At this point, other antifuses on the vertical track have a potential of Vpp/2 across them (Vpp on one side and Vpp/2 on the other). This Vpp/2 voltage is not sufficient to program the antifuses. Other antifuses on the same horizontal track also have Vpp/2 across them (Vpp/2 on one side and ground on the other). Most other antifuses in the chip still have Vpp/2 on both sides and will not program.

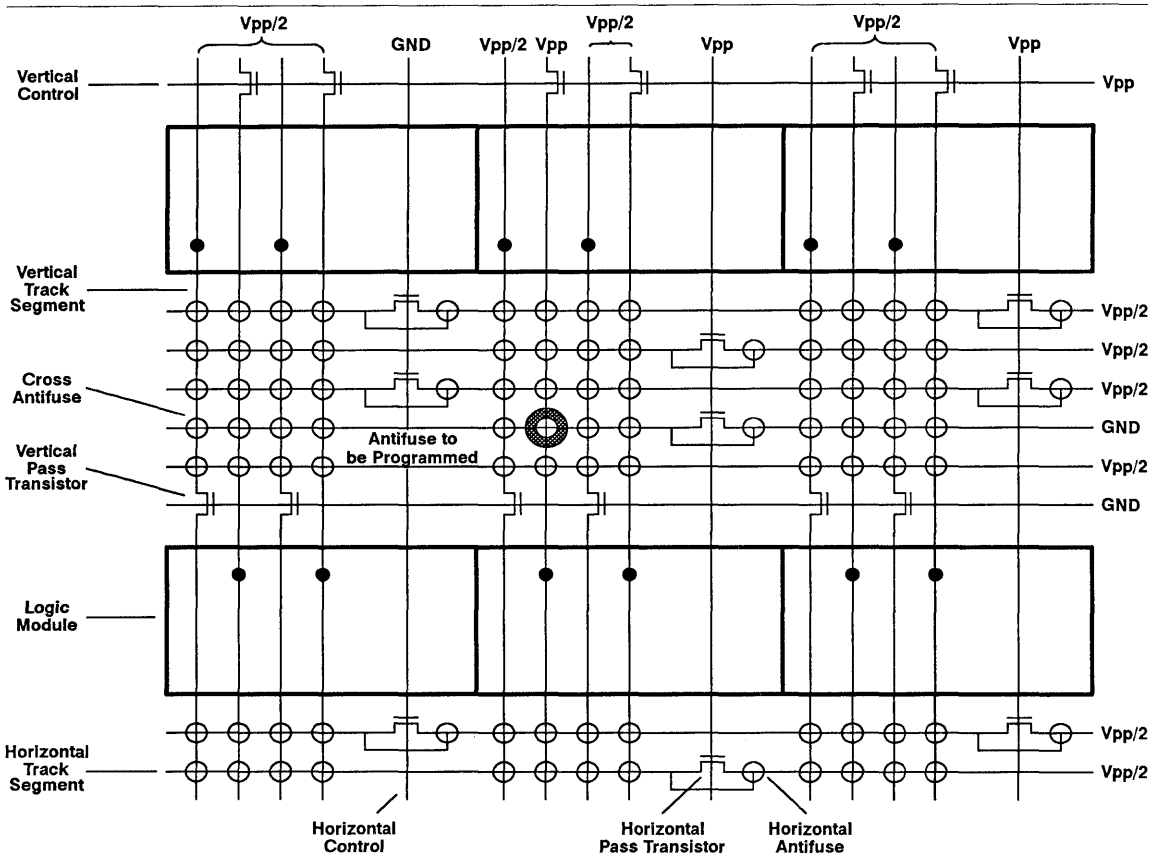


Figure 4B. Programmable Interconnect

Programming Algorithm

In concept, the A1010/A1020 are programmed in a manner very similar to many other programmable logic devices as well as memories such as EPROMs. The programming algorithm consists of:

1. An addressing sequence to select the antifuse to be programmed.
2. A programming sequence where Vpp is applied in pulses until the antifuse programs.
3. A soak or "overprogram" step to assure uniform, low antifuse resistance.
4. A verify step to make sure the antifuse was properly programmed.

Unlike a memory where an antifuse is addressed by applying a parallel address, the A1010/A1020 are addressed in a serial manner by using the special DCLK (Data Clock) and SDI (Serial Data In) pins. There is a large shift register which travels around the periphery of the chip. Bits in this shift register can be used to drive tracks to ground, Vcc, Vpp, or float. It is also possible to sense the level on the track (high or low) and load this information into the shift register. The shift register is about 320 bits long in the A1010 and 420 bits long in the A1020 (due to the larger number of tracks). By shifting in the correct address, any antifuse can be selected for programming. The shift register also plays a key role in the testing of the chip. This will be discussed later.

The programming sequence starts with the precharge pulse where Vpp/2 is applied to the Vpp pin. This is followed by a programming pulse where Vpp is applied to the pin. Following the program pulse, the voltage on the Vpp pin is returned to a nominal value (about 6 volts). See Figure 5 for a typical Vpp waveform example. The precharge/program pulse sequence is repeated until either the selected antifuse programs or a maximum number of pulses is exceeded (in which case the antifuse is considered non-programmable and the device is rejected).

Confirmation that an antifuse has programmed is determined by monitoring the current on the Vpp pin. This current is very low (typically < 10 ua) until an antifuse programs. Once an antifuse is programmed, an electrical connection is made between Vpp and ground in which case currents in the range of 3-15ma may be

observed on Vpp. Once this current is observed, the antifuse is considered programmed and enters the soak or "overprogram" cycle. Here, extra pulses are applied to the antifuse to achieve minimum antifuse resistance.

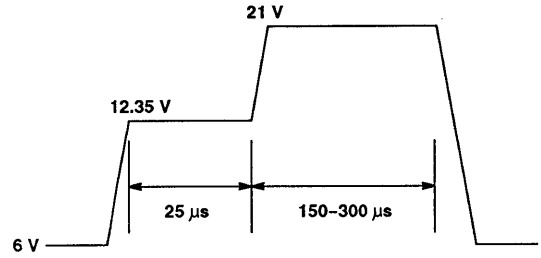


Figure 5. Vpp Waveform

ACT Family Programming Algorithm

Current Parameters

V Program	=	21 V
V Precharge	=	12.35 V
V Verify	=	6.0 V
t Program	=	150 -300 µs
t Precharge	=	25µs
I Threshold	=	~2.5mA (to detect programmed antifuse)
I Max	=	15 mA (clamp current)
# Soak	=	30-800 pulses
Maxpulses	=	60,000

Test Modes of the A1010/A1020

The unique architecture described above allows outstanding testability of unprogrammed devices at the factory. Details of the various test modes available are as follows:

1. The shift register circling the periphery of the chip can be both downloaded and uploaded. This allows the use of various test patterns to assure the shift register is fully functional.
2. All vertical and horizontal tracks can be tested for continuity and shorts. There are several ways to implement these tests. One way of doing continuity testing is to precharge the array, turn on all vertical or horizontal pass transistors on a track, drive the track low from one side of the chip, and read a low on the other side. Shorts can be detected by driving every other track low after precharge and reading back on the other side. Note that these tests also confirm that the vertical and horizontal pass transistors will turn on.
3. It is important for programming to make sure that all tracks can hold the precharge level. By charging a track, floating it, and waiting a predetermined amount of time, the track can be read back and confirmed it is still high.
4. Leakage of vertical and horizontal pass transistors can be tested for by driving one side of a track to a voltage via the Vpp pin and grounding the other side. All pass transistors except the one being tested are turned on. If excess current is detected on the Vpp pin, the pass transistor is considered defective.
5. The A1010/A1020 have a dedicated clock buffer which travels across all horizontal channels. This buffer can be tested by driving with the clock pin and reading for the proper levels at the sides of the array.
6. The A1010/A1020 have two special pins referred to as Probe A and Probe B (Actionprobes™). By entering a test mode, the shift register can be made to address the internal output of any Logic Module. This output is then directed to one of two dedicated vertical tracks which in turn can be observed externally on the Probe A or B pins. This ability to observe internal signals (even on unprogrammed parts) allows Actel to perform a large number of functional tests. The first such test is the Input Buffer Test. Input buffers on all I/O pins can be tested for functionality by driving at the input pad and reading the internal I/O output node through the probe pins.
7. Test modes exist to drive all output buffers low, high, or tristate. This allows testing of Vol, Voh, Iol, Ioh, and leakage on all I/Os.
8. One of the key tests is the ability to functionally test all internal Logic Modules. By turning on various vertical pass transistors and driving from the top or bottom of the chip, any of the eight module inputs can be forced to a high or low. The output of the module can then be read through the Actionprobe pins. The Logic Module test allows 100% fault coverage of each Module. In addition, the architecture allows Modules to be tested in parallel for reduced test time.
9. The A1010/A1020 have two dedicated columns on the chip which are transparent to the user and used by the factory for speed selection. These columns are referred to as the "Binning Circuit." Modules in the columns are connected to each other by programming antifuses. The speed of the completed test circuit can then be tested. The Binning Circuit allows the separation of units into different speed categories. It also allows the speed distribution within each category to be minimized.
10. There are several tests to confirm the programming circuitry is working. The first such test is a basic junction stress/leakage test. The program mode is enabled and Vpp voltage plus a guardband is applied to the Vpp pin. All vertical and horizontal tracks are driven to Vpp; thus no voltage is applied across the antifuses. The Ipp current is then measured. If it exceeds its normal value, the device is rejected.
11. The A1010/A1020 have a test to assure all antifuses are not programmed. This is referred to as the Antifuse Shorts Test (or Blank Test). The array is precharged and then the vertical tracks are driven to ground. The horizontal tracks are then read to confirm they are still high (a programmed or leaky antifuse would drive a horizontal track low). The test is repeated by driving horizontal tracks low and reading vertical tracks.
12. The functionality of the programming circuitry can be verified by programming various extra antifuses on the chip which are transparent to the user. Some of these antifuses were already described earlier when the Binning Circuit was discussed. The A1010/A1020 also have a Silicon Signature™. The Silicon Signature consists of four words of data, each

word 23 bits in length. The first word is hard wired (no antifuses) and contains a manufacturer ID number as well as a device ID number. These numbers can be read by a programmer and the proper programming algorithm would be automatically selected. The other words contain antifuses and are programmable. Actel is currently using bits in these words to store information such as the wafer number and run number the chip came from. Thus each A1010/A1020 has traceability down to the wafer level. By programming this information, the functionality of the programming circuitry is also tested. Future Actel software will allow the user to program a design ID and checksum into the Silicon Signature, and by later reading this back, the user can verify the chip is correctly programmed to a given design.

13. The most important antifuse test is the stress test. When this test is enabled, a voltage applied to the Vpp pin can be applied across all antifuses on the chip (the other side is grounded). The voltage applied is the precharge voltage plus a significant guardband. After the voltage is applied, the Antifuse Shorts Test is again used to make sure no antifuses have programmed. The antifuse stress test is effective at catching antifuse defects. Since the reliability of the antifuse is much more voltage dependent than it is temperature dependent, this test is also an effective antifuse infant mortality screen. See the Actel A1010/A1020 Reliability Report for details.

Burn-In of the A1010/A1020

As mentioned above, Actel has found that antifuse infant mortality failures can be effectively screened out during electrical testing, and it is thus unnecessary to do any kind of burn-in for standard commercial production units to screen out antifuse infant mortality failures. However, burn-in is still an effective screen for standard CMOS infant mortality failure mechanisms, and it is required for all military 883C Class B products. MIL-883C Method 1005 allows several types of burn-in screens. These can be divided into two categories: steady-state (static) and dynamic. Static burn-in applies DC voltage levels to the pins of the device under test. The device may or may not be powered up. Dynamic burn-in applies AC signals to device inputs. These signals are selected such that the device receives internal and external stresses similar to what it may see in a typical application.

Static burn-in is by far the simplest method to implement. By choosing appropriate biasing conditions and load resistors, it is possible to design a single burn-in circuit which could be used for both unprogrammed and programmed devices. It would not matter what pattern is programmed into the device. Static burn-in can be an effective screen for some types of failure modes, particularly those which may happen at device inputs or outputs (such as screening for mobile ionic contamination). It is not, however, very effective at stressing internal device circuits. Many internal nodes may be biased at ground without receiving any voltage or current stress. Signal lines will not toggle, and it may not be possible to screen failure modes such as metal electromigration.

A properly designed dynamic burn-in can effectively stress inputs, outputs, and internal circuits. However, dynamic burn-in of ASIC products can be very expensive because customer specific custom burn-in circuits and burn-in boards must be designed and built in order to properly stress each design implemented in the ASIC. This results in large NRE costs and long lead times to design and build these boards. From the standpoint of burn-in, a programmed A1010/A1020 FPGA is essentially the same as a mask-programmed ASIC, and it would require similar custom burn-in circuits to do a dynamic burn-in. However, Actel has been able to use the testability features of its FPGA products to allow effective dynamic burn-in of unprogrammed devices. This dynamic burn-in allows us to stress circuits in a way which static burn-in would be unable to duplicate.

During burn-in of unprogrammed units, test commands are serially shifted into each device using the SDI pin and clocked using the DCLK pin. There are three test modes shifted into each device. The first test stresses each cross antifuse with a voltage of Vpp–2V (Vpp is normally set at 7.5V so each antifuse gets 5.5V across it). This voltage is applied to all vertical tracks while the horizontal tracks are grounded. It requires 322 bits of data to enable this mode for the A1010 and 416 bits for the A1020. The data is shifted in at a 1 MHz cycle rate. Once enabled, the stress mode is held for 10 ms.

The second test mode is identical to the first except that the horizontal tracks are driven to Vpp–2 V while the vertical tracks are grounded. Note that both of these modes are similar to the antifuse stress tests described earlier (although the stress voltage is lower during burn-in). Not only do these tests stress the antifuses, but they also toggle all routing tracks in the chip to Vpp–2V and ground. All input and output tracks to the logic modules are also toggled.

The third test drives several I/O pins on the chip to a low state. Prior to this, they are at high impedance state and held at Vcc through pull-up resistors. This test confirms that the burn-in is being properly implemented by looking at these I/O pins to see if they display the proper wave form. It also passes current through each I/O as it toggles low.

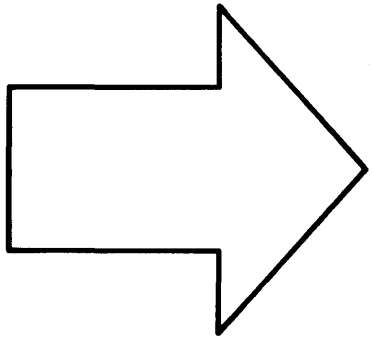
Although the chip is unprogrammed, the above tests allow us to apply stresses to the inputs, outputs, and internal nodes which are similar to what a programmed device may see in normal operation. Once burn-in is completed, post burn-in testing as specified by MIL-883C is performed (including PDA) to assure fully compliant devices are shipped to the customer.

Conclusion

The description of the A1010/A1020 architecture and the numerous test modes attest to the outstanding testability of these devices. All internal logic gates can be tested without programming antifuses other than the few for the Binning Circuit and Silicon signature. Because the A1010/A1020 are one-time programmable, the only item that is not fully tested at the factory is the programmability of all the individual antifuses. However, this is done on the programmer while the units are being programmed. Being able to test all internal gates allows Actel to achieve functional yields that are superior to other one-time programmable devices and equivalent to reprogrammable parts.

1 Henshaw, "User Requirements for Fault Coverage", Wescon Proceedings, 1990, P. 179

2 AMD PAL Device Data Book, 1988, P. 3-106



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Article Reprint 3

AN ARCHITECTURE FOR ELECTRICALLY CONFIGURABLE GATE ARRAYS

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An Architecture for Electrically Configurable Gate Arrays

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Abstract — **An architecture for electrically configurable gate arrays using a two-terminal anti-fuse element is described. The architecture is extensible, and can provide a level of integration comparable to mask-programmable gate arrays. This is accomplished by using a conventional gate array organization with rows of logic modules separated by wiring channels. Each channel contains segmented wiring tracks. The overhead needed to program the anti-fuses is minimized by an addressing scheme that utilizes the wiring segments, pass transistors between adjacent segments, shared control lines, and serial addressing circuitry at the periphery of the array. This circuitry can also be used to test the device prior to programming and observe internal nodes after programming. By providing sufficient wiring tracks segmented into carefully chosen lengths and a logic module with a high degree of symmetry, fully automated placement and routing is facilitated.**

I. Introduction

MASK-programmable gate arrays offer the architectural flexibility and efficiency to integrate thousands of gates, but require long development time and high nonrecurring engineering costs. On the other hand, the convenience of field programming is available with programmable logic device (PLD) technologies, but their architectures have not allowed integration of a wide variety of applications exceeding a few hundred gates [1], [2].

We describe a novel gate array architecture [3] which combines the flexibility of mask-programmable arrays with the convenience of field programmability. Its implementation is made possible by a two-terminal electrically programmable anti-fuse offering low resistance in its conducting state and small area.

The architecture supports a design style similar to conventional gate arrays, including fully automatic placement and routing algorithms attaining 85–95-percent utilization. This required considerable emphasis on symmetry and routability, which we touch on below.

The anti-fuse is so called because it irreversibly changes from high to low resistance when "blown" by applying a programming voltage across it. The anti-fuse, or fuse for short, has an ON-state resistance of approximately 500 Ω. The layout area of the fuse cell is generally limited by the pitch of the first- and second-level metal lines that connect to it; it is about the same size as a via.

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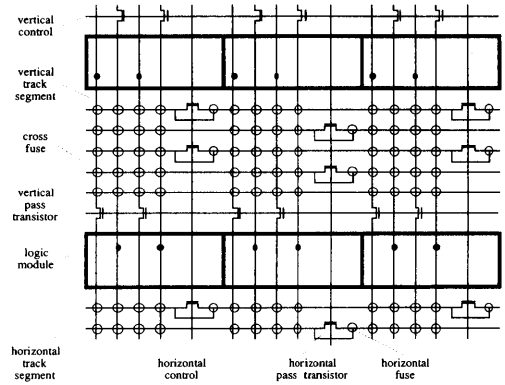

Fig. 1. Interconnect architecture.

This paper focuses on the architecture itself, which is fairly independent of the exact details of the particular CMOS technology and the anti-fuse. Other papers describe more fully the anti-fuse [4], a CMOS circuit implementing the architecture [5], and a study comparing the architecture's logic density to that of conventional gate arrays [6].

II. Programmable Interconnect Architecture

The general architecture, shown in Fig. 1, exhibits the familiar gate array organization: rows of logic cells interspersed with routing channels. There are, of course, several key differences.

The tracks in the channels are not simply empty areas in which metal lines can be arranged for a specific design. Rather, they contain predefined wiring "segments" of various lengths. Other wiring segments pass through the channels vertically. Each input and output of a logic module is connected to a dedicated vertical segment. Other vertical segments just pass through the modules, serving as feedthroughs between channels. (The number and lengths of segments in Fig. 1 are only suggestive.)

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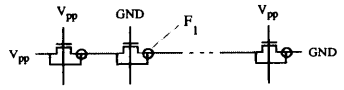

Fig. 2. Horizontal fuse programming.

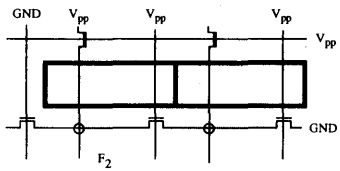

Fig. 3. Cross-fuse programming.

A fuse is located at each crossing of a horizontal and vertical segment. Programming one of these "cross fuses" provides a low-resistance bidirectional connection between the segments. Other fuses are located between adjacent horizontal segments within a track. When blown, these "horizontal fuses" connect the two segments to form a longer one. (Although not shown in the diagram, fuses may also be provided to connect adjacent vertical segments.)

In order to program a fuse, we need to apply high voltage across it. This is accomplished by an efficient addressing scheme that uses the wiring segments themselves, pass transistors connecting adjacent segments, and control logic at the periphery of the array. Fuse addresses are shifted into the chip serially.

As shown in Fig. 1, each column of "horizontal pass transistors" connecting horizontal tracks is controlled by a shared "horizontal control" line running across the array. Each row of "vertical pass transistors" is controlled by a "vertical control" line. The peripheral circuitry can drive the control lines and the segments at the end of each track.

Horizontal fuse programming is quite simple. In the example of Fig. 2, we apply programming voltage V_{PP} across the fuse F_1. All horizontal control lines except the one in the column containing F_1 are turned on by connecting them to V_{PP}, and the appropriate track segments are driven to *GND* and V_{PP} as shown. (Vertical fuses, if present, are programmed similarly.) Cross-fuse programming uses both horizontal and vertical control lines as shown in Fig. 3. Segments not driven to either *GND* or V_{PP} are left precharged to $V_{PP}/2$. Thus the voltage across fuses not being programmed is either zero or $V_{PP}/2$.

Some care is required to assure that a unique fuse is addressed. Fig. 4 shows how previously blown fuses can divert current along a "sneak path," in this case programming fuse F_5 through previously blown fuses F_3 and F_4 instead of programming F_2. Fortunately, we are not interested in blowing an arbitrary pattern of fuses (this is not a PROM!). For example, we are not concerned with programming a pattern that connects two outputs together since this does not form a useful net. If we consider only relevant patterns, it can be shown that programming the fuses in a carefully chosen order eliminates sneak paths. In general, fuses must be programmed starting from the center of the chip and moving outward, channel by channel. Determining the proper order is a bin sort operation, and can be done by software in linear time.

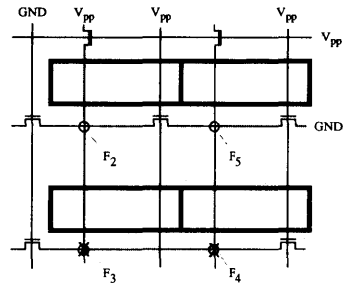

Fig. 4. A sneak path.

TABLE I

macro	4 transistor cells	modules
3 input NOR	2	1
4:1 mux, non-inverting	6	1
D latch with clear	4	1
D flip-flop with clear/set	7	2
full adder	10	2

The pass transistors and peripheral control logic are also used to test the chip; this is discussed in detail later.

III. Choice of the Logic Module

As outlined so far, the programmable interconnection architecture could be used with a variety of logic modules. Which would be best? This turned out to be a very difficult question, involving subtle trade-offs among routability, the logical capability of the module as perceived by the user, and delays due to capacitive loading in the routing segments.

The complexity of the module must be balanced with the routing overhead. Mask-programmed gate arrays provide very flexible and efficient routing. They therefore use a simple four-transistor cell. On the other hand, routing is very expensive in both area and delay with present programmable logic arrays. These generally use a module capable of implementing more complex functions [2]. The architecture outlined here has a cost of routing closer to a conventional gate array, suggesting a logic module of intermediate size. Because this is about the same complexity as conventional gate array hard macros, the designer can use a library like the familiar gate array cell libraries; there is no need to map logic into a more complex module. Table I lists several typical gate array macros and the numbers of four-transistor cells and logic modules required to implement them.

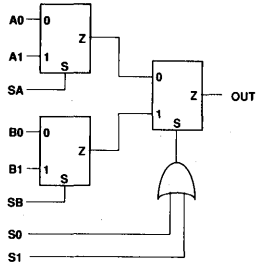

Fig. 5. Module function.

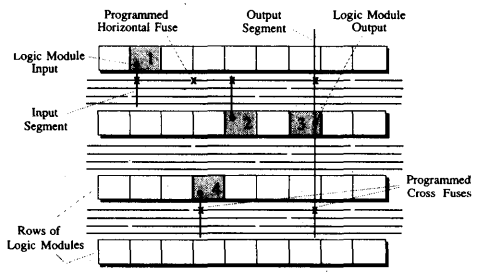

Fig. 6. A routing path.

Our chosen module, shown in Fig. 5, has eight inputs and a single output. It is composed of three two-to-one multiplexors, with an OR gate on the last stage's select input. Various macros, such as those in the table, are implemented by using an appropriate subset of the inputs and tying the remaining inputs high or low. Thus the module can implement all macros with two inputs, most with three inputs, many with four inputs, etc.

The module's output is connected to a vertical segment spanning several channels. Each input is connected to a short vertical segment spanning one channel. Four of these span the channel above the module, four the channel below. The use of short segments for the inputs reduces parasitic capacitance and hence delay.

Note that each input is accessible from either the channel above or below but not both. At first, this would appear to limit routability compared to a conventional "double-entry" gate array cell, in which signals may enter from either channel. However, there is nearly always more than one way to implement a macro. For example, there may be up to four distinct ways to implement a two-input gate: with both signals connecting to inputs in the top channel, with both signals connecting to inputs in the bottom channel, with one signal in the top and the other in the bottom channel, or vice-versa.

By letting the router choose an implementation that uses inputs accessed from convenient channels, the benefits of full double-entry symmetry are approached or sometimes attained. The degree of symmetry possible for a particular macro m implemented in a given module is reflected in the following measure S:

$$S(m) = \log_2(N(m))$$

where $N(m)$ is the number of distinct possible implementations of the macro m. Full double-entry symmetry would correspond to a value $S(m)$ equal to the fan-in of the macro. To evaluate the overall symmetry of a module, we average $S(m)$ over the macro library, weighted by relative macro usage $U(m)$ and the fan-in $F(m)$:

$$\frac{\sum_m U(m)S(m)}{\sum_m U(m)F(m)}.$$

This is the effective fraction of macro inputs in a typical design that have double-entry symmetry, and is an important criterion for choosing a module.

IV. Routing

Fig. 6 illustrates the routing of a net. The vertical segment connected to the driving module's output is connected by cross fuses to horizontal segments, which in turn connect to the segments associated with module inputs. In the top channel, a horizontal fuse is used to link two segments into a longer one.

The resistance of the blown fuses and the parasitic capacitance of the segments used form an RC tree, with the driver of the net as the root. Note that each input is driven through a maximum of three and generally two fuses to limit the delay. (If the number of series stages in the RC tree were allowed to increase further, the delay through the routing would increase rapidly.) The maximum number of fuses and the segment lengths (hence capacitances) can be altered to suit the chip dimensions and the resistance of the fuse technology.

In rare instances, it is not possible to place the macros so that all inputs on the net lie within the channels spanned by the output segment of the driving module. To handle this case, a few additional uncommitted long vertical segments are provided. The net is then routed from the output segment to a horizontal segment, then to the long vertical segment, then to another horizontal segment, and finally to the necessary input segments. To keep the number of fuses in series limited to four, no horizontal fuses are allowed in such nets. (If necessary, the architecture can be extended to provide a special fuse connecting the output directly to a long vertical segment passing over the driving module, thus eliminating the first horizontal segment and reducing the total number of fuses in series back to three.)

A means must also be provided to connect internal signals to the bonding pads of the chip. Each pad has a dedicated bidirectional buffer, which connects to the array through an associated I/O module. The I/O modules fit in the outer columns and rows of the array next to the logic modules. Each I/O module has two inputs, data and enable, and an output. The data and enable signals are

sent to the output buffer of the associated bonding pad, and the module's output comes from the input buffer of the pad. Thus the I/O module can be configured to provide input, output, tristate, or bidirectional capability.

To minimize clock skew due to differential routing delay, one entire track (or more if needed) in each channel is set aside for clock distribution. These tracks are connected directly to buffers, so that each input presents a similar load driven through exactly one fuse.

An interesting theoretical question is whether more horizontal tracks are needed in each channel here (where the lengths of the wiring segments must be predetermined) than in mask-programmed routing (where the wiring is customized for the design). Surprisingly, a high probability of routability is obtained with only a few tracks above channel density.

This requires a careful choice of the lengths of the segments, based on statistics from an extensive suite of design examples. This was done by first determining the distribution of net lengths, i.e., the length each net would run along each channel if the constraint of fixed segmentation were absent (as in a conventional gate array). The distribution of physical segment lengths provided on the chip was chosen to obey similar statistics. Then the segmentation was "tuned" manually based on actual routings which obeyed the constraints it imposed.

To obtain good routing performance it is also necessary to take advantage of the symmetry of the macros where possible. For example, observe that if macro 4 in Fig. 6 permits its input to be routed from either the upper or lower channel, there is a better chance of finding a free horizontal segment to connect it.

V. Testing

To assure high programming yield, it is necessary to thoroughly test the chip for defects in the modules and fuses prior to programming. With a simple addition, the addressing circuitry used for programming suffices for this purpose as well.

Continuity of the tracks is easily verified by turning on all vertical and horizontal pass transistors, and using the peripheral circuits to drive the tracks from one end and read them back from the other. Testing for the absence of shorts between adjacent tracks is done in a similar way by applying a pattern of alternating ZERO's and ONE's.

Shorted or weak cross fuses are detected by turning on all horizontal and vertical pass-transistor lines, grounding all horizontal segments, and driving all vertical segments to some stress voltage. Horizontal fuses are tested column by column, with the same addressing method that is used to program them.

To verify the functional operation of the modules, we need to apply test vectors to their inputs and read their outputs. A vector is applied simultaneously to an entire row of modules by turning on all vertical pass transistors except those in the row being tested. Data are applied to

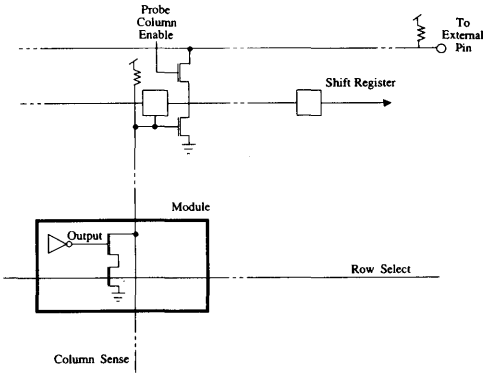

Fig. 7. Probe circuit.

the inputs in the channel above the row from the periphery at the top of the array, and to the inputs in the channel below the row from the bottom of the array.

Since the outputs of the modules share a vertical track with outputs of other modules above and below them, some other means is required to read the module outputs at the array periphery. As shown in Fig. 7, a select line is provided along each row of modules, and a sense line along each column. Activating the select line for the row of modules under test gates their output values onto the sense lines. The sense lines are loaded into a shift register at the top of the array.

This ability to read the output of any module at the array periphery is highly useful *after* programming as well. Only a small amount of extra circuitry is required to select one of the sense lines and make its value available at an external pin of the chip. Thus by shifting in the appropriate address, the user can observe any internal node of his design externally in real time. This virtual probe can be used and its address changed even as the programmed chip is operating in the user's system.

VI. Implementation: Silicon and Software

The architecture has been implemented in a CMOS device. For details, including the speed of the module in isolation and in an application, see [5].

Computer-aided design tools have been developed to support the architecture. Designs are entered as schematics or net lists using a cell library.

The placement and routing algorithms are specific to the architecture. As usual these are time consuming, taking up to a few hours on a low-cost workstation. They achieve 100-percent routing completion. (Even expert users have never been able to improve manually on the automatic router.) The probability of successful routing can be predicted by analyzing some statistics of the design.

Because the nets are *RC* trees, delays are not a simple function of capacitive load as with mask-programmed gate

arrays. Nevertheless, we are able to quickly calculate precise delays at each input for post-layout simulation and timing verification.

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DIELECTRIC BASED ANTIFUSE FOR LOGIC AND MEMORY ICS

by Esmat Hamdy, John McCollum, Shih-ou Chen,
Steve Chiang, Shafy Eltoukhy, Jim Chang,
Ted Speers, Amr Mohsen

A paper presented at the
International Electron Devices Meeting, 1988

DIELECTRIC BASED ANTIFUSE FOR LOGIC AND MEMORY ICs.

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Shafy Eltoukhy, Jim Chang, Ted Speers, Amr Mohsen

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ABSTRACT

This paper describes a *P*rogrammable *L*ow *I*mpedance *C*ircuit *E*lement (PLICE), which is a dielectric based antifuse for use in both logic and memory ICs. The antifuse element offers significant size and performance improvement compared to other programmable cells. A simple thermal model has been developed to predict the antifuse resistance. Each antifuse occupies an area of 1.5 um^2 using 1.2um technology. It can be programmed within 1 msec, and has a tight resistance distribution centered around 500 ohms. The reliability of both the programmed and unprogrammed states is demonstrated to be better than 40 years. The antifuse was used in the design of the first family of desktop-configurable channeled gate arrays and a 64K PROM device.

INTRODUCTION

PROMs and programmable logic devices commonly employ programmable elements such as fusible links, EPROM or EEPROM cells. These programmable elements are either large in area, require high programming current, or are three terminal devices. This paper describes a Programmable Low Impedance Circuit Element (PLICE), which is a dielectric based antifuse that offers significant size and performance improvements over other programmable elements. The antifuse structure, technology, characteristics, thermal model and reliability are described below.

ANTIFUSE STRUCTURE AND TECHNOLOGY

The PLICE antifuse is a dielectric between an n+ diffusion and poly-Si as shown in the SEM cross-section (Fig. (1)) and is compatible with CMOS and other technologies such as bipolar and BIMOS. The PLICE element was integrated in a standard 12 mask, double layer metal twin tub CMOS technology. Three additional masks were required; n+ antifuse diffusion, antifuse poly, and 40 nm oxide mask for the high voltage transistors, bringing the total to 15 masks. Four transistor types (TABLE 1) are used; the low voltage high speed transistors are used for the logic and signal path while the high voltage transistors are used for the programming path. Fig. (2) is a photomicrograph of a 2000 gate programmable gate array utilizing 186,000 antifuses. There are roughly one hundred antifuses for each logic gate to achieve a high degree of interconnectivity and gate utilization. Each antifuse occupies an area equivalent to a contact or via. The antifuses are incorporated into a cell structure such that when the antifuse is programmed, it connects a metal 1 and metal 2 line [1,2]. The cell structure size is thus limited by the metal 1 and metal 2 pitch. Fig. (3) is a photomicrograph of a 64K PROM designed using the same technology with a typical access time of 35 nsec.

ANTIFUSE CHARACTERISTICS

When 18 volts is applied across the antifuse through X-Y select transistors [1,2], the antifuse is programmed to the conductive state in about 200 usec as shown in Fig. (4). Fig. (5) shows a tight resistance distribution of antifuses programmed with a current of 5 mA.

ANTIFUSE THERMAL MODEL

Once the dielectric is ruptured, the resistance R_l of the conductive state is determined by the size of the conductive conduit (link). The size of the link is determined by the amount of power dissipated in the link which melts the dielectric. Since the temperature of the molten core varies inversely with its radius, the molten core will expand until its temperature drops below the melting point of the dielectric. Since the size of the link is much smaller than the thickness of the conductive silicon layers on both sides of the dielectric, the temperature gradient and the resultant heat conduction can be modelled by a simple sphere. The resultant equation for the link temperature T_l:

$$T_l = I_p V_l / 4\pi k_{th} r_l \quad \ldots\ldots\ldots\ldots (1)$$

Where I_p is the programming current, V_l is the voltage across the link, r_l is the radius of the link, and k_{th} is the thermal conductivity of silicon. The calculation however becomes

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complicated if the thermal conductivity of silicon is taken into consideration as a function of its temperature [3]. Furthermore, the power dissipation is distributed throughout the sphere. Hence a computer simulation that breaks the sphere into 1 nm thick conductive shells was used to calculate the link temperature T_l and resistance R_l vs programming current I_p. The resultant calculations are plotted in Fig. (6). The link radius r_l is determined by the equilibrium of power dissipation and melting temperature, as expressed in the following equation [4]:

$$r_l = 2I_p(\sqrt{\rho_l + \rho_{si}/2})/87\pi \quad \ldots\ldots\ldots (2)$$

where ρ_l, ρ_{si} are the resistivities of the link and silicon respectively during programming and the relation between link resistance R_l and link radius r_l can be obtained as follows[4]:

$$R_l = (\rho_l + \rho_{si})/\pi r_l \quad \ldots\ldots\ldots\ldots\ldots (3)$$

From eqn.(2) and eqn.(3) we derive that R_l is thus inversely proportional to I_p (Fig. (6)), given by the following equation:

$$R_l = (87/2I_p) * (\rho_l + \rho_{si})/\sqrt{\rho_l + \rho_{si}/2} \quad \ldots (4)$$

This can be further simplified to:

$$R_l = 2.5/I_p \quad \ldots\ldots\ldots\ldots\ldots\ldots (5)$$

At 5 mA, for example, the link radius is about 20 nm and the fuse resistance is 500 ohms - (approximately the impedance of a 20um wide EPROM cell) in its conductive state. The programmed antifuse resistance is a function of the reading current as shown in Fig. (7). The resistance rises at a current just before the programming current, due to heating of the conductive channel; drops when the silicon in the conductive channel melts; and continues to decrease beyond the original resistance as the current exceeds the programming current. This is due to the permanent widening of the conductive link.

ANTIFUSE RELIABILITY

Programmed antifuse reliability was evaluated using discrete antifuses incorporated in a Kelvin structure (Fig. (8)). The structures were stressed with a 5 mA current between two of the terminals 1, 2 at a temperature of 250C. Fig. (9) is a plot of the monitored voltage across the programmed antifuse as a function of stress time. Failure is indicated by an increase in voltage as the structure becomes open. Measurement of the antifuse through the other two terminals 3, 4 indicated that the programmed antifuse did not fail or exhibit any measurable resistance change. Investigation of the failure using SEM indicated that the failure is due to poly contact electromigration. With 0.9 eV activation energy [5] for contacts, the predicted lifetime is more than 40 years. Fig. (10) is a plot of time to breakdown vs 1/electric-field for unprogrammed discrete antifuses. Extrapolation of Fig. (10) indicates that the lifetime of an unprogrammed antifuse under continuous 5.5v stress exceeds 100 years, with a failure rate less than 1 FIT. In addition to the accelerated discrete antifuse device reliability data, 384 product units have accumulated a total of 571,000 device hours of dynamic burn-in at 5.5 volt and 125C (with some units reaching 2500 hours) with no failures or change in a.c. characteristics. This is equivalent to a failure rate of less than 100 FIT.

SUMMARY

In summary we have presented and modelled a reliable high performance dielectric based antifuse which can be programmed with relatively low current and is compatible with CMOS and other technologies. The cell read current, 2 mA at 1 volt, is an order of magnitude higher than that of an EPROM of comparable size. There is no data (charge) retention concern. The unique combination of small size and low resistance has enabled the development of the first family of desktop-configurable channeled gate arrays and a 64K PROM device.

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4) to be published

5) ACCELERATED TESTING HANDBOOK, Technology Associates ,D. S. Pech and O. D. Trapp , 1987, p. 5.36-37

TABLE 1
TECHNOLOGY OVERVIEW

PROCESS:TWIN TUB DOUBLE LAYER METAL
CMOS 15 MASKS

TRANSISTOR	OXIDE	LEFF	VOLT
N LOW VOLT	25 nm	1.1 um	5 V
P LOW VOLT	25 nm	1.2 um	5 V
N HIGH VOLT	40 nm	1.5 um	20 V
P HIGH VOLT	40 nm	1.8 um	20 V

ANTIFUSE CHRACTERISTICS:

PROGRAMMING VOLTAGE	18 V
PROGRAMMING TIME	< 1 mS
PROGRAMMING CURRENT	< 10 mA
ON RESISTANCE	< 1K OHMS
OFF RESISTANCE	> 100M OHMS

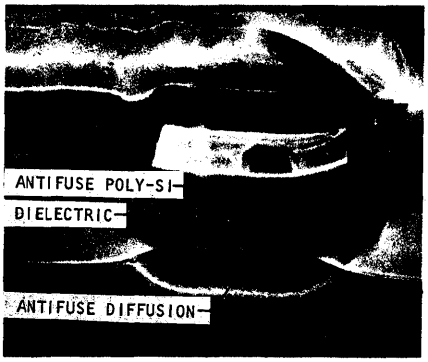

Fig.(1) SEM cross-section of antifuse.

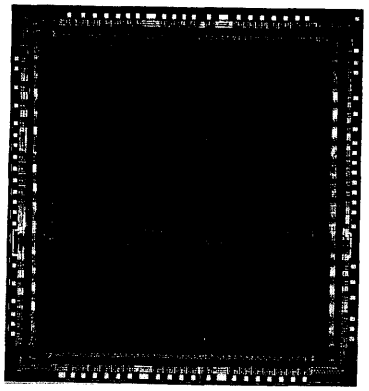

Fig.(2) Photomicrograph of 2000 gate programmable gate array.

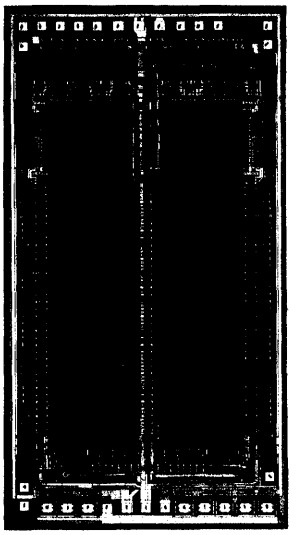

Fig.(3) Photomicrograph of 64K PROM

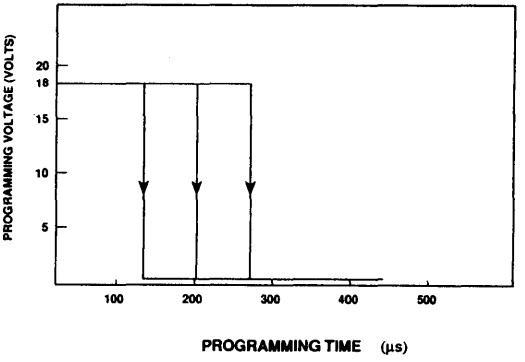

Fig.(4) Programming time of antifuse with 18V programming voltage.

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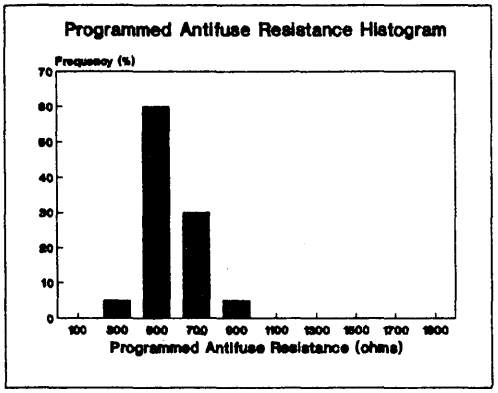

Fig.(5) Programmed antifuse resistance histogram, programmed with 5 mA current.

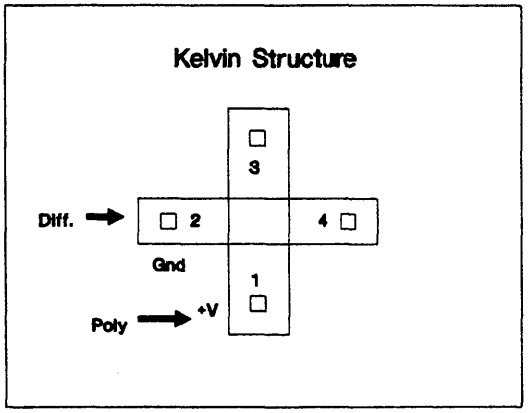

Fig.(8) Antifuse Kelvin structure.

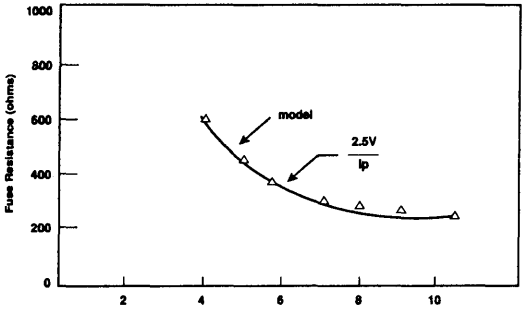

Fig.(6) Programmed antifuse resistance versus programming current.

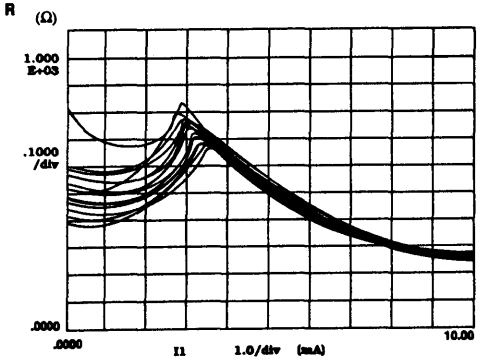

Fig.(7) Programmed antifuse resistance versus reading current, with 100 ohms of parasitic resistance in series.

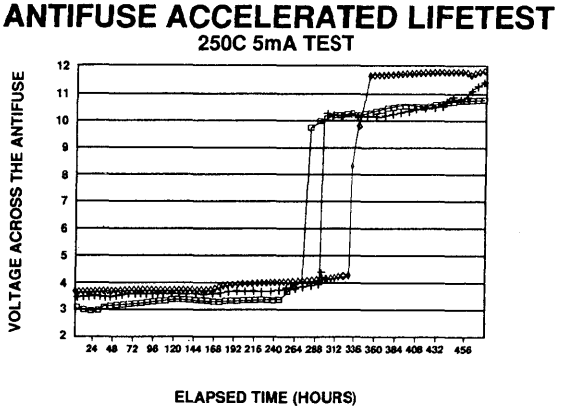

Fig.(9) Voltage across antifuse versus stress time, with 5 mA stress current.

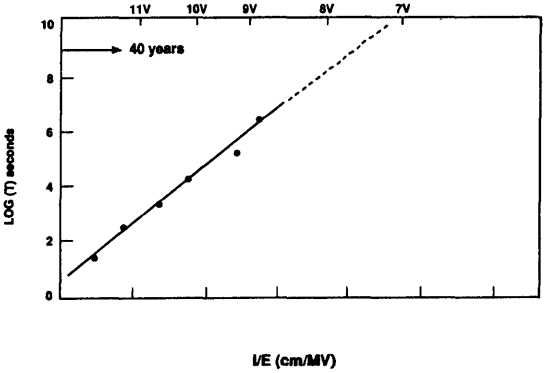

Fig.(10) Time to breakdown versus inverse electric field.

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OXIDE-NITRIDE-OXIDE ANTIFUSE RELIABILITY

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Oxide-Nitride-Oxide Antifuse Reliability

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Abstract

Compact, low-resistance oxide-nitride-oxide antifuses are studied for TDDB, program disturb, programmed antifuse resistance stability, and effective screen. ONO antifuse is superior to oxide antifuse. No ONO antifuse failures were observed in 1.8 million accelerated burn-in device-hours accumulated on 1108 product units. This is in agreement with the 1/E field acceleration model.

Introduction

Field programmable gate arrays has been a fast growing field only recently [1]. The key to their configurability is the development of a programmable interconnect element. This element should have small area, low post programming resistance, and be reliable. Many known interconnect elements have been used, including SRAMs, EPROMs, and EEPROMs. Problems encountered using these elements are: large area, high resistance, or inefficient utilization due to circuit complexity. The antifuse approach, however, has some unique and attractive features. Since it is only a two terminal device, the area required is small, and the simple two terminal resistor structure allows simple and efficient routing schemes [2]. The programmed antifuse has very low resistance. It was found that oxide-nitride-oxide (ONO) antifuses have a lower and tighter resistance distribution than that of oxide antifuses (Fig. 1). The choice of antifuse material has further improved both the yield and the reliability over that of oxide antifuses. In addition, ONO is highly radiation resistant. Initial evaluation results indicate that products containing ONO antifuses can withstand 1.5 million rads [3]. The technology and performance characteristics of the ONO antifuse has been previously described [4]. In this paper, we will report the reliability characterization of the ONO antifuse.

We will discuss three different types of antifuse reliability. The first is that the unprogrammed antifuse has to survive a 5.5V 40 year operating condition. The second is that during programming, all unprogrammed antifuses are subject to a momentary stress of half the programming voltage (Vpp/2). The programming yield is required to match or exceed PAL yields which are in excess of 99%. The third is that programmed antifuses should have a very low resistance, which will not increase in value over the life of the part. As will be shown below, the unprogrammed antifuse is reliable, well in excess of the 40 year lifespan, the programming yield is excellent, and the programmed antifuse is not subject to any measurable electromigration. The weakest link in the technology is not the antifuse, but typical CMOS process limitations.

Antifuse Structure

The ONO antifuse is sandwiched between N+ diffusion and N+ poly-silicon gate to form a very dense array with density limited by metal pitches (Fig. 2). A thin layer of oxide is thermally grown on top of the N+ surface, followed by LPCVD nitride, and the reoxidized top oxide. The target electrical thickness of the combined layer is equivalent to 9nm of silicon dioxide.

TDDB of Unprogrammed Antifuses at 5.5V

For the sub 10 nm ONO thickness, time-dependent-dielectic-breakdown (TDDB) reliability over 40 years is an important consideration. The very first task in determining the feasibility of the antifuse was to examine its TDDB reliability. Typical electrical field and temperature accelerated tests were done in order to extrapolate the dielectric lifetime under normal operating conditions. Based on the oxide study [5], it was reported that there may be different field dependencies of lifetime in high field (>6MV/cm) and in low field (<5MV/cm) regimes. In the case of ONO antifuses, the 5.5V operating field is already over 6MV/cm. The extrapolated data from the high field regime was therefore assumed accurate. This assumption was later confirmed with device burn-in data.

Field Acceleration (E vs 1/E model for ONO)

200X200 um^2 ($0.04mm^2$) area capacitors were packaged and then stressed at different voltages. ONO thickness ranging from 8nm to 9.5nm were studied. The test splits and sample sizes are summarized in Table 1. The TDDB distribution at each voltage condition is shown in Fig. 3.

In the literature, the oxide intrinsic lifetime has been observed to have an exp(1/E) dependence, which is explained mainly with the Fowler-Nordheim tunneling mechanism [6]. Oxide Log(I) curves and lifetime $Log(t_{50})$ curves exhibit a linear function of 1/E behavior. On the other hand, nitride Log(I) has been shown to follow the Frenkel Poole behavior ($\sqrt{E}$) [7]. Log(I) of ONO is not a linear function of 1/E (Fig. 4a). Rather, it more closely follows E

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(Fig. 4b). Also, several studies have fitted lifetime of ONO to an E model [8,9].

Nevertheless a careful examination of our data revealed that TDDB lifetime of ONO follows the 1/E model (Fig. 5) better than the E model (Fig. 6). This is in agreement with conclusions from one study [10], but in contradiction with others which did not examine the fit between data and the 1/E model [8,9]. Based on our observation, we found that the E model can fit the data well over 4 to 5 orders of magnitude of time span. However, as time span increases to 7 orders of magnitude, the E model is clearly inadequate (Fig. 6).

Since there is no theoretical basis for ONO to follow the 1/E model or the E model, we tried a statistical approach to find out which model can best fit the data. First, the data is fitted to different field dependent models of $\exp(E^n)$ with n ranging from -1.5 to 1 at 0.5 intervals. Then the correlation coefficient is compared for different models in Fig. 7. The residual comparison is shown in Fig. 8. Again, the E model (n=1) turns out not to be a good fit for the data. The best fit appears to be n = -.5 or -1. This seems to suggest that ONO behavior is similar to oxide (n = -1). But, the addition of nitride (n=0.5) has changed the n to between -0.5 to -1. Which of the two exponents, n=-0.5 or -1, should be used may depend on the ONO processing conditions. The difference between extrapolated lifetime based on these two models is not nearly as dramatic as the choice between E and 1/E. At 5.5V, the difference in the extrapolated lifetime between n= -0.5 and -1 is one order of magnitude in time. On the other hand, the difference between n=1 and -1 is 5 orders of magnitude. In the subsequent analysis, we will use 1/E model exclusively for simplicity. The conclusion reached will not change much if the $1/\sqrt{E}$ model were to be used.

Besides the 0.04mm^2 area capacitor data, we also did a TDDB study on single antifuses (3.2um^2) and ACT 1010 product antifuse arrays (0.36mm^2). Results are shown in Fig. 9. Again, the data follows the 1/E model well for all different area sizes.

Temperature Acceleration

The temperature effect on the 0.04mm^2 ONO area capacitor lifetime is shown in Fig. 10. The activation energy as a function of the electrical field is shown in Fig. 11. A field dependent activation energy has been reported for oxide TDDB lifetime, as well.

For the 5.5 volt lifetime estimate, the activation energy is close to 0.9eV (1/E model). Using this estimate and the product TDDB defect distribution (Fig. 12), the 1% failure lifetime at 5.5V is well over 40 years. The projected product antifuse failure rate (containing 100K to 200K antifuses) is less than 50 FITS at 125°C.

Program Disturb and Screen

During programming, all antifuse electrodes are precharged at a given voltage, Vpre. To program the antifuse, its poly-silicon electrode is raised to Vpp while its N+ diffusion is grounded. The unselected antifuses are subjected to the stress of either Vpre to ground or Vpp to Vpre for an average of 100 times the single antifuse programing time. Usually the Vpre is set such that stress is approximately Vpp/2. If defective unselected antifuses fail (become programmed) due to this stress, they will show up as programming failures. These defective antifuses can be screened out at wafer sort by a 1 second stress at 10 volts (10V/1s). This screen is done twice during sort. The first 10v/1s (FS-1) screens out the defective dielectric distribution. The second 10V/1s stress (FS-2) simulates the percent yield loss during programming. In Fig. 13, it shows a typical wafer trend on the failure rate of both first and second stress. The 10 run average of FS-2 is 0.3 %. This suggests that the programming failure loss due to antifuse defects after the screen should be less than 0.3%.

Unlike floating gate EPROMs and EEPROMs, latent ONO defects can be easily screened out with a voltage stress as described above. This is one more advantage of the antifuse structure as a programming element. Once an antifuse has passed the voltage screen at sort, it is very reliable. Based on either 1/E or $1/\sqrt{E}$ model, the 10V/1s stress is equivalent to a stress time at 5.5V well over 40 years. We have calculated the equivalent product failure rate at 5.5V as a function of the FS-2 screen yield loss. It shows that for an FS-2 of 0.5%, the equivalent FITs at 5.5V 125°C is less than 50, which is consistent with the results mentioned at the end of the previous section.

Programmed Antifuse Reliability

Once the antifuse is programmed and forms a low resistance path, the resistance should remain low. In the case of oxide, it is a known fact that they are susceptible to self healing [11] or an increase in resistance with time. This is not the case for ONO as will be shown in the following section.

A four terminal Kelvin structure was used for the reliability study (Fig. 14). A constant 5mA current, which is much larger than the operating current, was passed through the antifuse at 250°C (through terminals A,B) while the voltage across the antifuse was monitored between terminals A and B. A typical voltage vs time graph is shown in Fig. 15. A sudden increase in voltage indicates that an open circuit has formed. Prior to that, there is no significant change in the voltage across the antifuse indicating that the resistance remained low.

Next, electric continuity measurement and scanning electron microscopy (SEM) were done on the Kelvin structure. It was found that

the antifuse resistance still remained low when measured from the other two unstressed terminals C and D. This is the case for all samples tested under this condition. SEM analysis showed that the open circuit was related to the metal to poly contact electromigration failure (Fig. 16). The activation energy (based on 250°C and 200°C data) for the contact electromigration is 1.1eV, which is in agreement with typical values obtained from contact electromigration failures [12]. The extrapolated lifetime of contacts in these circuits under normal operating conditions is well in excess of 40 years. The real lifetime of a programmed antifuse itself is yet to be determined.

High Temperature Product Burn-in Life Data

In previous sections, it was demonstrated that the extrapolated ONO antifuse lifetime follows the 1/E model instead of the E model. Product burn-in data supports this conclusion. 1108 units (including PROMs, ACT1010, and ACT1020) containing an average of about 100K antifuses per unit, about 5% of which were programmed, underwent dynamic burn-in at 125°C and 5.5V with roughly an accumulated 1.8 million device hours. No antifuse failure has been observed while two CMOS circuit failures have been observed and identified in the peripheral circuitry. This data is consistent with the failure rate projection based on 1/E extrapolation, while the E model extrapolation based on TDDB test data would have projected 90 unit failures (out of 1108 units) due to ONO antifuses.

Conclusions

We have investigated three reliability aspects of the ONO antifuses. During operation, the lifetime of the ONO antifuse is well in excess of 40 years at elevated temperatures. It has been further demonstrated that the E model is not adequate for lifetime extrapolation. Results indicate that 1/E is a better choice. The key to successful extrapolation is that data should span over seven orders of magnitude in time. Based on the 1/E model, the extrapolated lifetime is well over 40 years at 5.5V. To screen out the programming yield loss due to breakdowns of defective unselected antifuses, a screen was developed. This is not a yield limiting factor in the typical process as the yield loss due to the screen on the average is 1%. After the screen, the programming yield is higher than 99%. The reliability of programmed ONO antifuses was also studied. It was found that the lifetime is limited by the contact electromigration, not by the ONO antifuse. In addition, the resistance remains low throughout the test indicating the antifuse resistance does not increase. Finally, more than 1100 product units and over 1.8 million unit hours of burn-in data have shown no failure at all that can be attributed to the ONO antifuses. This is in agreement with the prediction based on wafer-level tests and the 1/E model.

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Table 1 Field accelerated test data for two lots with thickness ranging from 8nm to 9.5nm. The test was done on 0.04mm2 area capacitor.

Lot A					Lot B				
Voltage (V)	Tox (nm)	E-field (MV/cm)	# of cap	t_{50} (sec)	Voltage (V)	Tox (nm)	E-field (MV/cm)	# of cap.	t_{50} (sec)
13.5	8.3	16.2	22	4.2e-3	14.0	8.7	15.9	25	9.8e-3
12.5	8.3	15.1	22	3.7e-2	13.0	8.7	14.9	25	5.0e-2
12.0	8.3	14.4	22	1.5e-1	12.5	8.7	14.3	25	2.4e-1
11.5	8.3	13.8	22	8.6e-1	12.0	8.7	13.7	25	1.3e0
11.0	8.4	13.1	22	4.7e0	11.4	8.7	13.1	25	9.0e0
10.5	8.4	12.5	9	5.8e1	11.2	8.7	12.5	45	8.0e1
10.0	8.3	12.0	6	3.2e2	10.8	9.0	12.0	45	3.52e2
9.5	8.3	11.4	6	2.5e3	10.2	9.0	11.3	45	2.88e3
9.0	8.3	10.7	36	2.5e4	9.7	9.0	10.8	45	2.07e4
8.5	8.3	10.2	15	2.3e5	9.0	8.7	10.3	32	3.35e5
8.0	8.3	9.6	59	1.5e6	9.0	9.3	9.7	32	2.22e6
Sub-total of tested cap.			241					401	
Total of tested cap.			642						

Table 2 High temperature operating life test data (HTOL).

Device	# of units	# of fuse per unit	Device Hours @ 125°C/5.5V*	# fuse Fail	Equivalent Device Hours @ 55°C
PROM64	275	65,536	450,000	0	18.8 Million
1003JLCC	238	40,000	359,400	0	15.0
1010JLCC	144	112,000	283,000	0	11.8
1020JLCC	61	186,000	90,000	0	3.8
1010PLCC	358	112,000	616,000	0	25.8
1020PLCC	32	186,000	5,300	0	0.2
Total	1108	701,536	1,804,100	0	75.5 Million

* All PLCC, 114/144 of 1010 JLCC and 32/61 of 1020 JLCC have 5.75V.

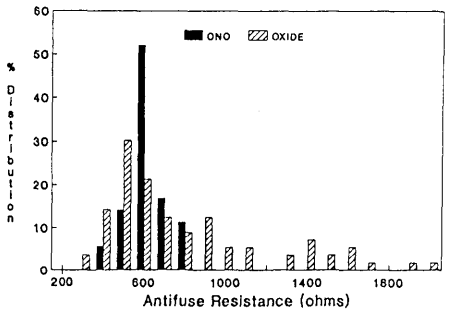


Fig. 1 ONO antifuse has a tighter resistance distribution than oxide antifuse.

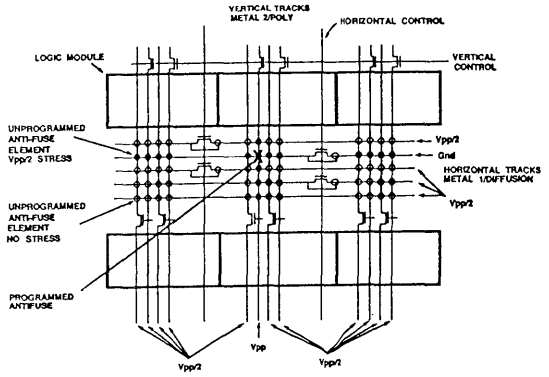


Fig. 2 Simplified product architecture showing logic modules, routing tracks, and antifuse arrays. Vpp is applied to program a selected antifuse. Unselected antifuses have Vpp/2 or 0V stress.

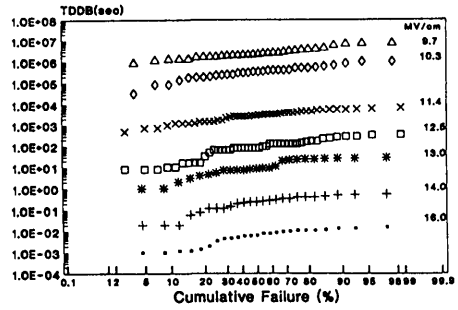


Fig. 3 Cumulative percentage failure verses time on a log-normal scale.

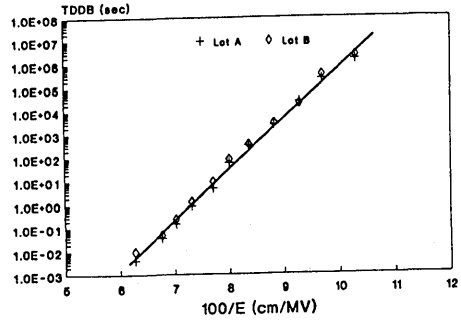
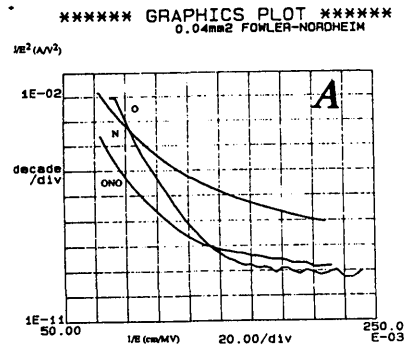


Fig. 5 Log t_{50} vs 1/E for two lots. 0.04mm^2 area capacitor was used.



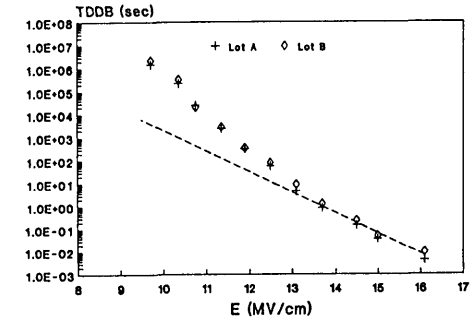


Fig. 6 Log t_{50} vs E for two lots. Log t_{10} has a similar E dependence.

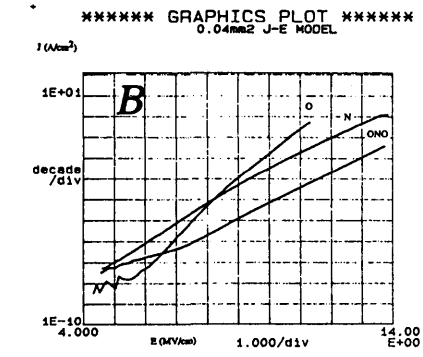


Fig. 4 I-V characteristics of oxide, nitride, and ONO. (a) Fowler-Nordheim tunneling plot. (b) J vs E plot. Log(J) of ONO is not a linear function of 1/E I-V.

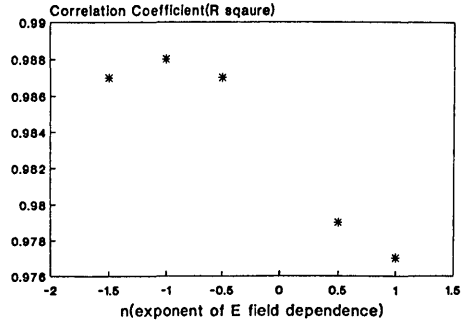


Fig. 7 t_{50} was fitted to 5 different distributions. The fitting correlation coefficient (R^2) is plotted against the field exponent n in [exp(E^n)]. 1/E(n= -1) has the best fit with the largest correlation coefficient.

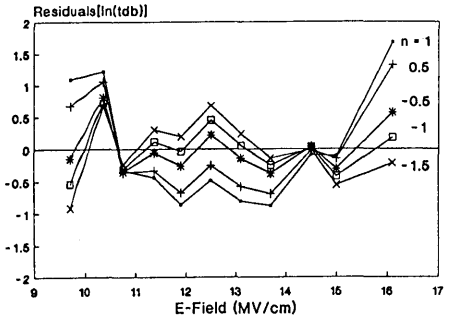


Fig. 8 Residuals at each data point are plotted for 5 different n's. E field dependence has the largest residuals. 1/E and $1/\sqrt{E}$ have the smallest residuals

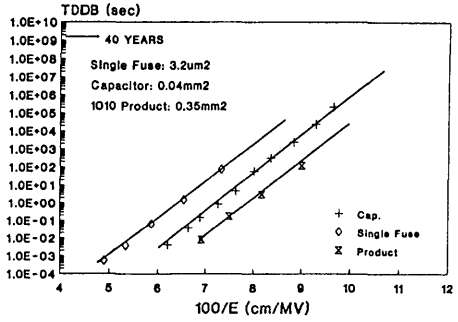


Fig. 9 Log t_{50} can be fit as a linear function of 1/E with the same slope for three different structures: single fuse ($3.2um^2$), area capacitor ($0.04mm^2$), and product array ($0.35mm^2$).

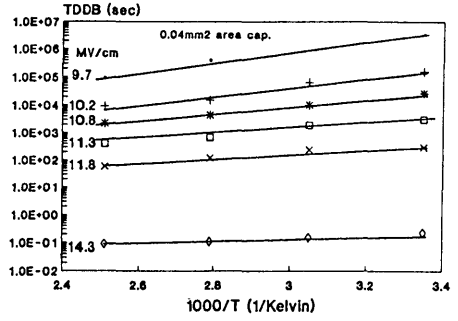


Fig. 10. Field effect on t_{50} at different temperatures ranging from 25°C to 150°C.

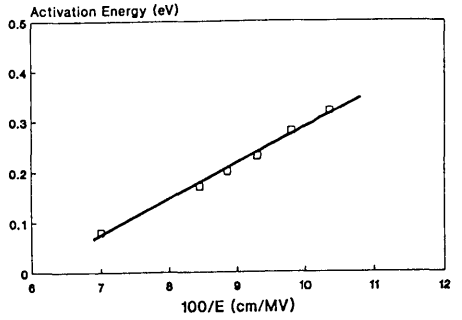


Fig. 11. Field dependence of ONO activation energy.

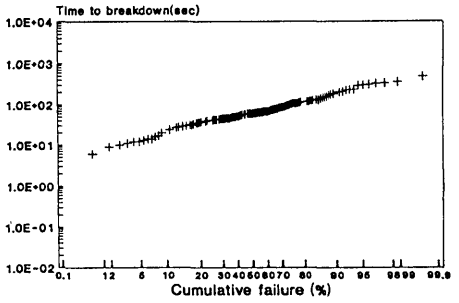


Fig. 12. Cumulative percentage failure of product antifuse array ($0.35mm^2$) vs breakdown time at 11V stress.

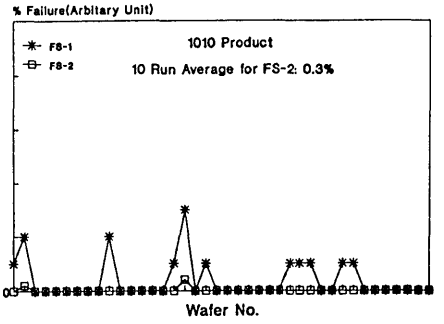


Fig. 13 A typical wafer sort yield loss plot for one lot. After the screen, the 10 run average yield loss is less than 0.3%. Since the screen is more severe than 5.5V/40 years, the product will be very reliable throughout the operating lifetime.

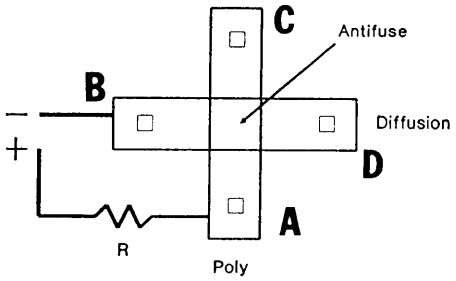


Fig. 14 A four terminal Kelvin structure is used for programmed antifuse reliability test. When an open failure is detected through two stressed terminals, A and B, the antifuse resistance remains low as measured through two unstressed terminals, C and D.

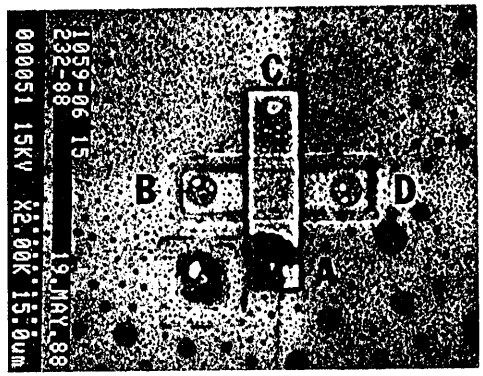


Fig. 16 SEM photograph of the Kelvin structure after showing an open circuit. The open is identified to be at poly to metal contact due to contact electromigration.

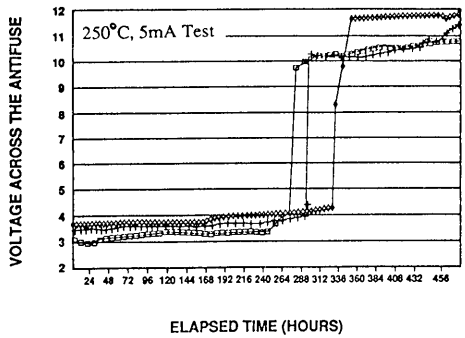


Fig. 15 Voltage across antifuse versus stress time, with 5mA current. Antifuse resistances remains little changed prior to contact failure.

Actel

Article Reprint 10

AN FPGA FAMILY OPTIMIZED FOR HIGH DENSITIES AND REDUCED ROUTING DELAY

by Mike Ahrens, Abbas El Gamal, Doug Galbraith,
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An FPGA Family Optimized for High Densities and Reduced Routing Delay

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ABSTRACT: The Act-2 family of CMOS Field-Programmable Gate Arrays uses an electrically programmable "antifuse" and new architectural and circuit features to obtain higher logic densities while increasing speed and routability. Improvements include: two new logic modules, novel IO and clock driver circuitry, and more flexible and faster routing paths. New addressing circuitry shortens programming time and speeds complete testing for shorts, opens and stuck-at faults. Fully automatic placement and complete routing are retained. Special software tools used for architectural exploration and layout generation are noted.

1. Introduction.

Previous papers described an architecture for field-programmable gate arrays (FPGAs) [1], and its implementation in the Act-1 FPGA circuits [2]. These demonstrate that user programmability can be obtained without sacrificing the application flexibility of a channeled gate array architecture.

This paper describes new architectural features, circuit techniques and software that approximately double system speeds, and are capable of extending the architecture to logic densities of 8,000 gates in 1.2 micron technology and to approximately 16,000 gates for 0.8 micron. (Note that these gate counts are based on the capacity of an equivalent mask-programmed gate array. Other measures would yield higher values.) The circuits employ a one-time electrically programmable "antifuse" offering small area and capacitance, and low resistance once programmed [3].

As before, the architecture consists of rows of logic modules separated by horizontal channels. This organization is similar to that of a channeled gate array, except that instead of an area for custom metallization the channels contain wiring segments of various lengths which can be connected by antifuses.

A key goal was to insure complete automatic placement and routing with acceptable routing delays. This is facilitated by the inherent flexibility of the channeled architecture and the integration of large numbers of antifuses (700,000 or more) on a single chip.

2. Logic Module

The choice of the logic module is critical to an FPGA architecture. The module must be simple enough to permit a compact and high-speed circuit layout. Yet it must also be flexible enough to accommodate the most frequently used logic functions (macros) with several choices of routing. Our approach is to evaluate many candidate modules against macro usage statistics from actual applications. (The philosophy is similar to that used to define the instruction set of a RISC microprocessor. It has also recently been applied to BiCMOS gate arrays [4].) To assist in this task, a program has been developed that can enumerate all macros accommodated by a given module in minutes [5].

The Act-1 family uses one general-purpose module, which implements all combinational functions of 2 inputs, many of 3 or 4 inputs, and others ranging up to 8 inputs [1]. Any sequential macro can be configured from one or more modules using appropriate feedback routings.

At higher logic densities, the law of averages makes designs begin to adhere more closely to typical macro usage statistics (see, e.g., [4]). This motivates the use of a mix of two new modules, each of which is most efficient for a different set of macros. The "C-module" is a modified version of the Act-1 module reoptimized to better accommodate high-fan-in combinational macros, e.g. wider AND gates, though with some loss in ability to accommodate sequential functions. The S-module, on the other hand, is optimized for configuring sequential macros. It can accommodate a latch or flip-flop and/or many combinational macros of one to seven inputs. Both transparent-high and -low latches and rising- and falling-edge-triggered flip-flops are possible.

The two-module scheme can reduce the number of modules required for a block of logic by up to a factor of 3. On average, logic density per module is increased by over 50%. Furthermore, because the density is increased, the number of routed nets in a typical critical path is reduced. This significantly improves speed. Fig. 1 shows how a typical critical path in a state machine can be implemented to take advantage of the wide fan-in of the C-module, and the capabilities of the S-module. The delay paths include only two routed nets. Performance data is summarized in Table 1.

Since the fan-in of each module is no larger than that of a typical gate-array macro, the two-module scheme maintains

the generality of a "fine-grained" architecture. Significantly larger and more specialized modules would risk a sharp loss of efficiency for applications that deviate from typical usage statistics. Using a larger module, or more types of modules, also adds constraints to the placement and routing problem, making automatic solution more difficult and ultimately increasing net delay.

3. Input/Output

Of particular importance to system performance is the delay between the time a clock signal changes at an input pad and when data appears on an output pad, referred to as T_{clk-Q}. (Memory bus interface applications are a good example). The goal is to gain maximum speed without sacrificing flexibility.

This is accomplished by providing a dedicated transparent-high latch in each output path. If desired, the dedicated latch can be combined with a transparent-low latch configured from a logic module to form a rising edge-triggered flip-flop. (Note that the net connecting the two latches is not in the critical path, so T_{clk-Q} is not increased relative to having a dedicated flip-flop in each IO.) If flow-through operation is desired, the output latch gate is simply tied off to make the latch transparent.

To limit set-up time requirements, a dedicated transparent-low latch is provided on each input path. The polarities of the input and output latches are chosen so they can be combined with each other, and possibly with other internal latches or flip-flops, to form a path that is functionally equivalent to a chain of rising-edge flip-flops. (See Fig. 2.).

Chips with many simultaneously switching outputs require some form of slew rate control to avoid noise problems; several alternatives are possible. Sequencing the operation of several parallel drivers limits the slope of the current ramp when driving a passive load, but large di/dt can occur in bus contention situations when the contending driver suddenly shuts off. Feedback remedies this problem, but can still allow large di/dt in asynchronous systems where the logic state changes before a transition is complete. Instead a current mirror circuit was used to limit the drive current.

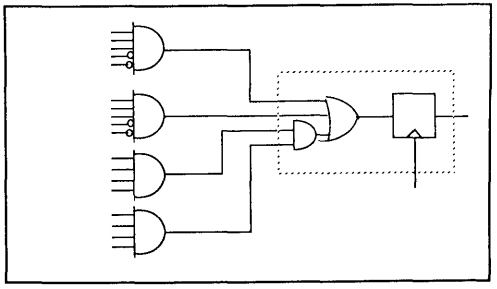

Figure 1: part of a state machine implemented in four C-modules and one S-module.

This results in lower di/dt noise in worst case situations, a simple way to implement programmable slew rate, and 90% power efficiency. The output buffer meets the 4mA HCT buss driver specification for AC, and the 6mA specification in steady state when the current limit shuts off. ESD protection is >2000V.

Connections between the array and the IO pads are made via special IO modules interspersed with the logic modules. The IO module has inputs for data, slew control, tristate, and separate gates for the input and output latches. The gate inputs are not restricted to a dedicated clock signal, but may each be driven from any pad or internal net.

4. Clock Distribution

Clock distribution is a problem in most large chips. In an FPGA, where the load capacitance may be changed or redistributed to suit each application, it is a greater challenge.

Special distribution networks are provided to deliver high-fanout clock signals to the inputs of any logic or IO module with minimal skew. Each network may be driven directly from an input pad for high speed, or from user-defined internal logic. High speed and low power are obtained by a distributed driver with 90% power efficiency.

Skew is further reduced by automatic placement algorithms that balance the loading on each branch of the distribution tree.

All clock inputs may also be routed in the normal way instead, allowing many local asynchronous clock signals if desired.

parameter	nsec
module input to module input (critical net):	7-8
setup+hold time (module used as flip-flop):	< 6
input pad to IO module output:	5-7
IO module input to output pad:	8
clock distribution net skew:	< 5
in-circuit probe delay (module to pad):	15-20

Table 1: Performance Estimates.
(1.2 micron CMOS, typical process, 5 volts, 25 C).

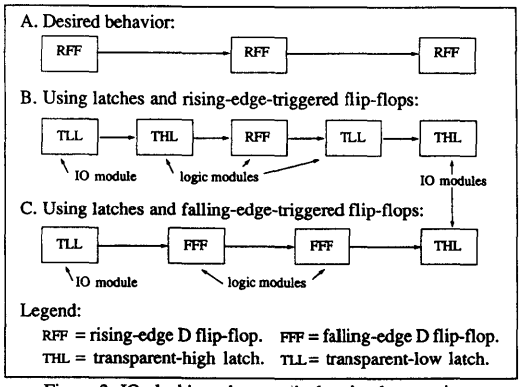

Figure 2: IO clocking--three equivalent implementations.

5. Routing Architecture

Each routing channel contains horizontal tracks divided into segments of various lengths [1]. Surprisingly, the restriction to segments of predefined length does not greatly increase the number of tracks beyond what would be required in the unrestricted case of mask-programmed channels [6].

In an efficient architecture it is inevitable that some nets' routings will be slower than others. The use of a low resistance switch, such as the antifuse, helps to narrow the resulting delay distribution. Further improvements have been obtained by a reduction in the maximum number of antifuses in the worst delay paths, as follows.

In the vertical direction, most nets are routed using a short dedicated segment connected to the module's output driver through an "isolation" transistor (Fig. 3). (The transistor isolates the module circuitry from programming voltages present on the segments). In this case, there are only two antifuses plus the isolation device in the path from the buffer to each input (input A in the figure).† Though this favorable routing can be assured for speed critical nets, generally some 5-10% of the other nets must be placed with an input in some channel beyond the span of the dedicated segment (input B, Fig. 3). In the past, this required use of an uncommitted vertical segment and 4 antifuses.

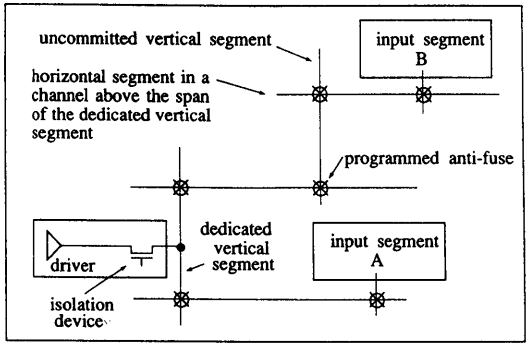

Figure 3: Act-1 Routing

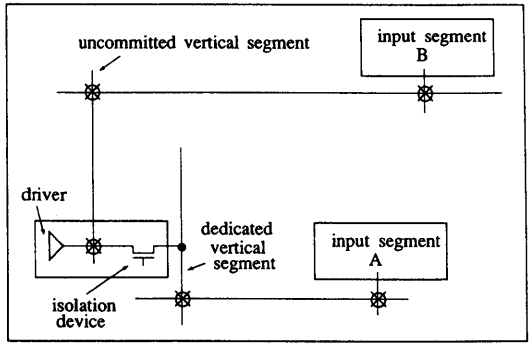

Figure 4: Act-2 Routing

Alteration of the order in which antifuses are programmed and a robust driver circuit permit limited programming of antifuses on the node connecting the driver to the isolation device, without risk of device breakdown [7]. This allows direct connection of the driver to any of several uncommitted vertical segments, as shown in Fig. 4. Since the additional antifuse presents little more resistance than that of the bypassed isolation device, the delay of these nets is not much greater than those using dedicated segments. Prediction of delays prior to placement (when it is not yet known which nets require uncommitted segments) becomes more accurate as well.

Segmented channels represent an unusual layout challenge. They are as dense and large as a memory array, yet not repetitive. (A carefully chosen but irregular mix of segment lengths is provided for good routability.) For this reason, a layout generation program was developed that assembles the channels and modules automatically from the same database used by the routing software. This permits rapid layout of a family of arrays of various sizes by simply rerunning the generator with the appropriate input files.

6. Placement and Routing Software

Several new complexities are added to the placement optimization problem. Macros must be placed in modules of the appropriate type (C or S). Macros hooked to a clock network should be distributed so as to balance the load on the network's branches. There should not be excess demand for uncommitted vertical segments within the same column. Speed critical nets should be routed using only short horizontal segments and dedicated vertical segments.

Nevertheless, new algorithms make it possible to satisfy all these constraints. Nearly all designs with module utilization under 85%, and most designs with utilization under 95%, route without manual intervention. Table 2 summarizes results for several applications. Time for complete placement and routing is about 45-60 minutes on a 68030-based workstation.

7. Programming and Testing

The time required to program an antifuse falls exponentially with the applied voltage. To keep programming time under 5-10 minutes for a chip with nearly a million antifuses, new circuit designs were developed that eliminate the threshold voltage drop along the path from the chip's supply pad to the antifuse being programmed.

Changes have also been made in the addressing circuits. The pass transistor scheme described in [1] is appropriate for cases where there are many short segments in a track.

† Two adjacent horizontal segments in the same track may be connected end-to-end by an antifuse to form a longer segment [1]. For good routability it is necessary to route some small percentage of the nets in this way [6], which adds an antifuse to the path. However, speed critical nets are routed without this additional antifuse.

However in larger chips the number of horizontal segments per unit area decreases to the point that it is possible to address each individual segment directly using only a small proportion of area for the addressing circuitry [7]. The reduction in the number of pass devices in the programming path improves the programming current and lowers the resistance of programmed antifuses, improving performance. The pass transistor scheme is still used in the vertical direction where tracks are highly segmented.

Direct addressing also reduces the time required to test for breakdown of defective unselected antifuses during programming. A complete test for unintended connections between any two segments can be done after the conclusion of programming (despite the fact that it is not possible to uniquely address each individual antifuse once programming commences). The number of vectors required is only logarithmic in the number of nets. Previously, the test for shorts required one or more vectors after each antifuse is programmed.

Proper closure of a programmed antifuse is confirmed by the passage of the programming current. Note that this complete testing for shorts and opens, combined with exhaustive testing of each logic and IO module prior to programming, is more thorough than even a so-called "100% stuck-at fault coverage" test done on a conventional gate array.

Once programming and testing are complete, no increase in resistance of a programmed antifuse or false programming of an unprogrammed antifuse have been observed in 1.8 million accelerated burn-in device-hours [8].

8. Other Circuit Improvements

The Act-1 and Act-2 architectures allow user selection of any internal logic signal for presentation at a "probe" pad. This allows real-time external observation of each net as the chip operates in a system (similar to an in-circuit emulator for a microprocessor). Use of a sense amp circuit greatly increases the speed of the in-circuit probe path.

Another challenge is to keep the gates of thousands of isolation devices pumped to a high voltage during normal operation. A rapid, high-power pump operates when the chip turns on. It is then shut down when the desired voltage is reached and a low-power sustainer pump takes over. The required standby current is under 300uA.

design	logic module utilization	pins per logic module
a) design done in an 8K gate TI gate array	99.5 %	4.28
b) 32 bit datapath, 16x16 mult, state machine	99.4	4.30
c) 2901 ALU (x4)	98.1	4.57
d) DMA controller (x3)	97.1	3.99
e) asynchronous serial ECC	97.0	4.78
f) pipelined fixed point mult, div, sqrt	94.5	3.37
g) state mach, mult/add, datapath, counter	92.7	4.34
h) color crt controller (x3)	87.3	3.83
i) 32 bit datapath w/ sum, compare (x3)	86.8	5.25
j) 40 bit floating point add/sub	86.7	4.33
k) 16 bit datapath, 16x16 mult, state machine	98.1	4.86
l) 2901 (x2)	93.2	4.68
m) DRAM, DMA &SCSI controllers, UART	92.6	4.73

Table 2: Place and Route Examples.

Examples routed in possible implementations of the architecture with 1232 (a-j) and 649 (k-m) logic modules. The notation "(xN)" means the block was replicated N times.

Acknowledgements

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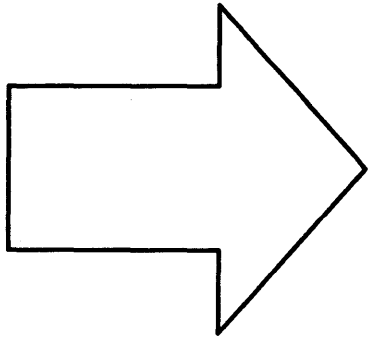

Metastability

Applications Note

Actel Metastability Characteristics

Designers often have asynchronous signals coming into synchronous systems. Typically a flip-flop is used to synchronize the incoming signal with the system clock.

If the asynchronous incoming signal does not meet the setup time requirement for the flip-flop, there exists a window of time where the incoming signal may cause the flip-flop to develop an unknown, or metastable, logic condition. Figure 1 shows this window as t_W. Actual clock setup time of the flip-flop is shown as t_{SU}; propagation delay of the flip-flop is shown as t_{CQ}. Resolution time (t_{res}) between flip-flop output and the next clocked device is the amount of time required for the metastable condition to stabilize.

The duration of a metastable condition is probabilistic. But the designer can calculate how often a metastable state will last longer than a given duration. Mean time between failures (MTBF) can be calculated from the following equation:

$$MTBF = \frac{1}{f_{clk} * f_{dat} * C1\, e^{-C2*tres}}$$

where the constants depend on the ACT™ 1 device characteristics, and:

MTBF = Mean time between failures (s)

f_{clk} = System clock frequency (Hz)

f_{dat} = Incoming data rate (Hz)

e = Natural log base

t_{res} = Resolution time (ns)

C1 = 10^{-9}/Hz

C2 = 4.6052/ns

(Value of C2 derived from circuit simulations.)

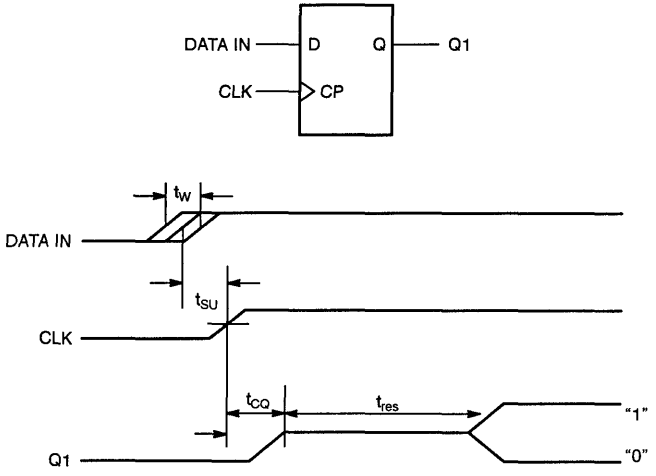

Figure 1. Metastable Condition

Sample Calculation

Using the MTBF equation for a design with a system clock frequency of 10 MHz and a data rate of 1 MHz, various resolution times produce the results shown in Figure 2. Linear increases in resolution time cause exponential increases in MTBF.

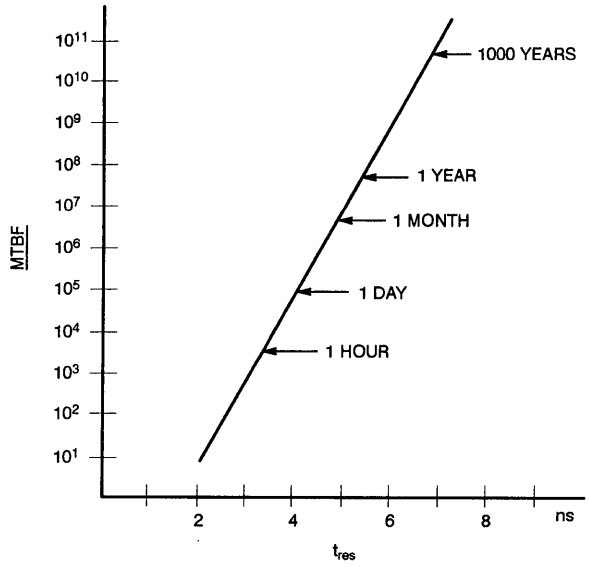

Figure 2. Metastable MTBF as a Function of Resolution Time

Three-Stating A1010/A1020 Designs

Applications Note

During board test and debug it is frequently desirable to place all chip I/Os into a three-stated condition. This provides isolation from other three-stating circuit devices connected to signals common to the ACT™ device. The three-stated condition also allows board test for trace integrity or insertion damage to ACT device pins.

Three-stating a design is easy using the unique debug features of ACT device architecture. Three special pins on the ACT device facilitate three-stating: MODE, SDI, and DCLK.

Three-State Pin Assignments

	PLCC/JQCC			PGA
	44-pin	68-pin	84-pin	84-pin
MODE	34	54	66	E11
SDI	36	56	72	B11
DCLK	37	57	73	C10

Pins SDI and DCLK should remain unassigned by the user or should be defined as input-only.

You may three-state all user-defined pins regardless of their normal mode definition: input-only, output-only, or three-stateable. Each pin can be temporarily three-stated for test and debug purposes.

Figure 1 shows the sequence of three-stating. Seven data bits are clocked into the device, using the SDI pin as data input, and DCLK as clock. The MODE pin distinguishes "test" mode from "normal." The data sequence clocked is {0001011}. After clocking the seventh bit, all user-defined pins enter a three-state condition until MODE is taken low.

Actel Actionprobe™ diagnostic tools allow 100% observability of internal nodes; ACT devices may also be isolated from external board circuitry. Together, these two features provide a powerful debugging feature previously unavailable in custom devices.

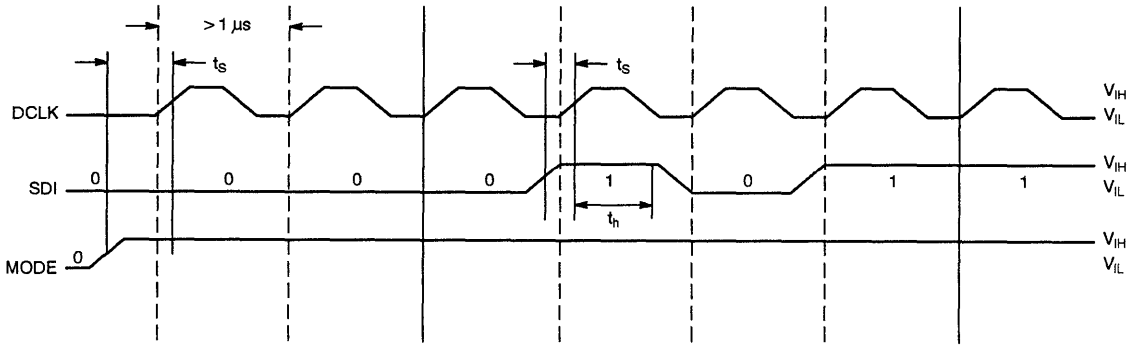

Figure 1. Three-state Timing

Notes:
1. $0\ V \le V_{IL} \le 0.5\ V$; $3.0\ V \le V_{IH} \le V_{CC}$
2. Test mode configuration is a low frequency (< 1.0 MHz) operation.
3. All setup and hold conditions (t_h, t_s) ≥ 250 ns.

5

Socket Selector Guide

Actel has compiled this list of known suppliers for the convenience of our customers. This is simply a list of suppliers that we are aware of rather than a list of recommended sockets, as we have not tested them for reliability. For information on these sockets, contact the manufacturers directly.

Socket Sources for Actel FPGA Packages

Production Sockets

	Lead Count	Source	Through-Hole	Surface-Mount
PLCC	44	AMP	821551-3	821979-3 or 822035-3
		METHODE	213-44-101	213-044-602
	68	AMP	821574-3	822029-3 or 822073-3
		METHODE	213-068-101	213-068-602
	84	AMP	821573-3	821808-1 (high profile)
		METHODE	213-084-101	213-084-602
PGA (11x11)	85	MILL-MAX	510-91-085-11-041	
		McKENZE	PGA-85H-012B1-1107	
PGA (11x11)	101	McKENZE	PGA-101M-012B-1-11B5	
PGA (13x13)	133	McKENZE	PGA-133H-003B-1-13GO	
PGA (15x15)	176	MILL-MAX	510-91-176-15-061	
		McKENZE	PGA-177M-003B-1-1552	
PQFP	100	YAMAICHI	N/A	IC149-100-05-S5
	144	AMP	822114-3/8222115-3	
	160	AMP	822114-4/822115-4	

Zero Insertion Sockets

	Lead Count	Source	Through-Hole	Surface-Mount
CQFP	84	WELLS	619-1000311-001	
	132	ENPLAS	OTQ-132-0.635-01	
	172	ENPLAS	OTQ-172(196)-0.635-02	
PQFP	100	YAMAICHI	IC51-1004-814-2	
	144	YAMAICHI	IC51-1014-KS10418	
	160	YAMAICHI	IC51-1604-845-1	
PGA	85	YAMAICHI	NP35-112-G4-BF85	
	101	YAMAICHI	NP89-12110-G4-BF101	
	133	NEPENTHE	NEP5-132-RS1311	
	176	YAMAICHI	NP89-22508-G4-BF177	
PLCC	44	YAMAICHI	IC51-0444-400	
	68	YAMAICHI	IC51-0684-390-1	
	84	YAMAICHI	IC51-0844-401-1	

CONTACTS:		
	AMP	(408) 725-4914
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	METHODE	(408) 262-3812
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Actel Technical Support

Supporting customers is important to us. We want to offer help in as many ways as possible to suit your particular needs. You can obtain Actel technical assistance by Technical Hotline, Bulletin Board, Customer Training, and our new *Action Facts* system.

Technical Hotline

The Technical Hotline provides information on Actel hardware and software products. Our applications engineers are ready to answer your calls from 7:00 a.m. to 5:30 p.m. PST, Monday to Friday. Our priority is to always have an applications engineer answer your calls "live." In addition to answering your calls, the applications engineers develop other ways of assisting our customers, such as writing application notes, user guides, and quarterly newsletters, creating design examples; and evaluating software.

Bulletin Board

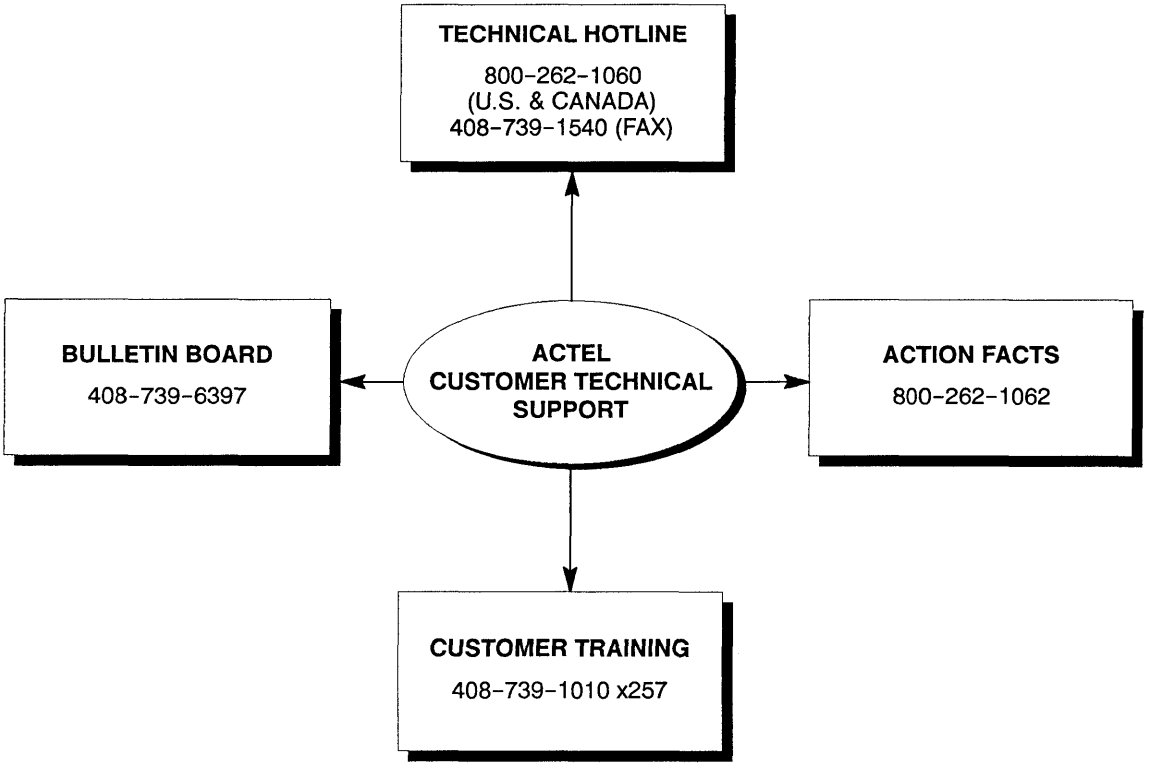
We currently offer information access by a 24-hour bulletin board. Customers can view information, download files such as new macros, and upload design files. The current modem configuration is 2400 baud, 8 data bits, one stop bit, no parity.

Customer Training

Actel offers an introductory two-day course covering all aspects of designing an Actel device. The class covers a discussion of the architecture of both the ACT 1 and ACT 2 families, design methodology, a brief look at the Viewlogic schematic capture and simulation tools, details of the Boolean entry tool (ALES 1), and a thorough examination of the Actel FPGA design software (ALS). With the guidance of the instructor, students develop an example circuit, which is programmed into an Actel device, debugged, and verified in a system board.

Action Facts

We are proud to announce a fast new 24-hour service to our customers — *Action Facts!* Current bugs, software schedules, new package pinouts, the latest application notes, and many more documents can be accessed instantaneously with this new system. Simply call the toll-free number, select the document you require, enter your fax number and extension, and the document will be faxed to you immediately!



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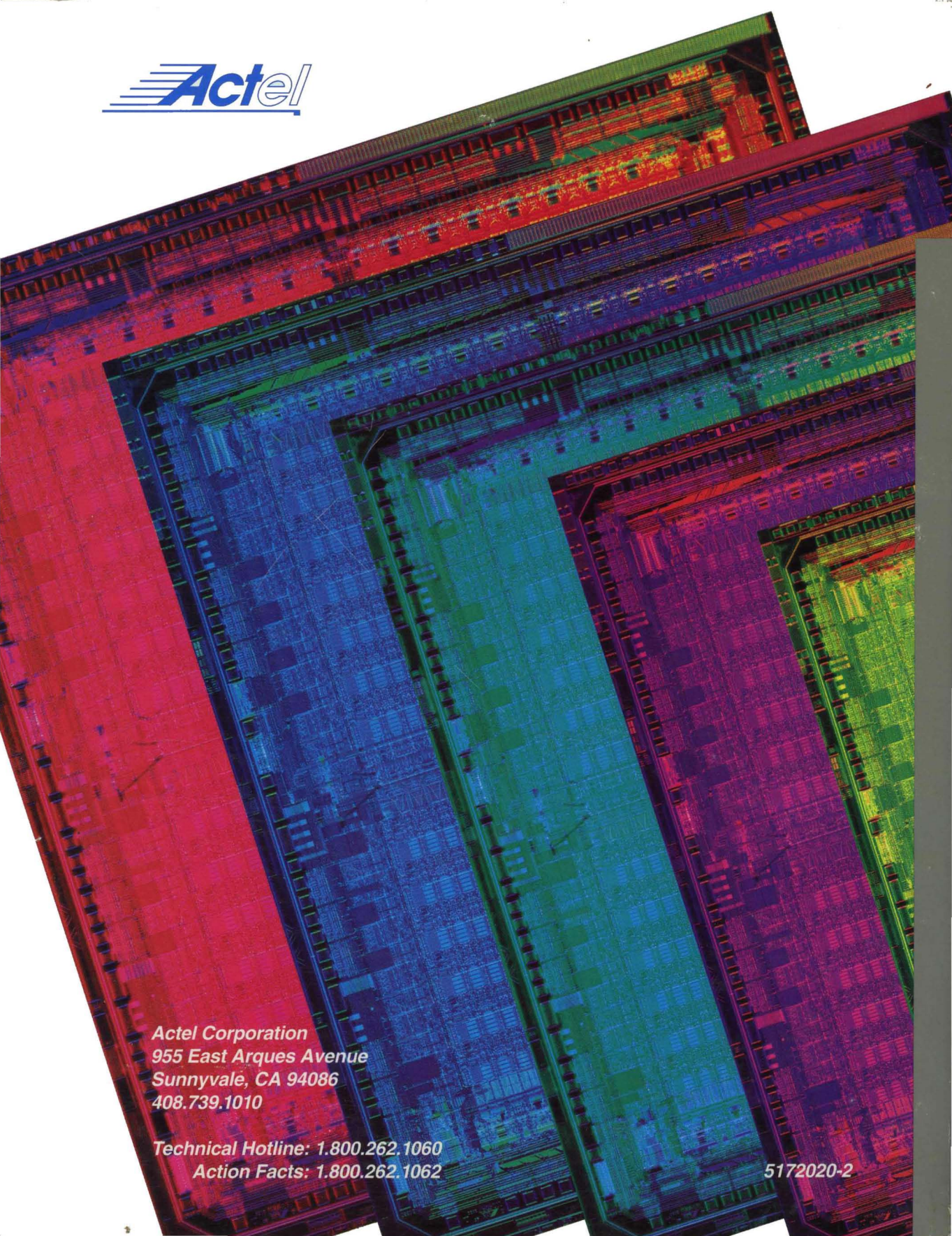

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